UNITRODE
Design Note

OPTIMIZING PERFORMANCE IN UC3854 POWER FACTOR CORRECTION APPLICATIONS

by Bill Andreycak

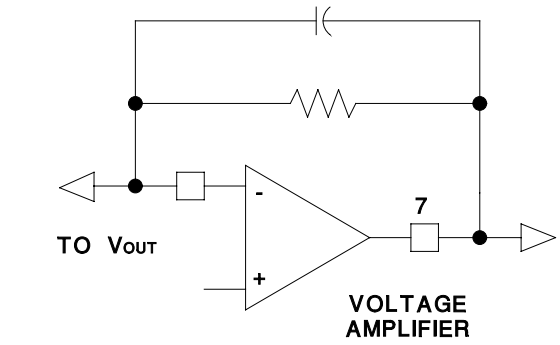
The performance of the UC3854 Power Factor Correction IC in the 250 watt application example has been evaluated using a precision PFC/THD instrument. The result was a power factor of 0.999 and Total Harmonic Distortion (THD) of 3.81%, measured to the 50th line frequency harmonic at nominal line and full load. Users should get similar results at these conditions. as well as over most line and load ranges. Summarized next are the circuit modifications which will improve the performance of most UC3854 PFC applications.

AMPLIFIER CLAMPS

There are a few ways to improve the obtainable power factor and performance in an application circuit. First, the current amplifier outputs should have a "clamp" circuit to limit the output voltage swing and prevent saturation of the amplifier. Without the clamps, overshoot of the current loop could result thus degrading optimal performance. The current amplifier should be clamped with a 7.5 volt zener diode from the output (pin3) back to the inverting input ISENSE(pin4). This example is shown in figure 1. Each amplifier is self protected with internal current limiting, however the IC power consumption may increase during this interval. This clamp is built in to the UC3854A.

CURRENT AMPLIFIER OFFSET VOLTAGE CANCELLATION

The current amplifier maximum input offset voltage is specified as +/- 4 millivolts. Failing to accommodate the offset voltage can causes a spike in the leading edge of the line current following the zero voltage crossing. The spike will occur until the current amplifier comes out of saturation and then resumes normal operation. The worst case offset voltage can be canceled by adding a small current to the biasing resistor (R3) located from I SENSE (pin 4) to ground. This cancellation current (1.1µA), when multiplied by the bias resistor value (3.9K) should be designed to provide the four millivolt offset.



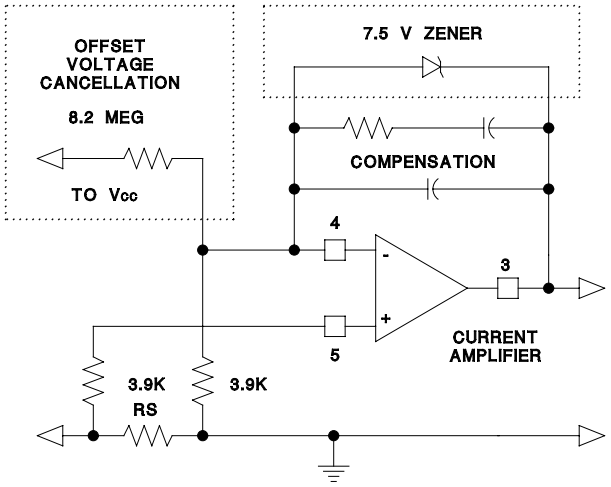


Figure 1.

This offset cancellation current should be obtained from the UC3854 supply voltage. Although a constant current source is optimal, a resistor from

Vcc to the I SENSE input will provide acceptable results as shown also in figure 1. An 8.2 megohm resistor will develop a 1.1 microamp current into the 3.9 K ohm resistor used in the design example. This will generate a 4.28 millivolt offset at the worst case of operation where Vcc is 9 volts. It is adviseable to generate this bias from Vcc and not the UC3854 reference which is inactive until the undervoltage lockout threshold is reached. Bias cancellation circuits from the reference could cause the current amplifier to saturate before the devices crosses its UVLO turn-on threshold. This condition will increase the start-up current of the UC3854 above its 2 milliamp specification and may prevent start-up in certain off-line applications.

CURRENT SENSE AMPLITUDE

The current sense signal should be made as high as possible, and a one volt full scale signal is recommended. Since resistive sensing can cause high power loss many users elect to generate only 100 to 200 millivolts at full load. In comparison, ground noise and slight amplifier offset voltages represent a higher percentage of the total current sense signal. Best results are obtained with the one volt (max) input and lower performance could be incurred with lower current sense signals. especially at light loads and high line voltages. Alternatives to resistive current sense are given below .

CURRENT SENSE TECHNIQUES

An optional technique to resistive current sensing should be considered to reduce power loss in the current sense circuitry. Two current sense transformers can be installed to sum both the switch and diode currents which will recreate the actual inductor current as shown in figure 2. These transformers must be designed to operate over the full range of duty cycles for the PFC converter design which approaches 100% as the line voltages nears zero.

Another current sensing option is to use a DC current sense module or transformer which is typically Hall Effect based. Two application concerns are the cost and accuracy of this technique which may limit its usage to only specialized applications.

A single current sense transformer in series with the PFC switch can also be used. This technique will require some additional circuitry to accurately reconstruct the primary current signal as shown in figure 3. Generating the inductor current signal while the switch is on is a simple task. The difficulty is in reconstructing the inductor current while the switch is off while no current is flowing in the current sense transformer.

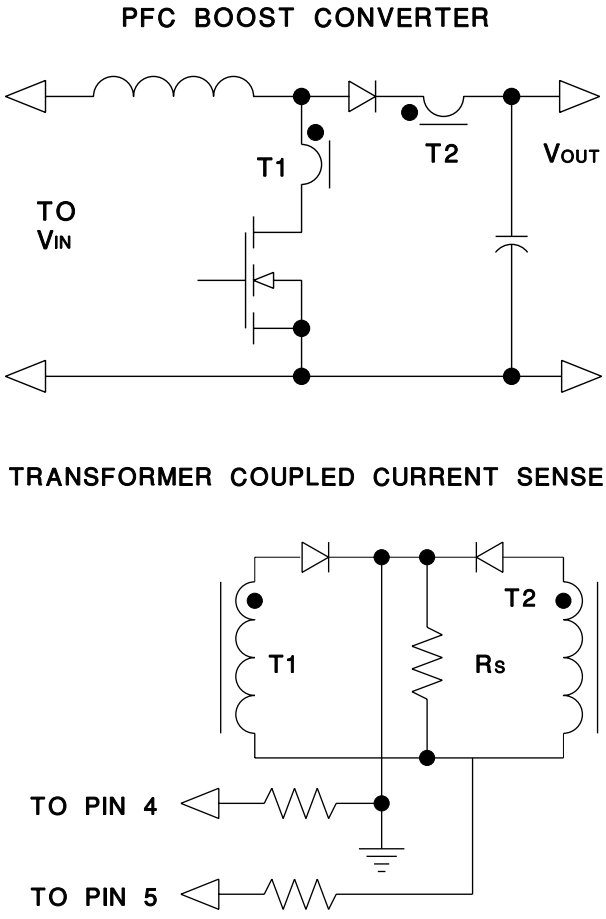


Figure 2.

Inductor current sensing can be simplified to use only one current sense transformer and a current sink circuit. The current sense signal is developed across resistor Rl through diode Dl while the switch is on. A second diode to the current sense transformer develops an identical voltage across capacitor Cl as determined by the current sense resistor primary current and turns ratlo. When the PFC switch turns off capacitor Cl maintains the peak amplitude of the previous current sense signal. Charge is removed by an ideal current sink circuit which lowers the capacitor voltage linearly during one switching cycle. The current is scaled to discharge at the rate proportional to Vout minus Vin(t) divided by the

inductor value, L. The input voltage (Vin) is constantly varying throughout the AC line cycle and so must the capacitor discharge current.

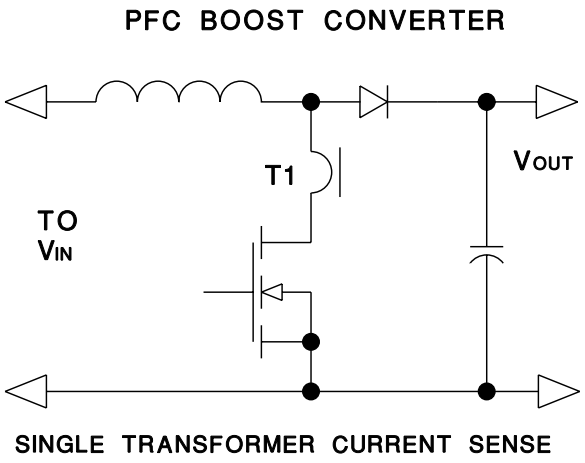


Figure 3.

The circuitry shown in figure 4 will modulate the current sink inversely with the instantaneous line voltage. This will result in the correct discharge of capacitor C1 to reconstruct the actual inductor current. Polarity has been optimized for use with the UC3854 which requires a current sense signal below the ground reference. Another option is to develop a few volts of current sense signal to improve noise immunity and resistively divide this down to the one volt maximum input to the UC3854 controller.

Transistors Ql through Q4 should be identical for best results. Transistors Ql and Q3 are for temperature compensation of the base emitter junctions of Q2 and Q3. Emitter ballasting (50 to 100 mV) will also improve performance. The emitter currents of Ql and Q2 should be similar and equal to Vin/Rin. This current is diverted away from the bases of Q3 and Q4 which limits the total range of sink current to the current sense filter capacitor, CFILT.

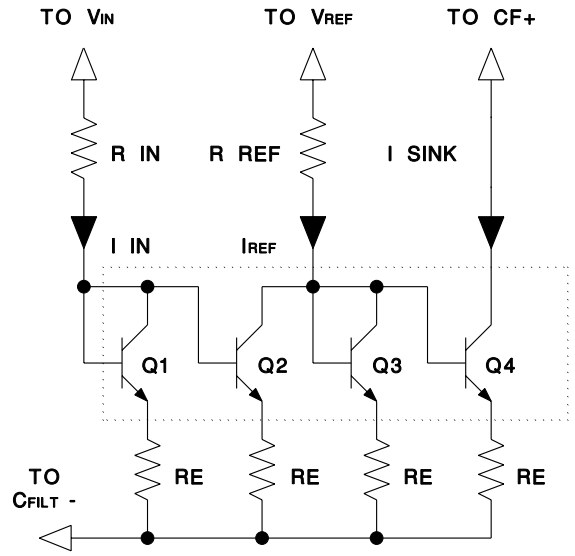
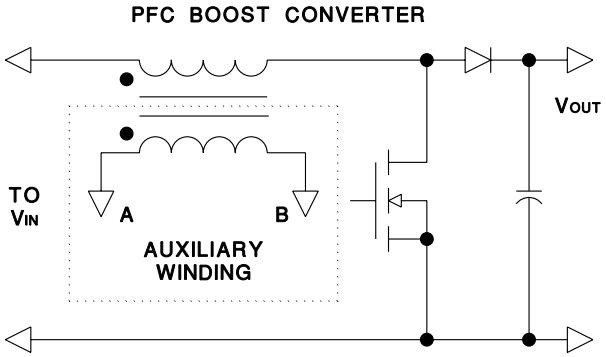


Figure 4.

SCHOTTKY PROTECTION DIODES

Each pin of the UC3854 must be protected from negative voltages exceeding minus three hundred millivolts (-0.3V) maximum. In most applications, only three pins of the IC need external protection Schottky diodes. The gate drive output (pin 16) requires a 1N5820 3 amp Schottky diode to protect against parasitic inductive effects with high speed switching. The multiplier output (pin 5) and peak current limit (pin 2) need Schottky diode protection during abnormal overcurrent conditions and during the initial inrush currents upon power-up. A 1N5817 Schottky diode will provide adequate clamping since the currents are low due to series resistors to the current sense circuitry.



REGULATED AUXILIARY SUPPLY

A secondary winding on the PFC boost inductor can be used to deliver a regulated auxiliary bias supply with few external components as shown in figure 5. Unlike more conventional and unregulated single

REGULATED AUXILIARY BIAS

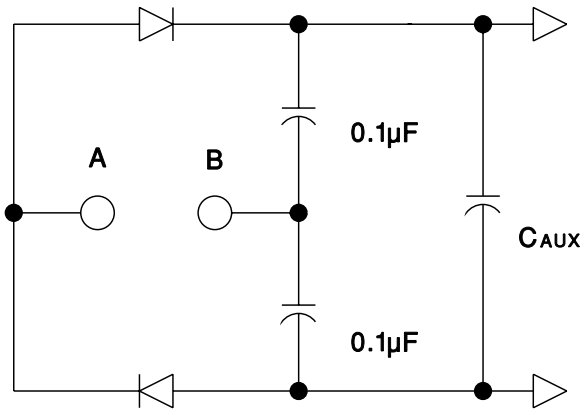


Figure 5.

diode or bridge rectifier techniques, this approach uses two diodes in a full wave configuration.

This arrangement develops two separate voltages across capacitors C1 and C2 each with 120 Hz components. However, when these two are summed at capacitor C3, the line variations are canceled, and a regulated auxiliary bias is obtained. The number of turns on the secondary winding will adjust the bias supply voltage. Additional windings on the boost inductor with similar rectification and filter circuitry can be used to deliver other semi-regulated isolated outputs.

UC 3854 POWER FACTOR CORRECTION EVALUATION KIT

LIST OF COMPONENTS

CAPACITORS (25 VDC)

C1 = 0.47 µF/250 VAC
C2 = 450 µF/450 VDC
C3 = 270 pF
C4 = 1 µF
C5 = NOT USED
C6 = 47 nF
C7 = 0.47 µF
C8 = NOT USED
C9 = 100 mF
C10 = 10 nF
C11 = 1 nF
C12 = 0.1 µF
C13 = 62 pF
C14 = NOT USED
C15 = 620 pF
C16 = 1 µF

DIODES

D1 =4 AMP/800VDC BRIDGE
D2 = UHVP806 FAST RECOVERY
D3 = 18 V ZENER
D4 = 1N5821 SCHOTTKY 3A
D5 = 1N4148
D6 = 1 AMP/100V BRIDGE
D7 = 1N5817 Schottky
D8 = 1N5817 Schottky

FUSE

F1 - 6A/250VAC FUSE

INDUCTOR

L1 = 1 milliHenry Inductor

TRANSISTORS

Q1 = 500V/0.25 ohm NMOS FET
Q2 = 450V/0.5A NPN
Q3 = 50V/.5A NMOS FET

RESISTORS (1/2 WATT)

R1 - 0.25 ohm/5 WATT
R2 = 3.9 K
R3 = 3.9 K
R4 = 1.6 K
R5 = 10 K
R6 = 24 K
R7 =240 K
R8 = 910 K (400V)
R9 = 91 K
R10 = 20 K
R11 = 220 K
R12 = 27 K
R13 = 75 K
R15 = ZERO ohm
R20 = 3 K
R21 = 24 K
R22 = 30 K/3W
R23 = 470 K
R24 = USER SPECIFIED
R25 = 910 K (400V)
R26 = NOT USED (OPEN)

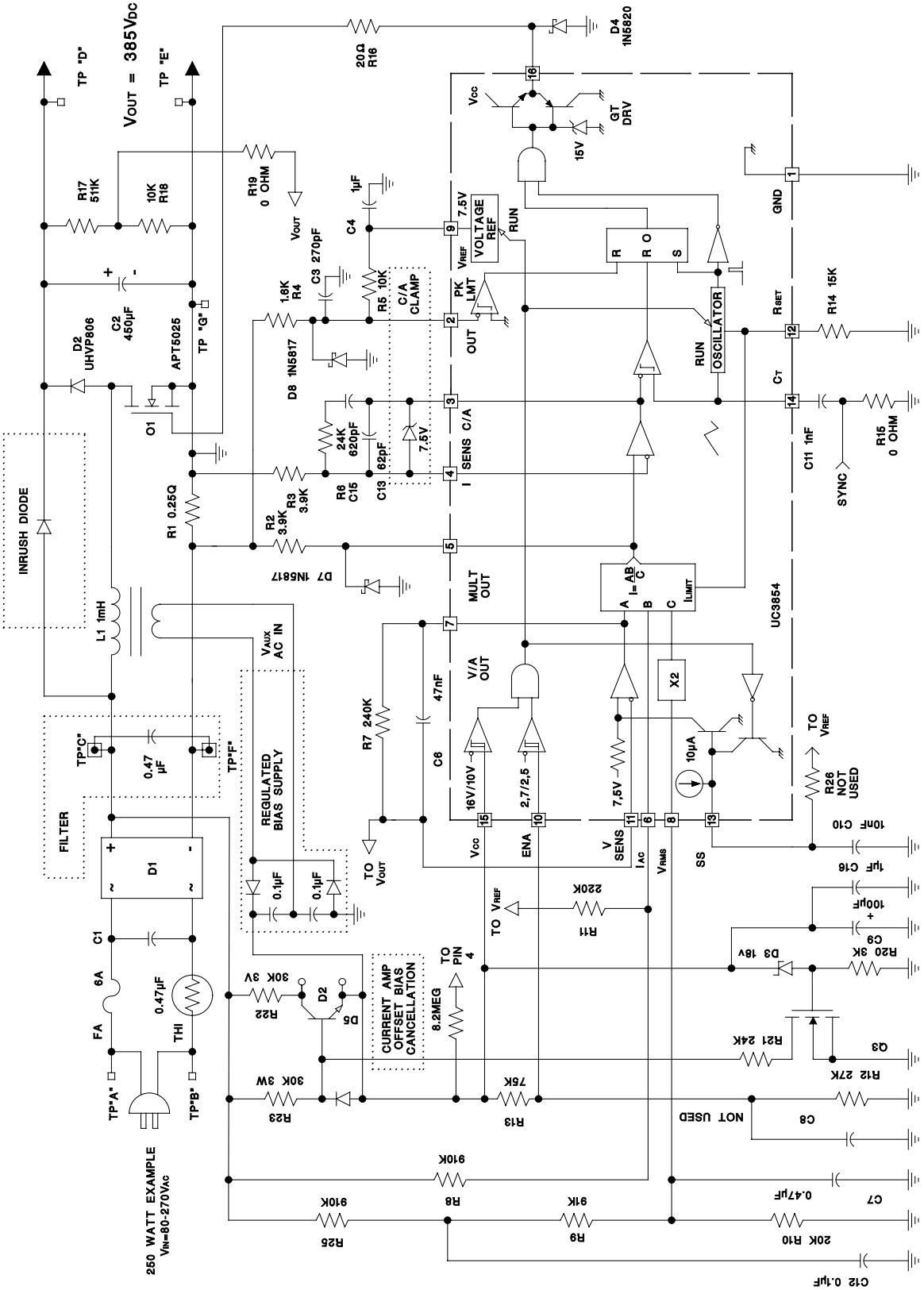
THERMISTOR

TH1 = ohm NTC

INTEGRATED CIRCUIT

U1 = UC3851 PFC CONTROLLER

UC3854 Evaluation PC Board Schematic
250 Watt Power Factor Correction Application



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