UNITRODE
Design Note

Design Considerations for Synchronizing Multiple UC3637 PWMs

by Mickey McClure

As motion control and power interface systems become more complex, the need for more sophisticated control circuitry arises. One common application involves the need for synchronizing multiple pulse width modulators (PWMs). This requirement may result from the need to eliminate beat frequencies when multiple PWMs reside on the same printed circuit board, or from timing considerations in redundant systems where voting between drivers is required.

The UC3637 is an extremely versatile PWM used in many motor control and power driver applications, and the need for synchronization often arises. In order to properly accomplish this, a few simple design rules must be followed. These rules apply primarily to resetting the part's current limit latches.

Figure 1 shows a block diagram of the UC3637. In a single PWM configuration, the triangle waveform, and therefore the operating frequency of the PWM is developed by charging and discharging a capacitor at pin 2, and comparing the voltage across this capacitor to the threshold voltages applied at pins 1 and 3. The design equations for this circuit are discussed extensively in Unitrode Application Note U-102, "Switched Mode Controller For PWM DC Motor Drive."

The most common configuration for synchronized PWMs is a single master PWM driving one or more slave PWMs. In this case the triangle wave is developed by the master exactly as it is in the single PWM case. The master triangle wave is then used to drive the PWM comparators on the one or more slave ICs. The only major concern is resetting the slave current limit comparators.

Figure 2 shows a simple circuit for operating synchronized UC3637 PWMs in a master/slave configuration. The important point to note about this circuit is that the pulse be pulse current limiting feature of the UC3637 is not used. The triangle wave is developed by the master, and used to drive its own PWM comparators as well as the slave PWM comparators. The threshold levels and the C_T pin of the slave IC are tied off to levels which force the current limit comparators to stay in the nonlimit state. With the slave C_T grounded, and the slave $+V_{TH}$ tied to a negative

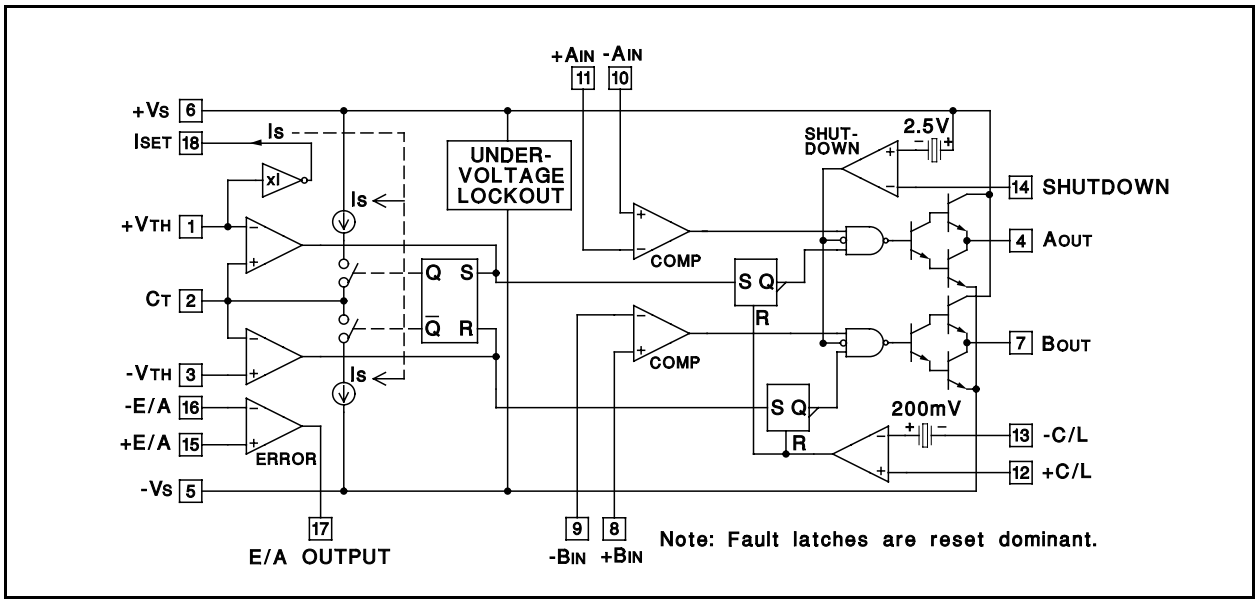

Figure 1. UC3637 Block Diagram

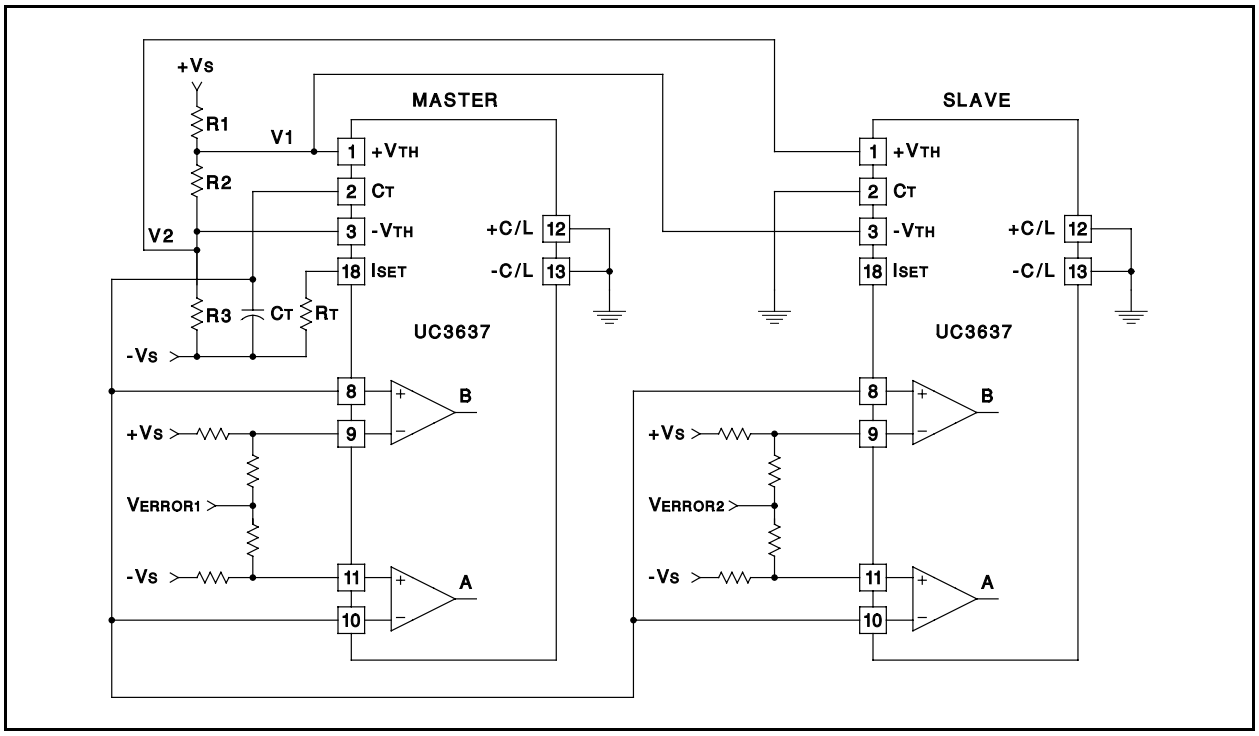

Figure 2. Synchronized PWMs with No Current Limiting

level, the A output current limit comparator will always keep the drive active. The B drive will also be active because -V_{TH} is tied to a positive level. The threshold levels can not simply be tied to the supply rails because those voltages are outside of the common mode range for the comparators.

As long as C_T is kept greater than 1000pF, the input capacitance of the slave comparators will not affect the oscillator frequency. If long signal runs are required, or many PWMs need to be synchronized, it is best to buffer the triangle wave with an op amp at the master IC.

While the circuit of Figure 2 is quite simple, current limiting requirements often rule out its use. The circuit shown in Figure 3 should be used for those applications where both current limiting and synchronization are required. In this circuit, the current limit comparators of the slave PWM are tied to threshold levels of the same polarity but lower magnitude than the threshold levels of the master. Independent pulse by pulse current limiting is accomplished by guaranteeing that the slave current limit comparators get reset each cycle. This can be assured by setting the difference between the master and slave threshold levels (dV) so that even with worst case offsets in both the master and slave ICs the magnitude of the master triangle wave will always be great enough to reset the comparators. The following equations outline a procedure for determining the minimum dV for the positive threshold. The dV for the negative threshold is determined by the same procedure:

1) $dV = V1 - V3$

The minimum dV must be able to compensate for the worst case offset errors of the threshold comparators. These errors result from both offset voltage and bias currents:

2) $V_{ERROR1} = (I_{BIAS}) \bullet Req$

3) $Req = \dfrac{R1 \bullet (R2+R3+R4+R5)}{R1+R2+R3+R4+R5}$

4) $V_{ERROR2} = V_{OS} = 150mV$

The worst case error occurs when the offsets of the master are opposite to the offsets of the slave. The offsets than add to each other to give the minimum dV requirement:

5) $dVmin = 2 \bullet (V_{ERROR1} + V_{ERROR2})$

The set point for dV is determined by adding the

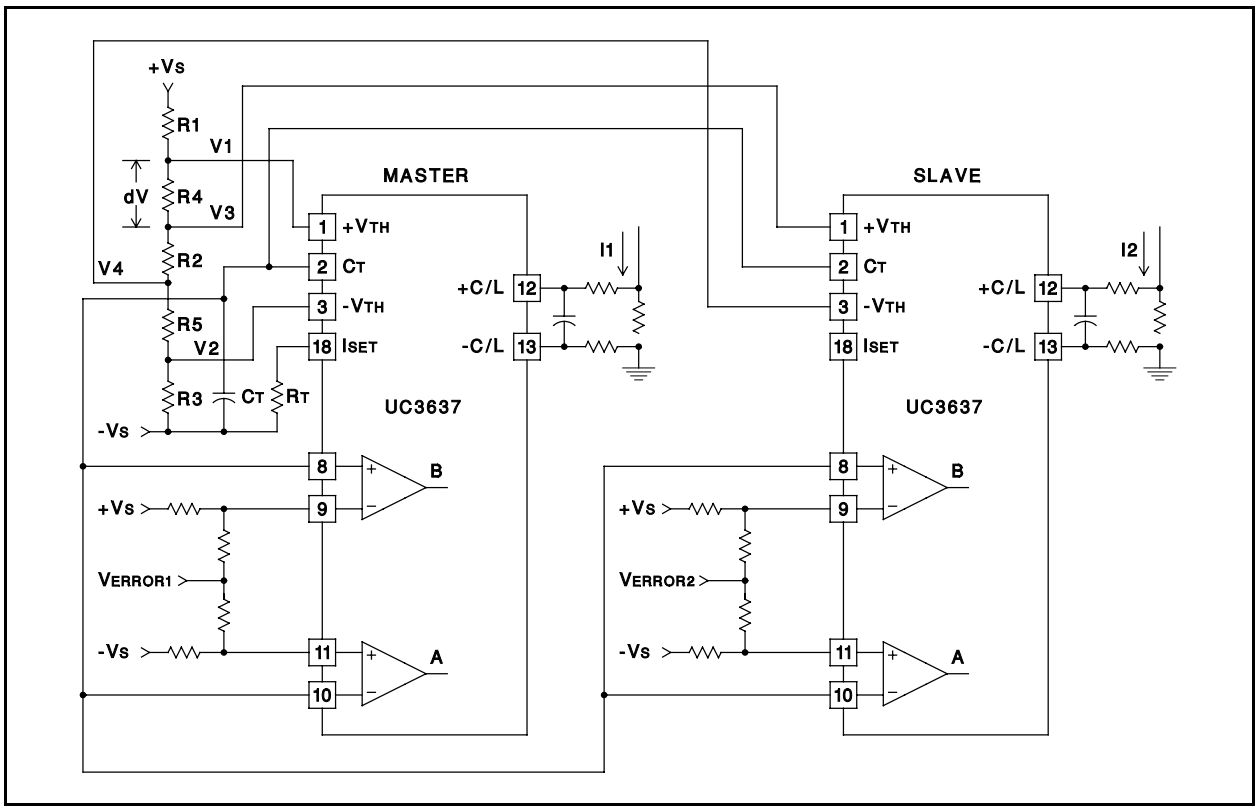

Figure 3. Synchronized PWMs with Current Limiting

maximum tolerance on dV to the minimum dV value. Because dV is set by a resistor divide network with independent terms in both the numerator and denominator of its voltage equation, the total error term is a function of twice the resistor tolerance, as well as the supply voltage. Taking these error sources into account yields the set point for dV:

6) dV_{SET} = dVmin + dVmin • (2) • (resistor tolerance) • (power supply tolerance)

We now select R4 by:

$$7)\ dV_{SET} = \frac{(+Vs - (-Vs)) \bullet R4}{R1+R2+R3+R4+R5} \quad \text{or}$$

$$R4 = \frac{dV_{SET} \bullet (R1+R2+R3+R5)}{(+Vs - (-Vs)) - dV_{SET}}$$

It should be noted that deriving the threshold levels for the slave PWM off of the same divide network as the master allows for much better tracking of dV. Since the difference between the master and slave threshold levels is small compared to the absolute voltage levels, the resistor tolerance becomes much less significant. If the slave threshold levels were derived off of separate networks, the resistor tolerance would affect the absolute threshold level by the tolerance of the resistors, resulting in a much higher percentage change in dV.

While these two simple circuits will suit the requirements of most synchronized systems, there may be cases where more complex circuitry is required. If a digital square wave clock is used to synchronize many PWMs, an integrator may be required to derive the triangle waveform. For certain critical systems, a phase lock loop may be more desirable as a synchronization mechanism. As always, the individual designer must evaluate the system requirements before a final design configuration can be selected.

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