UNITRODE
Design Note

Power Dissipation Considerations for the UC3726N/UC3727N IGBT Driver Pair

by Mickey McClure
Application Engineer
Motion Control Products

Optimized for driving Insulated Gate Bipolar Transistors (IGBTs), the UC3726N/UC3727N IGBT driver pair is a very versatile and cost effective solution for applications where voltage isolation is required. However, care must be taken to insure that the junction temperatures of both the UC3726N and UC3727N are kept below levels which assure reliable operation. The purpose of this design note is to outline the proper thermal design procedure for using this chip set.

BACKGROUND

In order to assure reliable operation, the junction temperatures of both ICs should be kept below 125°C. Although the absolute maximum rating is 150°C, the failure rates for silicon integrated circuits increase significantly at temperatures above 125°C. Also note that the electrical specifications of commercial grade ICs are no longer guaranteed at junction temperatures above 70°C. This does not mean that the device will not function, it simply means that some electrical parameters may fall out of their specified range. Since power devices typically operate with junction temperatures as high as 125°C, it is assumed for purposes of this analysis that operation at these temperatures is acceptable for the application. As always with power drivers, design verification in the lab is recommended. What follows is a thermal analysis of the example circuit designed in Unitrode Application Note U-143A, "New Chip Pair Provides Isolated Drive For High Voltage IGBTs."

POWER DISSIPATION IN THE UC3726N

Power losses in the UC3726N consists of output stage conduction and switching losses, as well as bias losses for the chip itself. Output stage conduction losses result from supplying the UC3727N bias current, the IGBT gate drive current,and the transformer magnetizing current. Each loss component can be calculated individually, and the results added to obtain the total power dissipation.

Since power is only transferred across the pulse transformer during the "full" voltage time period, all of the current required to power the UC3727N and the IGBT gate must be supplied during this 1/3 portion of the duty cycle. To calculate the loss associated with this power transfer, the rms value of the average current required to power the UC3727N and the IGBT gate must be calculated. For the example circuit described in U-143A, the average IGBT gate current is equal to:

$$1)\ I_G = 2 \bullet Q_G \bullet F = 2 \bullet 110nC \bullet 15kHz = 3.3mA$$

The typical bias current for the UC3727N is 24mA, resulting in a total average supply current of 27.3mA. Since the average current must be delivered in 1/3 of the duty cycle, the peak current is determined by:

$$2)\ I_{SUPPLY} = \frac{27.3mA}{0.33} = 82.7mA$$

To determine the loss resulting from this current (PL_{SUPPLY}), the rms value of the current is multiplied by the rms value of the total voltage drop of the upper and lower drive stages of the UC3726N:

$$3)\ PL_{SUPPLY} = (2.3V \bullet \sqrt{0.33})(82.7mA \bullet \sqrt{0.33}) = 63mW$$

To determine the loss resulting from the transformer magnetizing current, the rms value is determined for both the "full" time ($I_{MAGFULL}$) and "half" time ($I_{MAGHALF}$) currents. With a peak magnetizing current level of 35mA, the corresponding rms currents are calculated as:

$$4)\ I_{MAGFULL} = 35mA \bullet \sqrt{\frac{0.33}{3}} = 11mA$$

$$5)\ I_{MAGHALF} = 35mA \bullet \sqrt{\frac{0.66}{3}} = 16mA$$

The losses resulting from these currents are a function of the rms value of the appropriate voltage drops in the UC3726N. For the "full" time the voltage drop is the total saturation drop of the output drivers. For the "half" time the voltage drop is the sum of the drop across the half on driver (V_{CC} - 0.6 • V_{CC}) and the drop across the full on driver (0.4V):

6) $PL_{MAGFULL} = 11mA \bullet 2.3V \bullet \sqrt{0.33} = 14mW$

7) $PL_{MAGHALF} = 16mA \bullet 12.4V \bullet \sqrt{0.66} = 161mW$

The power dissipated due to switching loss is difficult to calculate, and some simplifying assumptions must be made. Since the transition from half to full voltage occurs when the transformer current reaches zero, it is assumed that the switching loss is very close to zero for this transition. For the transition from full to half voltage it is assumed that the transformer current remains constant as the sum of the peak magnetizing current and the peak supply current throughout the whole transition. This is a reasonable worst case assumption since the load is highly inductive. Furthermore, the fall time for the full to half driver is much slower than the rise time for the zero to full driver, and therefore the full to half driver is the primary contributor to switching loss.

Referring to Figure 3 of U-143C, the half driver fall time is 200ns, yielding a duty cycle of 0.08 for this calculation. Since the voltage transitions from 28 to 18V, the switching loss component is calculated as:

8) $PL_{SWITCH} = (35mA + 82.7mA) \bullet \sqrt{0.08} \bullet (2 \bullet \sqrt{0.08} + 10 \bullet \sqrt{\frac{0.08}{3}}) = 72mW$

The 2V term comes from the saturation drop of the output driver, and the 10V term comes from the 10V swing from 28V to 18V. In order to take into account other miscellaneous switching losses, the PL_{SWITCH} term is rounded up to 100mW.

The final dissipation calculation is the bias loss for the UC3726N itself. Using a single +30V supply, the typical bias current for the UC3726N is 26mA. This takes into account an additional 0.4mA/V I_{CC} component for each volt above the 20V supply level specified in the data sheet. The resulting power loss is:

9) $PL_{BIAS} = 30V \bullet 26mA = 780mW$

If an external +5V logic supply is available, it is highly recommended to power the logic supply (V_L) from this source. The bias loss in this case becomes a function of the reduced V_{CC} bias current and the bias current requirement for the external logic supply:

10) $PL_{BIAS} = 30V \bullet 16mA + 5V \bullet 13mA = 545mW$

The total power dissipation for the IC is calculated by adding the individual power loss components. If an external logic supply is not used, the total power dissipation is calculated as:

11) $PL_{TOT} = 0.063W + 0.014W + 0.161W + 0.100W + 0.780W = 1.12W$

With an external logic supply, the total power dissipation is 0.88W.

For a 16 pin plastic "batwing" package (N package) the worst case θ_{JA} is 50°C/W for typical PC board mount, resulting in a temperature rise of 56°C with no external logic supply. Using a max junction temperature of 125°C, the maximum ambient temperature for the IC in this application is 69°C. With an external 5V power supply, the worst case temperature rise is 44°C. If higher ambient temperatures are required, or if keeping the junction temperature below 70°C is required, heat sinking will be necessary.

POWER DISSIPATION IN THE UC3727N

The power dissipation calculations for the UC3727N are much more straight forward. The losses consist only of the bias loss for the IC, and the output stage conduction and switching losses. In order to determine the average output stage loss, the gate drive energy (W_{GD}) is determined by:

12) $W_{GD} = 2 \bullet \frac{1}{2} \bullet C_G \bullet V^2 = \left(\frac{Q_G}{V}\right) \bullet V^2 = Q_G \bullet V$

The factor of 2 results from the fact that the gate drive circuit must charge and discharge the gate every electrical cycle. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. This leads to the power lost due to the gate drive:

13) $PL_{GD} = \frac{W_{GD}}{T} = \frac{Q_G \bullet V}{T} = Q_G \bullet V \bullet F = 110nC \bullet 20.5V \bullet 15kHz = 34mW$

This is a worst case assumption since the power loss will actually be shared by the output driver and the gate resistor. In most cases there will be significant sharing of this loss with the gate driver resistor since

the output impedance of the driver stage is low. Because this calculation takes into account the total energy transferred to the gate, both switching loss and conduction loss are included.

To determine the power loss due to bias current, the total voltage drop of the UC3726N is subtracted from V_{CC}, and this result is multiplied by the bias current:

$$14)\ PL_{BIAS} = (30V - 2.3)(24mA) = 664mW$$

The resulting total power loss is calculated as:

$$15)\ PL_{TOT} = 0.034W + 0.664W = 0.698W$$

For a 20 pin plastic package (N package) the worst case θ_{JA} is 79°C/W for typical PC board mount, resulting in a temperature rise of 55°C. This leads to a maximum ambient temperature of 70°C for this application. Again, if it is desired to operate in a higher ambient, or to keep the junction temperature lower, heat sinking will be necessary.

TEST RESULTS

The UC3726/UC3727 IGBT Driver Pair Evaluation Board (See U-143C) was used to test the thermal characteristics of the driver pair. The evaluation board represents a typical PC board layout, where no heat sinking is provided except for a small copper ground plane. All electrical parameters for the circuit were programmed as described in U-143C. With a V_{CC} of 30V, and no external logic supply, driving the IGBT at 15kHz resulted in a lead temperature of 70°C for the UC3726N, and a case temperature of 47°C for the UC3727N. Assuming a θ_{JL} of 12°C/W for the UC3726N results in a junction temperature rise of 58°C, very close to the predicted rise.

Assuming a θ_{JC} of 35°C/W for the UC3727N results in a junction temperature rise of 46°C, which is significantly lower than the predicted value, indicating that the IC is dissipating less power than predicted. While this is a positive development in this case, it further points out the need to bread board circuits to prove out theoretical calculations.

Using an external +5V logic supply resulted in a lead temperature of 57°C for the UC3726N, and as expected had no effect on the case temperature of the UC3727N. The corresponding temperature rise of the UC3726N junction is 42°C. This difference in temperature rise of 16°C can be highly significant depending on the application.

As stated previously, properly heat sinking the ICs will result in much lower junction temperatures. While this technique leads to additional cost and complexity, it can lead to much greater design flexibility, particularly for driving IGBTs with very high levels of gate charge. Also, since the UC3726N features a "batwing" style package, heat is very effectively conducted to the center leads. Increasing the ground plane connected to these leads beyond what is shown on Figure 17 of U-143C will further reduce the junction temperature.

If other IC packages are used than those described in this design note, the power loss and maximum junction temperature calculations are the same. Refer to Packaging Section of the Unitrode Product and Applications Handbook for thermal impedance data.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460