UNITRODE

Design Note

An Intelligent Overvoltage Protection Scheme for 3V to 10V Power Supplies

by Chuck Melchin

Protecting sensitive circuitry from power supply overvoltage conditions is a concern for any system designer. Overvoltage conditions can be caused by transient load changes, loss of the power supply control loop, accidental miswiring or incorrect module installation. An intelligent protection scheme can be accomplished utilizing the UC3908 Programmable Voltage Clamp.

The UC3908 monitors a power supply output voltage and draws less than 100µA if no overvoltage condition is present. If an overvoltage condition occurs, the UC3908 will act as a shunt regulator and attempt to regulate the power supply voltage to a programmed level by internally shunting current from VC to ground. If the shunted current exceeds a maximum value, or if the overvoltage condition is of a long enough duration to trip the IC's internal thermal sense circuitry, the device provides a gate signal to an external SCR. The SCR crowbars the power supply output, while the UC3908 internally latches the shunt regulator fully on. The UC3908 also provides a overvoltage indicator signal through an open collector output any time an overvoltage condition occurs.

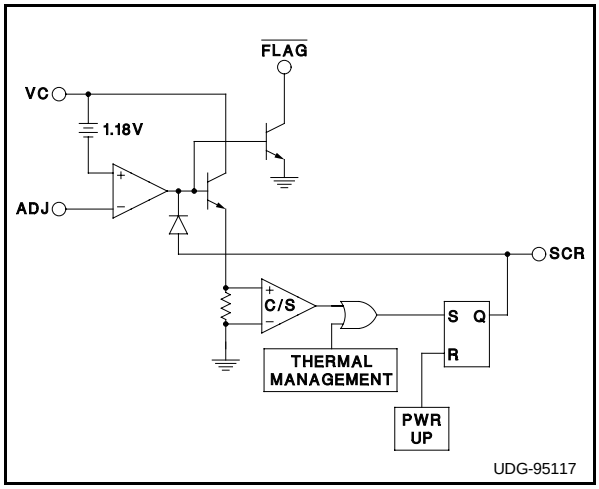

Figure 1. UC3908 Functional Block Diagram

Basic Operation of the UC3908 can be seen in the following flow chart:

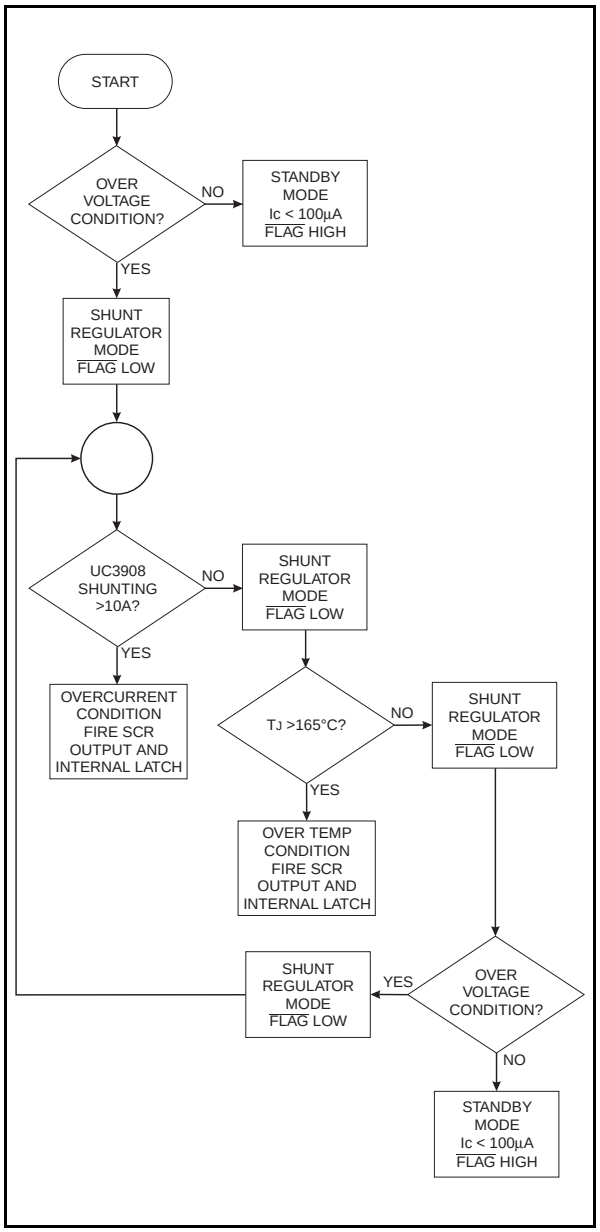

Figure 2. UC3908 Operational Flowchart

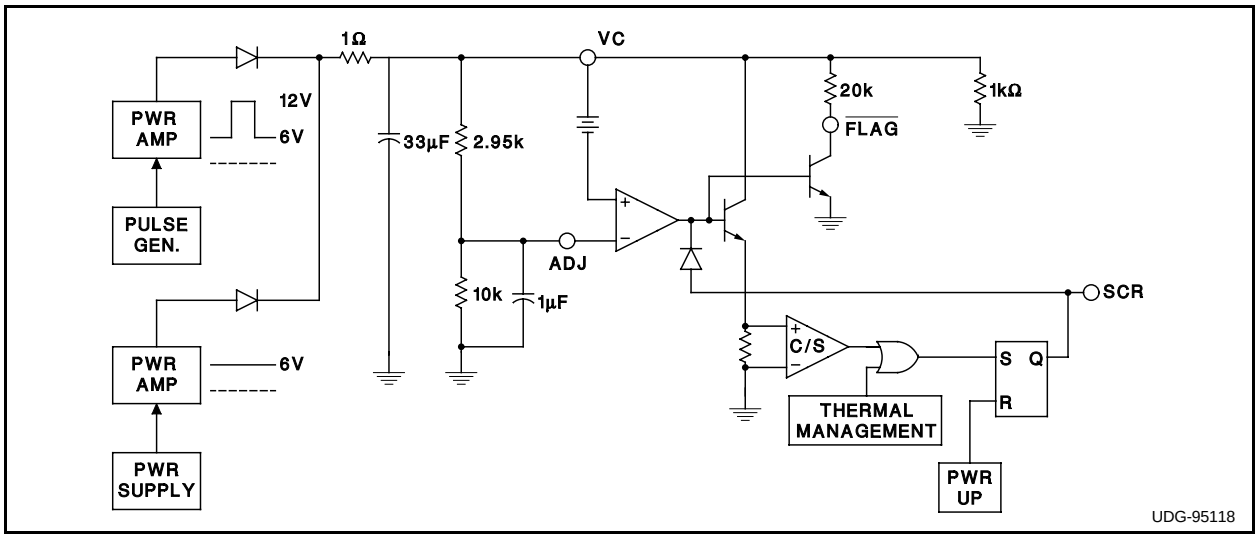

Figure 3. Lab Evaluation Circuit

Measured performance

The UC3908 can be evaluated using the circuit shown in Figure 3. It is intended to give the user the ability to simulate power supply overvoltage conditions with control over duration and magnitude of the transient. Four different real world scenarios using the UC3908 to protect the load of a 5V power supply were simulated using this circuit with the results described below.

The first condition shown (Figure 4) is an overvoltage transient with a magnitude resulting in less than 10A shunted by the regulator. The fault duration is small enough not to heat the device past its thermal trigger point. The resulting waveforms show FLAG going low to indicate a fault, 6A of shunted current for the duration of the transient and VC raising as a result of the shunted current. The SCR output stays low in the absence of an overcurrent or thermal firing of the internal latch.

The second set of waveforms (Figure 5) show an overvoltage condition of a duration and magnitude sufficient to cause a T_J of greater than 165°C. This causes a firing of the internal latch and SCR output through the thermal management circuitry. The FLAG output is low for the duration of the entire overvoltage condition. VC stays at 5V until the SCR output goes high and the internal latch turns on the shunt transistor hard. At this time VC drops to the V_{SAT} of the

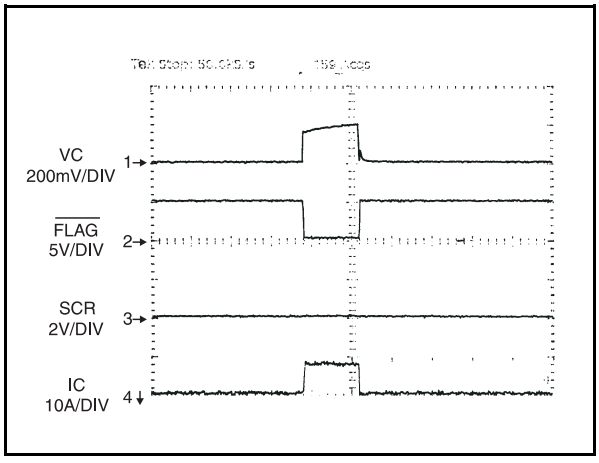

Figure 4. Shunt Regulation of O.V. Condition

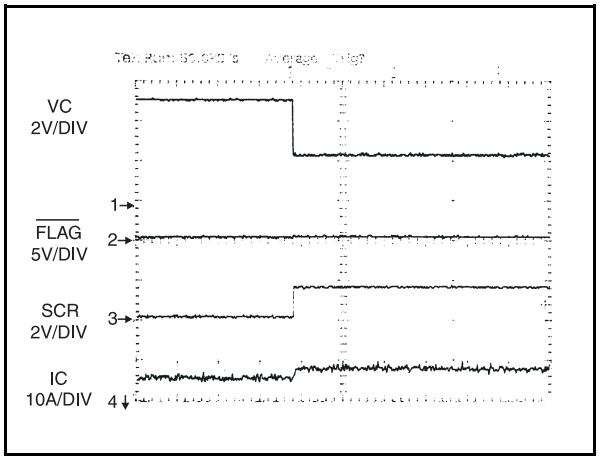

Figure 5. Thermal Firing of SCR Output

shunt and IC raises from its original magnitude of about 6A to the compliance of the power supply, which for this example was set at about 8A.

Figure 6 shows the UC3908 firing its SCR output and internal latch due to an overvoltage condition of sufficient magnitude as to result in a shunted current that exceeds the maximum value of 10 to 14A. Again the $\overline{\text{FLAG}}$ signal is high until the overvoltage condition occurs, causing it to go low. VC is at its nominal value of 5V until the transient current of @15A causes the overcurrent circuitry to fire the SCR output and internal latch. At this time VC drops to the V_{SAT} of the shunt transistor. In this example the overvoltage condition has been simulated as a long term or permanent condition rather than a transient.

The last example (Figure 7) is similar to the previous in that an overcurrent condition causes the firing of the SCR output and internal latch. But in this case it is a transient condition which allows us to observe the effects of the internal latch. In this simulation the internal latch turns the shunt on hard, and VC drops to its V_{SAT}. However, when the transient is through and IC returns to its nominal value, the shunt remains latched on and the V_{SAT} drops to a lower voltage. The $\overline{\text{FLAG}}$ also remains low due to the internal latch, and the SCR output voltage drops to VC minus approximately 1V.

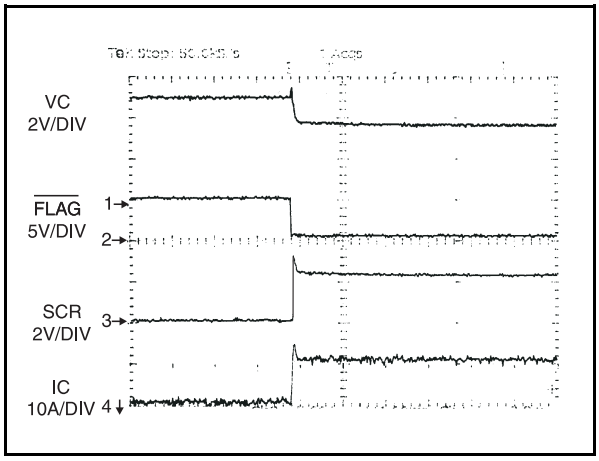

Figure 6. Overcurrent Firing of SCR Output

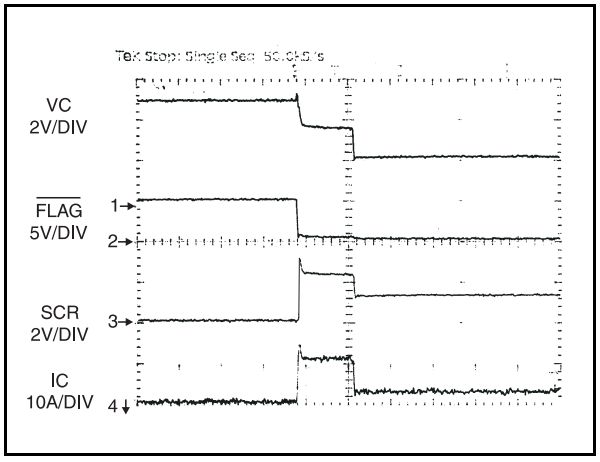

Figure 7. Effect of Internal Latch During Overcurrent Condition

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