UNITRODE

Design Note

UCC3911 Demonstration Board

By David Salerno

The UCC3911 demo board comes fully assembled, ready to test. It provides complete over-charge/over-discharge protection, as well as short circuit protection, for two Lithium-Ion cells. The user needs only to supply the two cells (or two power supplies) and a load (or a charger).

The board has been made approximately the size that would fit into a battery pack. The values selected for C1, C2 and CDLY will allow the charging of approximately 1500µf of load capacitance without tripping the overcurrent. This can be changed by the user if desired. Refer to the application section for more details.

The demo board schematic with the high current paths is shown in Figure 1. A parts list is given in Table 1. Note that test pads are provided for monitoring the KILL, OV, UV and LPWARN outputs, if desired.

Connecting the Cells

It is recommended that the Cell1(-) connection be made first, then the Cell2(+) connection. Pads for soldering to the battery tabs are provided on the back side of the board. They are labeled as Cell2 (+) and Cell1(-). This allows the board to sit right on top of the cells, eliminating the resistance and inductance associated with wiring. In addition, large plated through holes with the same labels are provided for attaching wires to an alternate power source, such as two adjustable lab supplies. The connection from the board to the middle of the two cells is made using the small plated through hole connected to R2, near the center of the board. This connection should be made after the other two, and can be done using a small wire, as the current is extremely low.

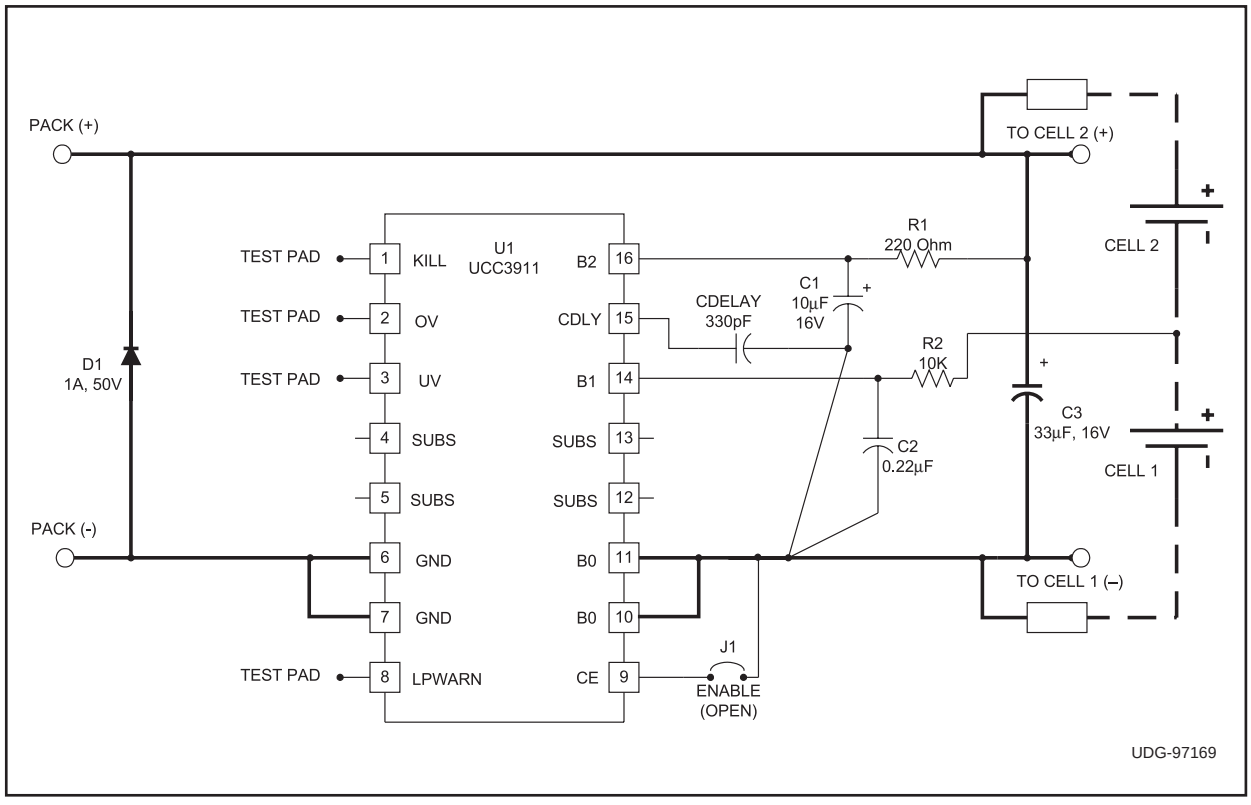

Figure 1. Demo Board Schematic

Capacitor C3 is required to assure a low supply impedance at the IC. This helps to mitigate the effects of battery ESR and ESL on circuit performance. This is especially important under short circuit conditions, where large di/dt's may otherwise cause a “rebound” or overshoot at turn-off.

Connecting the Load or Charger

The load (or Li-Ion charger) is connected to the circuit using the large plated through holes labeled Pack(+) and Pack(-).

Initializing & Enabling the IC

The UCC3911 may be disabled by placing a shorting jumper in the J1 location. This keeps the internal FET off, preventing charge or discharge of the cells, by holding the CE pin low. This also resets the “kill” latch and initializes the state machine. The circuit is enabled when the jumper is removed. The demo boards are shipped without the jumper in place. To initialize the IC, it is necessary to momentarily bridge the J1 pads after the cells are connected. When the jumper is removed, the circuit will be enabled. This only needs to be done once. To re-enable the IC after an overcurrent (or undervoltage) shutdown, momentarily connect the Pack output to a charger.

UCC3911 APPLICATION INFORMATION

While the UCC3911 is capable of providing overload and over and undervoltage protection of both cells with virtually no external parts, the demands of true short circuit protection require some passive external components. These are discussed in detail below.

Referring to Figure 1, diode D1 acts as a clamp across the battery pack output terminals to prevent damage to the IC from inductive kick when the pack current is shut off due to an overcurrent or over/undervoltage condition. It also provides reverse polarity protection during charge.

To prevent a momentary cell voltage drop, caused by large capacitive loads, from causing an erroneous undervoltage shutdown, an RC filter is required in series with the two battery sense inputs, B1 and B2. The resistors (R1 and R2) are sized to have a negligible impact on voltage sensing accuracy. The capacitors (C1 and C2) should be sized to provide a time constant longer than the overcurrent delay time. In the example of Figure 1, they are sized for a nominal 2.2msec time constant. They do not need to be low ESR style caps, as they see no ripple current. A larger resistor value and smaller cap value can be used on the B1 input due to the extremely low input current on this pin. (Note: the 5uA current listed in the data sheet for B1 is for test purposes. The current in this pin is guaranteed by design to be much less than 1uA.)

The overcurrent delay capacitor, C_{DELAY}, is discussed in the data sheet. This cap sets the time delay introduced before turning off the UCC3911's internal FET, after the overcurrent threshold is exceeded. If no capacitor is used, the nominal delay is 100μsec. To charge large capacitive loads without tripping the overcurrent circuit, a small cap (typically less than 1000pF) is used to extend the delay time. The approximate delay time is given below and shown graphically in Figure 2.

$$T_{DELAY}(\mu\,\text{sec}) = 25 + (25 + C_{DLY}(pf)) \bullet 0.4 \bullet V_{BATT}$$

The amount of time required will be a function of the load capacitance, battery voltage, and the total circuit impedance, including the internal resistance of the cells, the UCC3911's on resistance, and the load capacitor ESR. The required delay time can be calculated from:

$$T = -R \bullet C \bullet \ln\left(\frac{I \bullet R}{V}\right)$$

In this equation, R is the total circuit resistance, C is the capacitor being charged, I is the overcurrent trip current (5.25 Amps nominal), and V is the battery voltage. Using the minimum trip current of 3.5 Amps and the maximum battery voltage of 8.4V, the worst case maximum delay time required is defined as:

$$T_{MAX}(\mu\,\text{sec}) = -R \bullet C(\mu f) \bullet \ln\left(\frac{R}{2.4}\right)$$

In the example of Figure 1, Cdelay, C1 and C2 are sized to drive a 1500μF load capacitor. If large capacitive loads (or other loads with surge currents above the overcurrent trip threshold) are not being applied to the pack terminals, the overcurrent delay

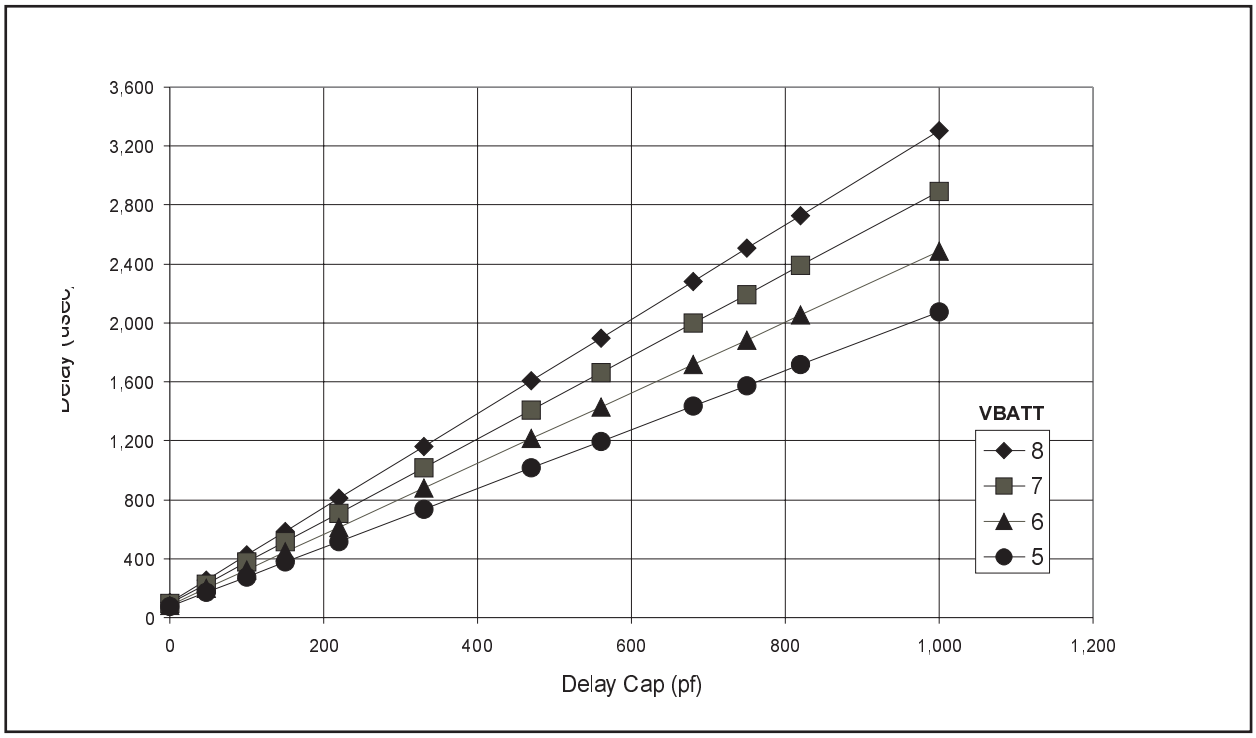

Figure 2. Nominal Overcurrent Delay Time vs. CLDY and VBATT

time can be short. In this case, it may be possible to eliminate Cdelay, as well as R2 and C2 altogether (replacing R2 with a short). In addition, the time constant of R1 and C1 can be made much shorter. R1 and C2 are still necessary, however, to assure proper operation under short circuit conditions. It is important to maintain a minimum R1/C1 time constant of 100μsec. (For example, R1 and C1 could be reduced to 100 Ohms and 1μF.)

Capacitor C3 prevents excessive overshoot at turn-off due to parasitic inductance. This is especially true under short circuit conditions, when a very high di/dt will occur at turn-off. A minimum of 22μf is recommended. It should be placed close to D1's cathode and pins 10 and 11 of the UCC3911.

Jumper J1, while in place, keeps the UCC3911 inhibited (pack output open). The jumper is removed or cut as the last step in manufacturing the battery pack to enable the output.

The four substrate pins (4, 5, 12, 13) may be soldered to electrically isolated copper pads to aid in heat transfer when operating at high load currents.

For more complete information, pin descriptions and specifications for the UCC3911, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

Reference Designator	Part Description	Part Value	Manufacturer	Part Number
C1	Tantalum Capacitor	10μF, 16V, “B” Case	Sprague	595D106X0016B2T
C2	Ceramic Capacitor	0.22μF, 16V, 0805 Case	AVX	0805YC224KAT
C3	Tantalum Capacitor	33μF, 16V, “C” Case	AVX	TAJC336K016R
C_{DLY}	Ceramic Capacitor	330pF, 50V, 0805 Case	COG	
D1	Fast Recovery Diode	1A, 50V, SMB Case	Diodes, Inc.	FR1A
R1	Metal Film Resistor	220Ω, 1/10W, 5%, 0805 Case		
R2	Metal Film Resistor	10KW, 1/10W, 5%, 0805 Case		
U1	Two Cell Protector IC		Unitrode	UCC3911

Table 1. Parts List

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