UNITRODE

APPLICATION NOTE

A NEW FAMILY OF INTEGRATED CIRCUITS CONTROLS RESONANT MODE POWER CONVERTERS

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ABSTRACT

A new family of integrated circuits is introduced. Devices from this family implement the necessary architecture to control a broad range of resonant mode converters. Key features in the areas of switch timing, fault management, and soft-start technique arc unique to this family. Individual devices arc customized to handle off-line or DC to DC. single-ended or dual-switch, zero-voltage-or-current-switched configurations. Specific application to three different resonant mode converters is mentioned.

SURVEY OF EXISTING CONTROL INTEGRATED CIRCUITS

Since 1986, interest in resonant mode power conversion has exploded in the technical conferences. IC makers have been quick to respond with offerings of control ICs. Table 1 is a list of chips available at the present time. To simplify thinking, the first three parts listed are essentially the same design as arc the last two. There arc significant differences in features and performance levels between the three groups. However, a common operational philosophy is shared by all: fixed-pulse-width variable-frequency. This approach has been applied to zero-current-switched (ZCS), quasi-resonant mode converters with reported success.

Table 1. List of Resonant Mode Control ICs

LD405
GP605
CS3805
- - - - - -
UC3860
- - - - - -
MC34066
CS360

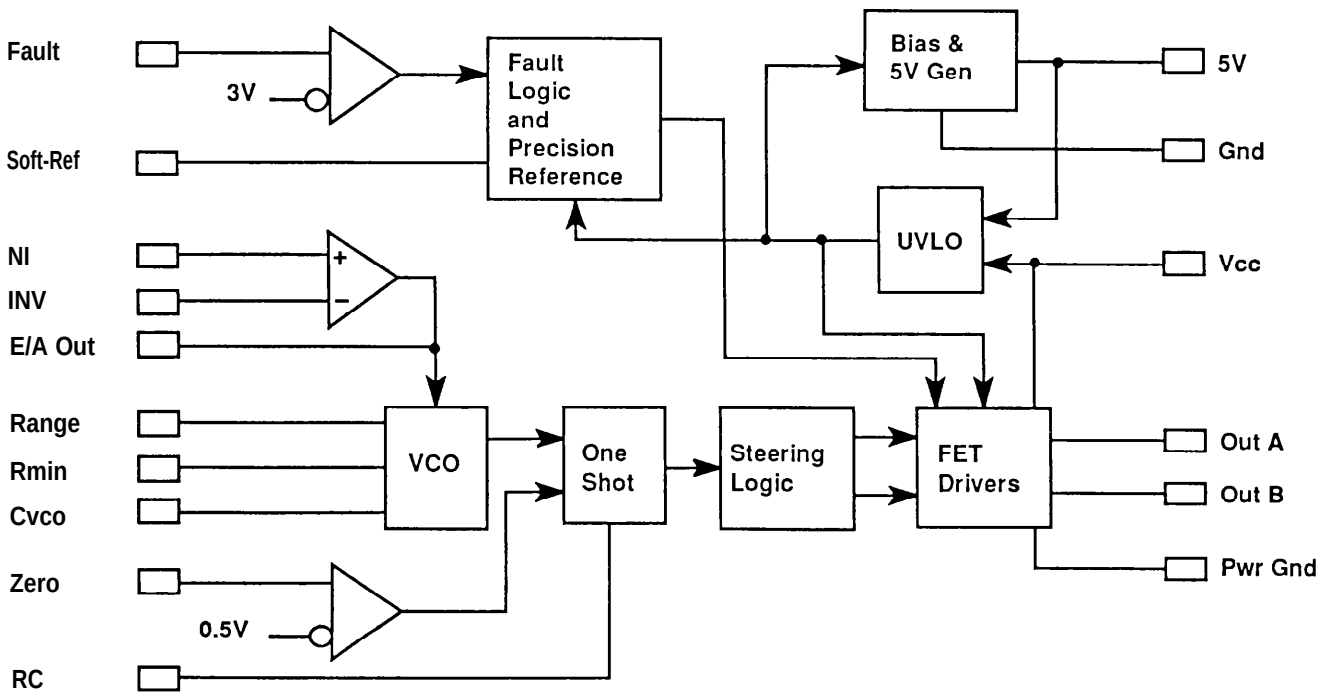

Figure 1. Controller Block Diagram

NEW FAMILY OF RESONANT MODE CONTROL INTEGRATED CIRCUITS

As the discipline is maturing, the advantage of some feature changes has become apparent. Versatility to control both ZCS and zero-voltage-switched (ZVS) converters is needcd. The ability to control proper switch times (on or off) with changing line, load, or component values is needed. To address these needs, a family of controllers based on a common silicon die has been developed. Three members of the family, the UC1861, UC1864, and UC1865 will be covered in detail.

The common block diagram of the family is illustrated in figure 1. These parts feature an error amplifier (E/A), voltage controlled oscillator (VCO), one shot timing generator with a zero wave-crossing detection comparator, steering logic to two output drivers, a 5V bias generator, and under voltage lockout (UVLO). A latched fault management scheme provides soft start, restart delay, and a precision reference.

Die options can be produced that give different UVLO levels, as well as different output properties. There arc two UVLO options. The first, suited for off-1ine operation has thresholds of 16 and 10V. While UVLO is active, Icc is less than 0.3mA. The other option is 8 and 7V, to accommodate lower input voltage DC/DC converters.

The flavor of the outputs required by different resonant mode topologies requires the steering logic to be configured specially for each application. The basic options that can be built allow for single or dual switch drive, and controlled on or off times. Zero-current-switching applications require controlled switch on times while zero-voltage-switching applications require controlled switch off times. Figure 2 shows these options.

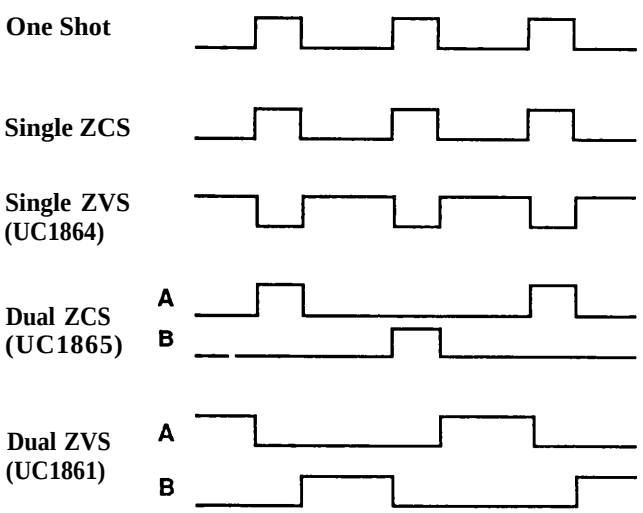

Figure 2. Output Drive For Different Converters

Table 2 details the options implemented in the 1861, ‘64, and ‘65. Other options can be built from the same die.

Table 2. Implemented Options in the 1861, ‘64, ‘65.

Device	UVLO Vth	Outputs	Zero-(?)-Switching
UC1861	16/10V	Dual	Voltage
UC1864	8/7V	Single	Voltage
UC1865	16/10V	Dual	Current

PRIMARY CONTROL BLOCKS

The fundamental control blocks essential for a majority of resonant mode converters arc an error amplifier. VCO, one shot timing generator, and output stage to drive power mosfets.

ERROR AMP & VOLTAGE CONTROLLED OSCILLATOR

Figure 3 details the E/A and VCO. The E/A output directly controls the VCO via the Irange generator. The VCO has inputs for two resistors, R_{ange} and R_{min} and one capacitor, C_{vco}. R_{min} and C_{vco} determine minimum frequency.

$$F_{min} = \frac{3.6}{(R_{min} * C_{vco})} \quad (1)$$

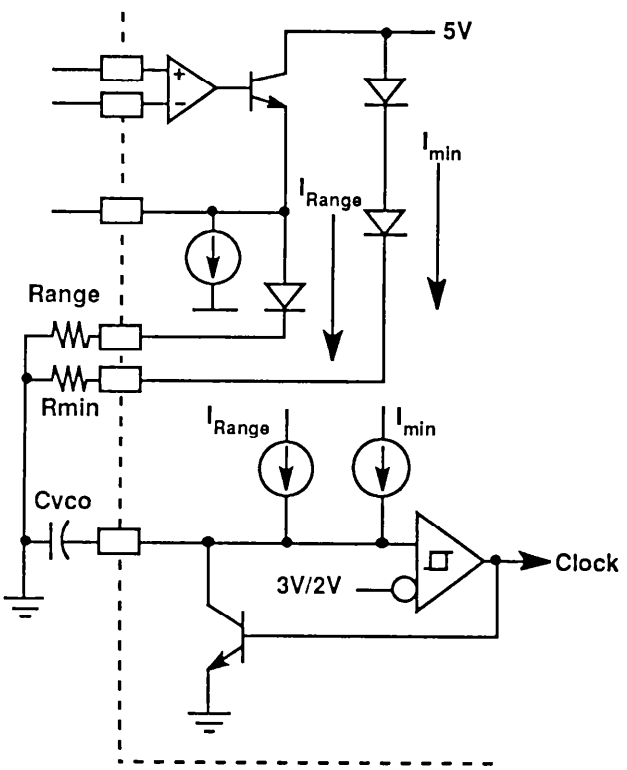

Figure 3. Error Amplifier and Voltage Controlled Oscillator

When the output of the E/A is less than or equal to one diode drop above ground, the VCO operates at minimum frequency. The E/A output can go as high as one diode drop below 5V. When at this potential, the VCO frequency is at its maximum.

$$F_{max} = \frac{3.6}{(R_{ange} \| R_{min}) * C_{vco}} \quad (2)$$

Usable maximum frequency tops out around l.5MHz. The Frequency range is the difference in equations 2 and 1.

$$\Delta F = \frac{3.6}{R_{ange} * C_{vco}} \quad (3)$$

Since the nominal E/A output swing is approximately 3.6V for full variation in VCO frequency, the gain of the VCO block is

$$dF/dV = \frac{1}{R_{ange} * C_{vco}} \quad (4)$$

In ZCS power supplies, an increase in frequency will corrcspond to an increase in the converter's output voltage. For these applications the E/A non-inverting input is connected to a reference voltage while the output voltage sense is fed back to the inverting input. For ZVS power supplies, a decrease in frequency corresponds to an increase in output voltage. For these systems, the input to the E/A are exchanged.

The common mode range of the E/A is from zero to 6V. This feature allows zero volts to be a valid reference voltage applied to the E/A. Soft start, covered later. takes advantage of this feature.

ONE SHOT TIMING REQUIREMENTS

The basic premise in resonant mode conversion is packets of energy delivered at varying repetition rates. Each energy packet dictates a basic switch on or off time, hence the one shot timer. In ZCS systems the switch is on. In ZVS systems the switch is off. The timer, then, should force the switch to conform to the resonant timing of the tank circuit. It is this conformance that achieves zero stress switching.

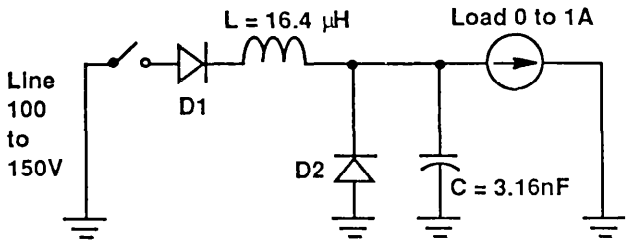

Figure 4. ZCS Resonant Tank Example

For purposes of convenience, a simplified ZCS resonant tank is presented to illustrate the timing requirements of resonant converters in general. This is an example, not a rigorous theoretical presentation. It does, however, demonstratc the problems to overcome in properly controlling a resonant mode converter. The circuit of figure 4 is designed to operate from line input of 100 to 150V and 0 to 1A load current. The tank frequency is arbitrarily selected to be 700kHz. A reasonable first guess for tank impedance is determined by

$$Z_o = \frac{V_{lowline}}{I_{max} * 1.386} \quad (5)$$

$$= 72 \text{ ohms.}$$

From the equations governing resonant tank natural frequency and impedance, L and C can be calculated.

$$F_o = \frac{1}{2\pi\sqrt{LC}} = 700\text{kHz} \quad (6)$$

$$Z_o = \sqrt{\frac{L}{C}} = 72 \text{ ohms} \quad (7)$$

$$L = \frac{Z_o}{2\pi F_o} = 16.4\ \mu\text{H} \quad (8)$$

$$C = \frac{1}{2\pi Z_o F_o} = 3.16\text{nF} \quad (9)$$

Figure 5 shows the pertinent current and voltage waveforms for the case of 125V input and 0.8A output. When the switch closes at zero time, the current starts to build linearly. Once the current reaches 0.8A, then load current is completely supplied through the inductor and D2 carries no current. At this point in time the L and C resonate together until inductor current returns to zero. At this time the switch is allowed to turn off, but it doesn't necessarily have to. D1 prevents reverse current in the switch. It isn't necessary to open the switch until the capacitor voltage decays to line voltage. It is acceptablc to open the switch any time during this "switch window". If it is opened too soon, the circuit will suffer severe switching losses. If it is not opened, the tank will resume resonating, as shown by the dashed curves. If the switch is opened later than the switch window, not only will the circuit suffer switching losses, but the transfer function becomes overly complex.

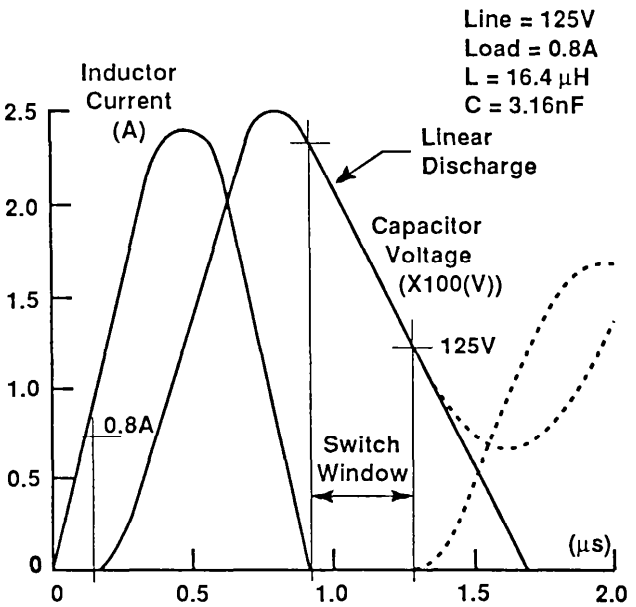

Figure 5. Typical Resonant Tank Waveforms

The graph in figure 6 plots the switch window as a function of load current for both high and low line voltage. For example, at a load current of 0.5A and high line, the switch must be closed for at least 0.80us and need not be opened until 1.61us. Examination reveals the most stringent switch window, 1.03 to 1.21us, occurs at low line and full load. Furthermore, this window is a subset of all other windows. This might lead to choosing a fixed on-time of 1.12us under the assumption that it is relatively easy to build a fixed time one-shot circuit with total variations less than +/-8%. However, further consideration will lead to a different conclusion.

In order to insure that the example in question can be produced, the variations of the resonant components and the possibility of output overload must also be examined. This example continues by assuming total variations for the capacitor are under 10% while under 20% for the inductor. A 20% overload is also allowed.

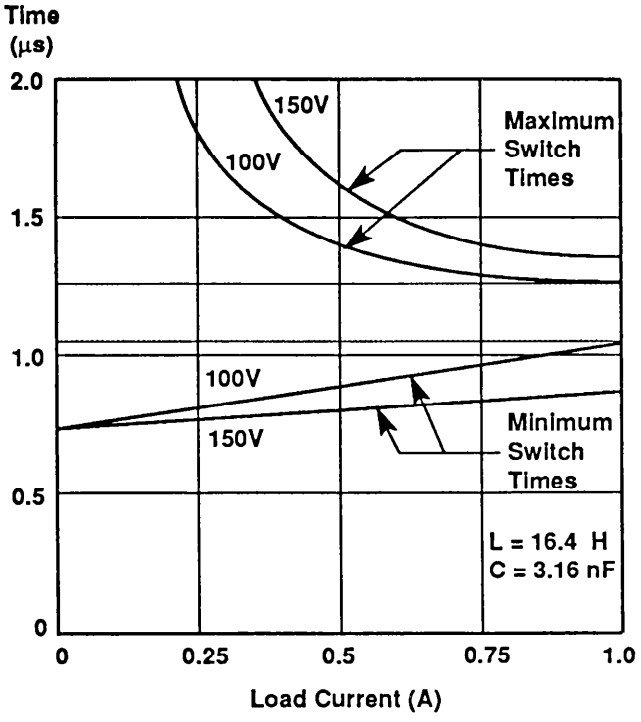

Figure 6. MinimumlMaximum Switch Time vs Load Current

Figure 7 shows the valid switch windows at 1.2A and 100V for nominal component values as well as the four tolerance comers. Several observations can be made. Firstly, the window for the case of +20% inductor and -10% capacitor variations has zero tolerance.

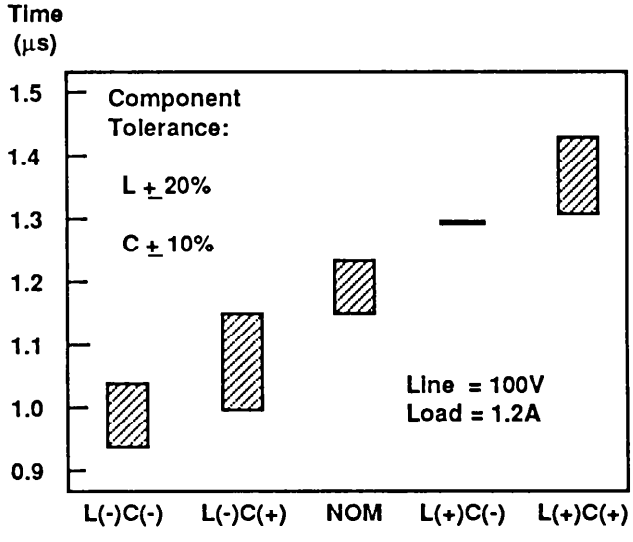

Figure 7. Switch Window vs Component Value

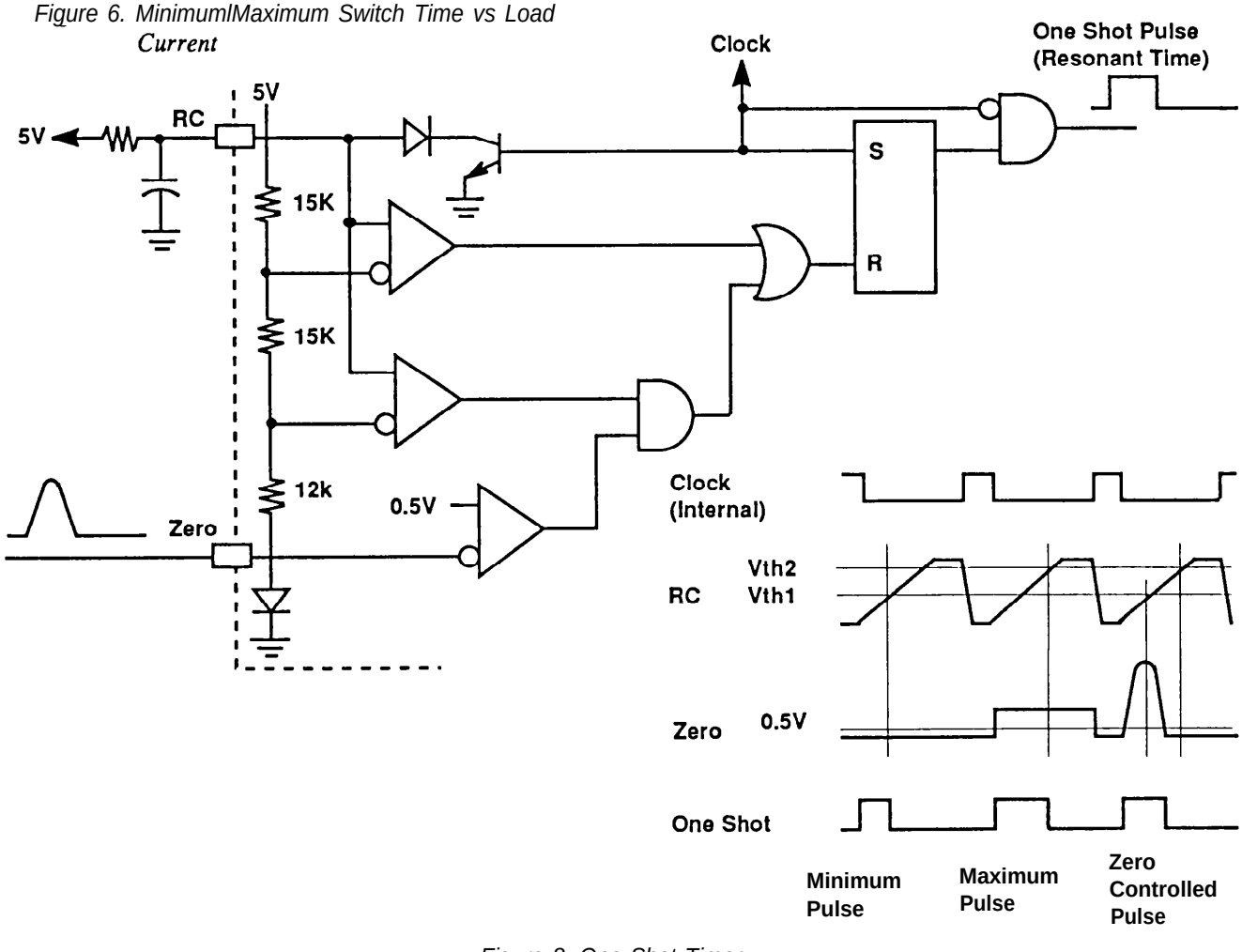

Figure 8. One Shot Timer.

The switch must turn off at 1.30us. This is because the tank impedance is exactly the ratio of low line voltage to overload current for these component values. This is the source of the 1.386 factor in equation 5. Secondly, and the point of the illustration, there is no possible value of fixed switch time that accommodates component variation.

ONE SHOT TIMING GENERATOR

In figure 8, details of the one shot timer arc seen. The clock signal from the VCO sets the latch, blanks the output, and causes the RC timing pin to be discharged. The timing pin determines the minimum and maximum times the one shot output will be high.

$$T_{max} = R * C \quad (10)$$

$$T_{min} = 0.3 * T_{max} \quad (11)$$

Between these two limits, the zero detect comparator will terminate the one shot pulse whenever the Zero pin goes below 0.5V. By sensing the zero crossing of the resonant waveform, the one shot adapts to different resonant component values and varying line/load conditions. The switch time will properly track the resonant tank assuring zero stress switching.

STEERING LOGIC & OUTPUT STAGE

Figures 9, 10, and 11, are block diagrams of the steering logic and output stages. Each output stage is a totem pole driver optimized for driving power mosfet gates. Gate currents of 1A can be obtained from each driver. Note the 1864 single driver is actually both drivers on the chip paralleled. Sample waveforms for the three configurations were shown in figure 2.

Fault and UVLO response of the three configurations is identical. These indications always force both drivers to the low state. During UVLO, the outputs can easily sink 20mA irrespective of Vcc.

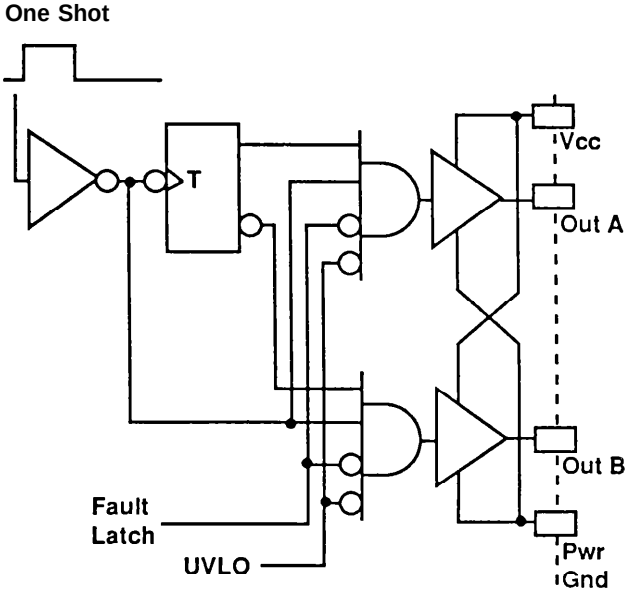

Figure 9. UC1861 Steering Logic

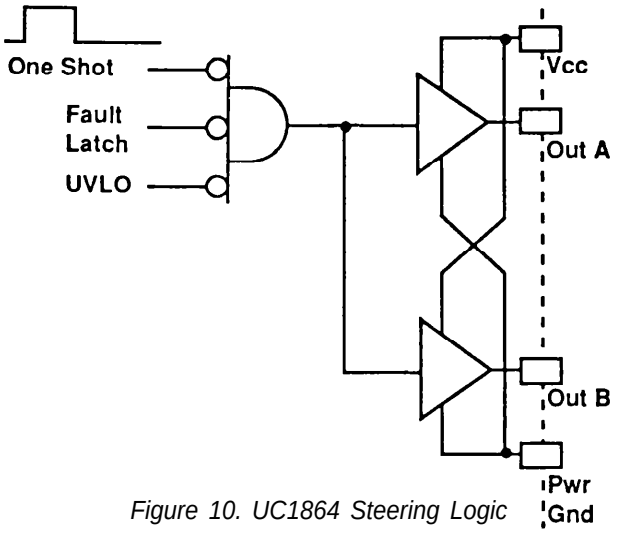

Figure 10. UC1864 Steering Logic

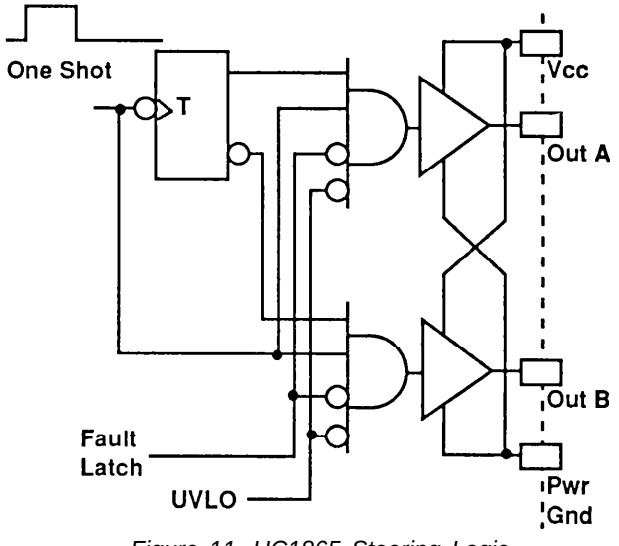

Figure 11. UC1865 Steering Logic

SECONDARY BLOCKS

The secondary blocks on board are UVLO, a 5V bias generator, and fault management with a precision reference. The purpose of the 5V generator is to provide a stable bias environment for internal circuits and up to 10mA of current for external loads. The one shot timing resistor connects to 5V.

UVLO senses both Vcc and 5V. It doesn't allow operation of the chip until both are above preset values. When Vcc is below the UVLO threshold, the 5V generator is off, the outputs are actively pulled low, the fault latch is set, and supply current is less than 300uA.

SOFT START, RESTART DELAY, PRECISION REFERENCE

A novel combination fault management and precision reference is shown in figure 12. One pin is dedicated to a fault sense comparator with a 3V threshold. A second pin does triple duty providing soft start, restart delay, and precision system reference. UVLO initializes the latches. forcing the chip output(s) to be low and the Soft-Ref pin to be discharged. After UVLO, Soft-Ref is charged by an internal 0.5mA current source until is it clamped at

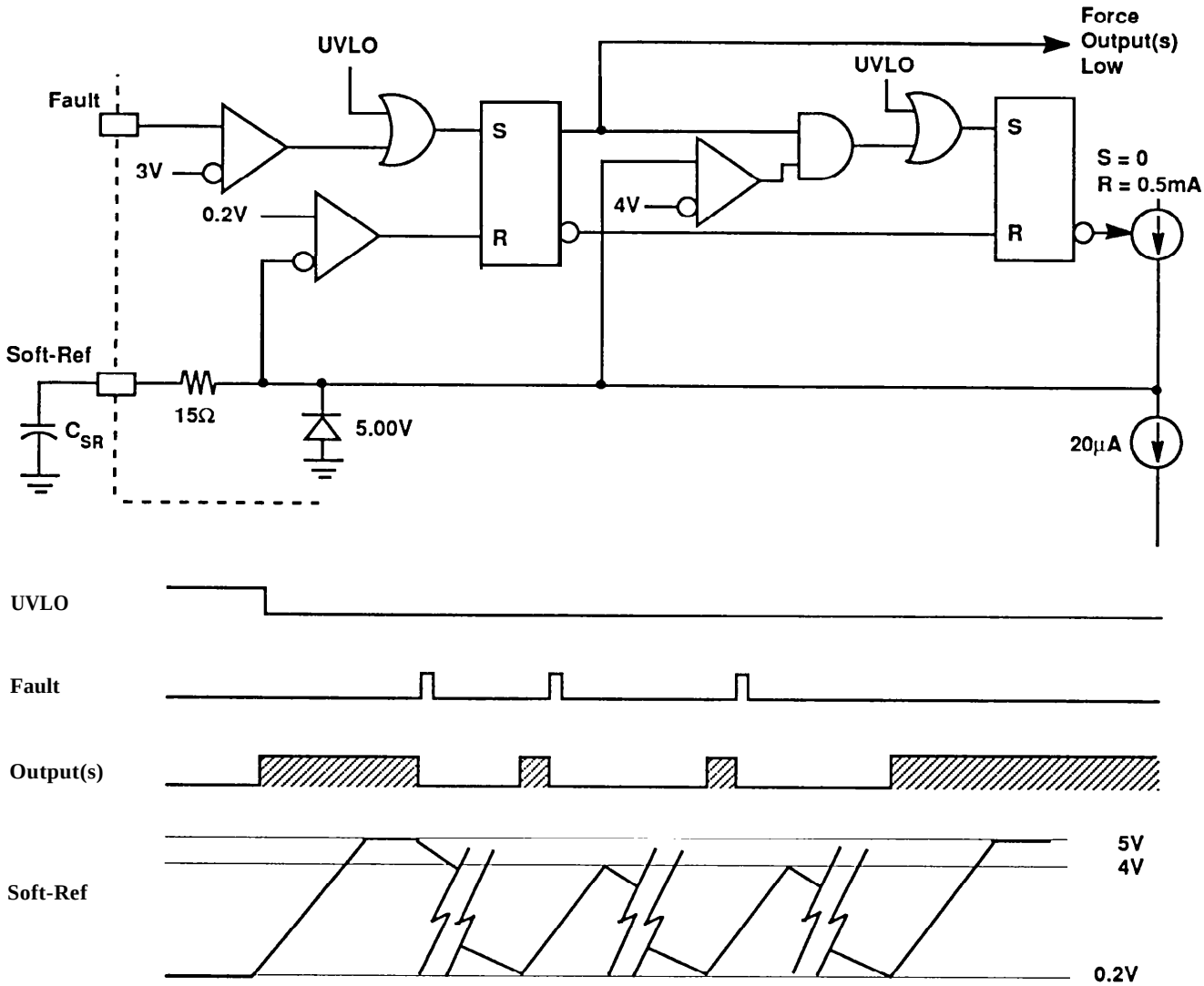

Figure 12. Fault Comparator, Soft Start, Restart Delay And Precision Reference

5V. The soft start time is approximately given by:

$$T_{softstart} = C_{sr} * 10kohms. \quad (12)$$

The recognition of a fault causes the outputs to be driven low and the Soft-Ref pin to be discharged with a 20uA current source. This is the restart delay period. When Soft-Ref reaches 0.2V, the outputs are enabled and the pin is recharged by the 0.5mA current. If a fault should occur before completion of the charge cycle, the outputs are immediately driven low, but the Soft-Ref pin is charged to 4 Volts before the 20uA restart delay current discharges the pin. The restart delay time during continuous fault operation is:

$$T_{restart} = C_{sr} * 190kohms. \quad (13)$$

The ratio of restart delay to soft start is 19:1. If shorter restart delay times are desired, a resistor of 20k or larger can be added from Soft-Ref to ground. The timing equations then become:

$$T_{softstart} = R_{sr} * C_{sr} * \ln\left(\frac{(0.48mA * Rsr) - 0.2}{(0.48mA * Rsr) - 5}\right) \quad (14)$$

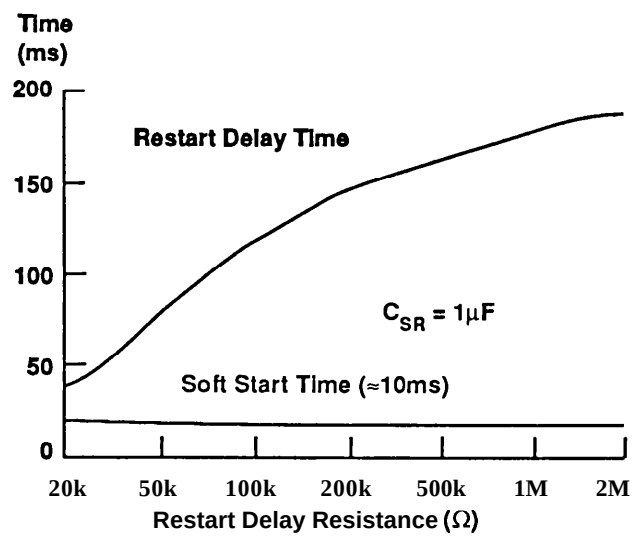

Figure 13. Soft Start And Restart Delay Times

$$T_{restart} = R_{sr} * C_{sr} * \ln\left(\frac{(20uA * Rsr) + 4}{(20uA * Rsr) + 0.2}\right) \quad (15)$$

Soft and restart times are plotted in figure 13 for C_{sr} = 1uF.

The restart feature can be defeated by the addition of a 100k resistor from Soft-Ref to 5V. In this configuration, a fault detection will permanently shut down the converter until either Vcc is recycled and UVLO resets the fault circuit, the 100k resistor is opened or Soft-Ref is externally pulled to ground. The soft start time becomes:

$$T_{softstart} = C_{sr} * 9.2kohm. \quad (16)$$

The Soft-Ref pin is the system reference pin. By ramping the reference from zero during soft start, the converter output will follow the ramp up under closed loop control. This technique allows controlled starts for both ZCS and ZVS systems with no significant overshoot.

The reference characteristic of the Soft-Rcf pin is due to a trimmed 5V zener-type clamp circuit. Fifteen ohms resistance separates the Soft-Ref pin from the clamp to eliminate zener oscillations for any external capacitance value. The clamp zener is designed to tolerate loading of +/- 200uA without degradation of reference accuracy. Loading, however, will alter the soft start and restart delay times, and could even preclude restart delay action unless care is taken in the design.

DC/DC ZVS SINGLE ENDED FORWARD CONVERTER APPLICATION

A ZVS multi-resonant forward converter based on previously reported (ref. 4) work is shown in figure 14. An 1864 is used to control the converter. A 22k resistor from the input line is used to start the circuit, which boot-straps power from the output to the chip after start-up. Before start-up, the chip draws less than 300uA and starts operating when Vcc rcachcs 8V. After start-up, the 22k resistor dissipates 70mW.

The switch voltage V_s is sampled with a l00k/5.1k divider network. The chip anticipates zero crossing when V_s = 10V. In this power converter, switch voltages of 200 to 300V are to be expected. A pnp is used to clamp the zero voltage, Vz to prevent damage to the chip. The 100k resistor represents an insignificant load to the resonant circuit.

The paralleled outputs are connected, as good practice dictates, to the mosfct gate with a small-valued resistor. A schottky diode parallels the output pins to protect the chip from negative voltage spikes that might result from parasitic ringing in the gate circuit.

This power stage was demonstrated to have excellent short circuit tolerance when the minimum switching frequency is well controlled. For this reason, the fault input is not used.

Sensed output voltage is scaled & presented to the non-inverting pin of the E/A. The inverting input is DC referenced to the Soft-Ref

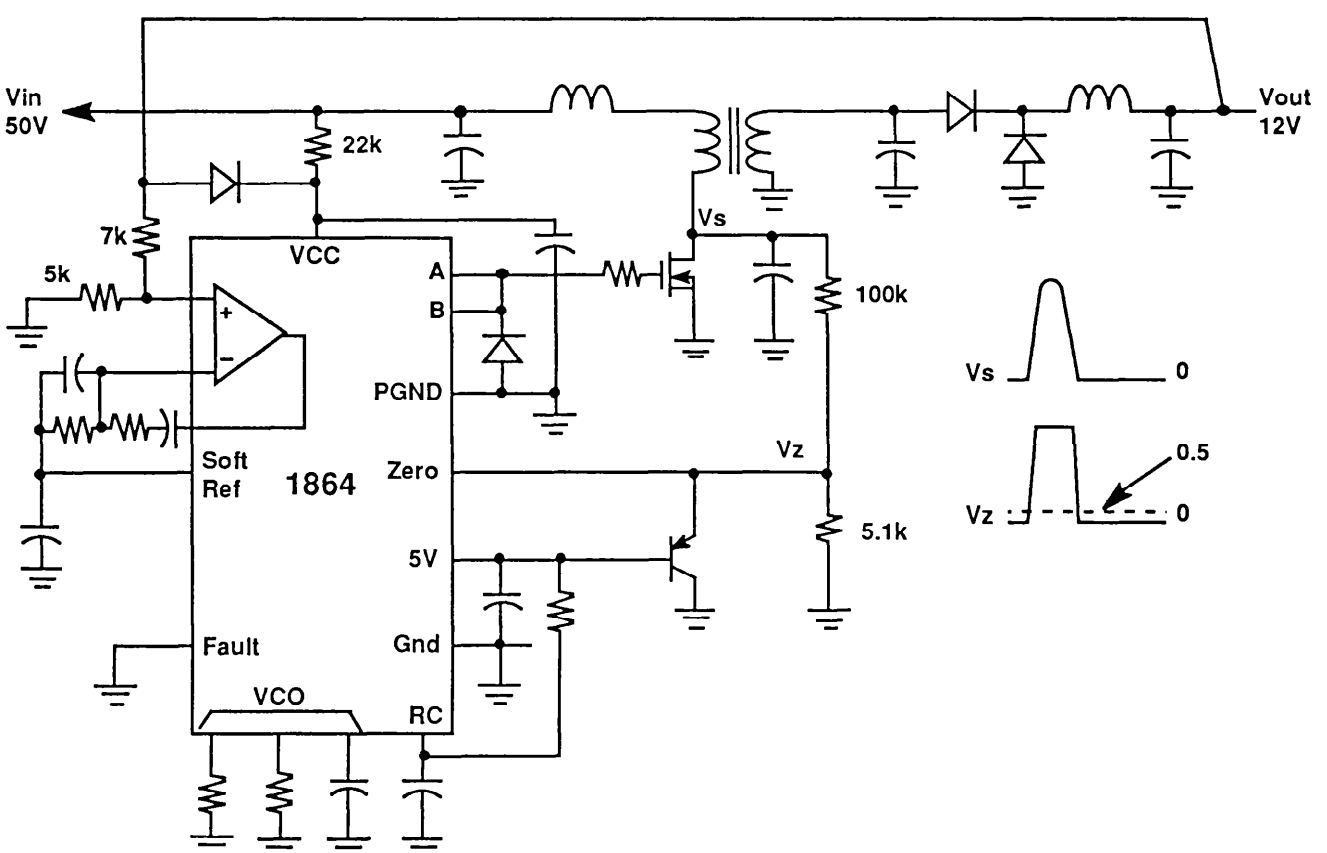

Figure 14. ZVS-MR Forward Converter Controlled By UC1864.

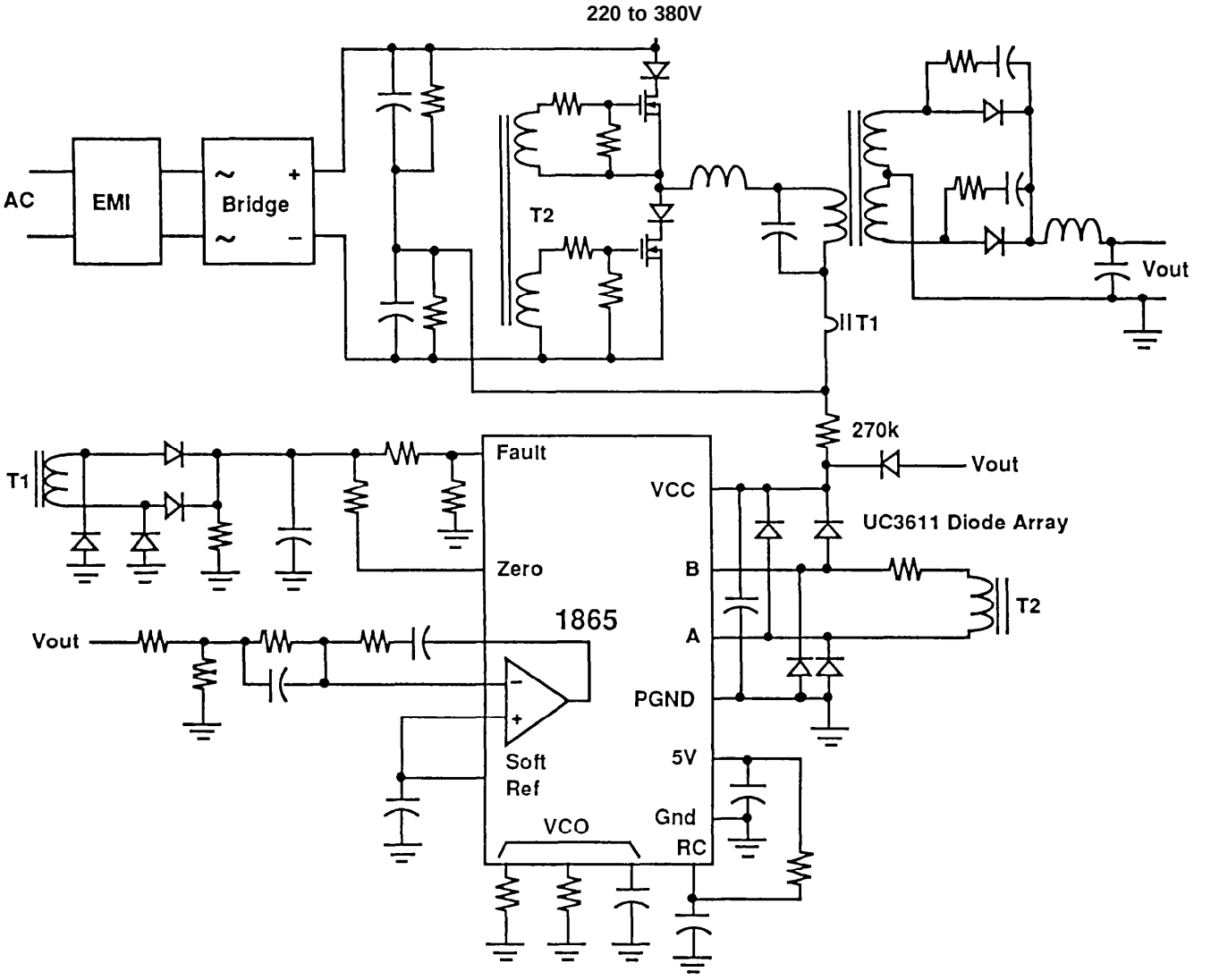

Figure 15. ZCS Off-Line Half-Bridge Converter With UC1865

pin, 5V. The compensation network shown represents zero DC load to the Soft-Ref pin. As long as C_{sr} is much larger than the feedback capacitor, then soft start behavior will be essentially as described in equation 12.

OFF-LINE ZCS HALF-BRIDGE CONVERTER APPLICATION

AZCS off-line half-bridge converter (ref. 1) with an 1865 control IC is shown in figure 15. Irrelevant details in the converter have been simplified. The wide UVLO hysteresis and low start current of the chip have been used in start-up. A single resistor from the high voltage bus is used to start the circuit which then sustains itself from output voltage.

This circuit samples resonant current with transformer T1. Rectified secondary current, converted to an analog voltage, is applied to the fault and zero inputs of the 1865. Excessive current in the resonant tank will effect a shutdown and restart. The resistor between current sense transformer and the zero pin is to limit

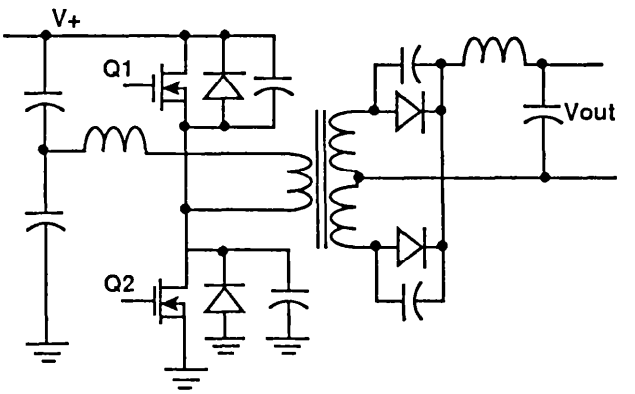

Figure 16. ZVS Half-Bridge Converter

current when the signal is at a high value. The allowable voltage range at the zero pin is zero to 9V, and resistive current limiting to less than 1mA is sufficient.

The half bridge power mosfets arc transformer driven from the differentially connected output drivers of the 1865. A UC3611 schottky diode array has been used to prevent the outputs from being forced too far above Vcc or below ground.

The E/A non-inverting input is directly connected to the Soft-Rcf pin to take advantage of all three features of the pin. This emphasizes the simplicity of application of the 1865 to this converter.

OFF-LINE ZVS HALF-BRIDGE CONVERTER APPLICATION

An off-line ZVS half-bridge converter (ref. 3) is shown in figure 16. An 1861 controls this converter in much the same manner as the two previous examples and is not shown here. The error amp configuration matches the ZVS example while the output stage is configured like the ZCS example.

This application does, however, present a difficulty in sensing zero voltage to control the one shot. In the first ZVS example, the voltage waveform was ground referenced and unipolar. The ZCS cxample had bipolar current, but a transformer and diode bridge conditioned the signal for the chip. In this example, zero switch voltage needs to be sensed for both Q1 and Q2. This poses no real problem for Q2. Q1 is another story. Some form of external circuitry must be employed to sense Q1 and translate the information to the ground referenced chip.

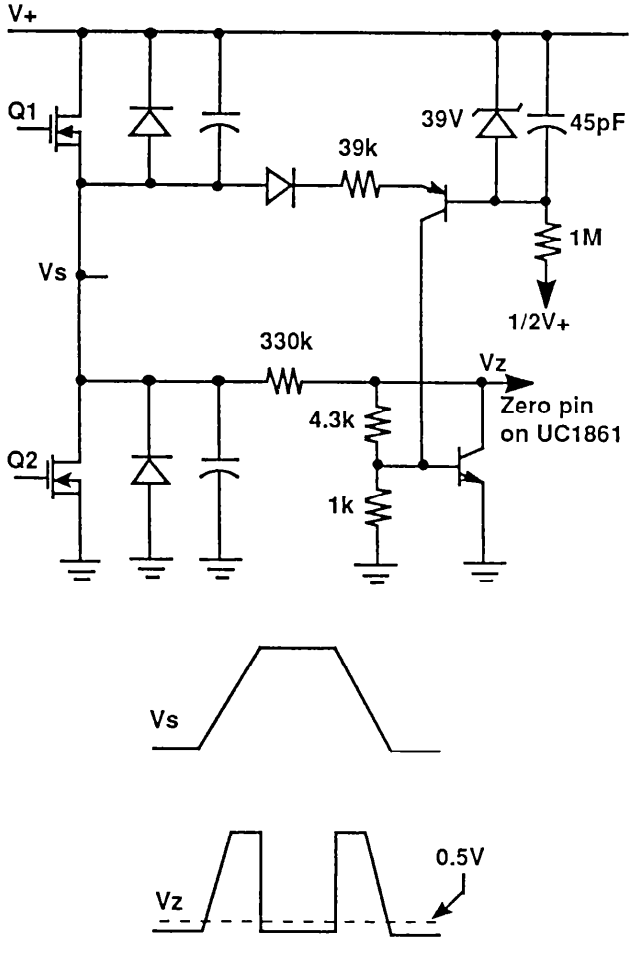

Figure 17. Zero Voltage Sensing Scheme For ZVS Half-Bridge Converter

An easily implemented high voltage comparator circuit is shown in figure 17. The pnp and diode are the only high voltage components used. The circuit dissipates only 300mW. The output of this circuit is applied directly to the zero input of the 1861.

CONCLUSION

A new family of integrated circuits to control resonant mode converters has been introduced that provides several improved features over those previously available. This family has parts that are suited not only to zero-current-switching, but also to zero-voltage-switching converters. The 1861, 1863. and 1865 are suited to off-line ZVS, DC/DC single ended ZVS, and off-line ZCS systems. Controllers for other specific converters can be built from this family. Adaptive control for resonant tank component variations as well as varying line and load conditions is inherent in the chip due to its zero crossing detect circuitry. A unique one pin approach to soft start, restart delay, and system reference provides adjustable restart delay to soft start time ratios as well as closed loop control during soft starts. Relative ease of application to three previously reported converters was discussed.

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