

## UCC3806 BiCMOS CURRENT MODE CONTROL IC

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### Abstract

*Space and cost constraints have forced power supply designs into smaller spaces and demanded more efficient designs with higher switching frequencies. With the introduction of the UCC3806 BiCMOS current mode controller, a designer has the advantages of reduced current consumption, power loss and propagation delays within the IC. The UCC3806 is pin-for-pin compatible with the popular UC3846 and UC3856 controllers. With minimal part changes, this device may be suitable for retrofit into many existing designs where higher power consumption and propagation delays posed problems in the past. An ideal application for the UCC3806 is in battery operated equipment where low power consumption is critical to extended operation.*

### INTRODUCTION

As power supply requirements are demanding higher switching frequencies and lower power consumption, bipolar PWM IC's may limit design flexibility. The versatile UC3846 consumes relatively low power but is slow by today's standards. The UC3856 fulfills the high speed requirements but uses significantly more power to accomplish the task. Unitrode's BiCMOS process produces fast, low power BiCMOS control ICs with the high power capabilities of bipolar devices, a prime example being the UCC3806.

The UCC3806 features slew rate limiting of the current sense amplifier input voltage. This allows direct injection of the primary current sense signal without the need to filter the inductive leading edge spike. The propagation delay from current sense to output is reduced to 125ns and rise and fall times of the gate drive outputs are only 65ns. Gate drive current remains high at  $\pm 500\text{mA}$  from the dual totem pole MOSFET drivers. The low undervoltage lockout thresholds make this IC ideal for many battery and automotive applications. Most features will be familiar to the designer acquainted with the UC3846. The one volt pulse by pulse current limiting remains, along with programmable latched or non-latched shutdown modes triggered via the Shutdown pin.

This Application Note highlights retrofit applications of the UCC3806 and provides a step by step process to accomplish this. Several new applications will be introduced with a review of some popular applications. Unitrode Application Note U-93 de-

scribing the UC3846 should be reviewed for background and additional information.

### UCC3806 BiCMOS Current Mode PWM Control IC Features

- 100 $\mu\text{A}$  startup current
- 1.4mA operating current
- Pin-for-pin compatible with UC3846 and UC3856
- Operating frequency to 1MHz
- $\pm 500\text{mA}$  MOSFET output stage
- 65ns output rise and fall times
- 125ns current amp to output delay
- Current Sense Slew Rate Limiting
- Undervoltage Lockout

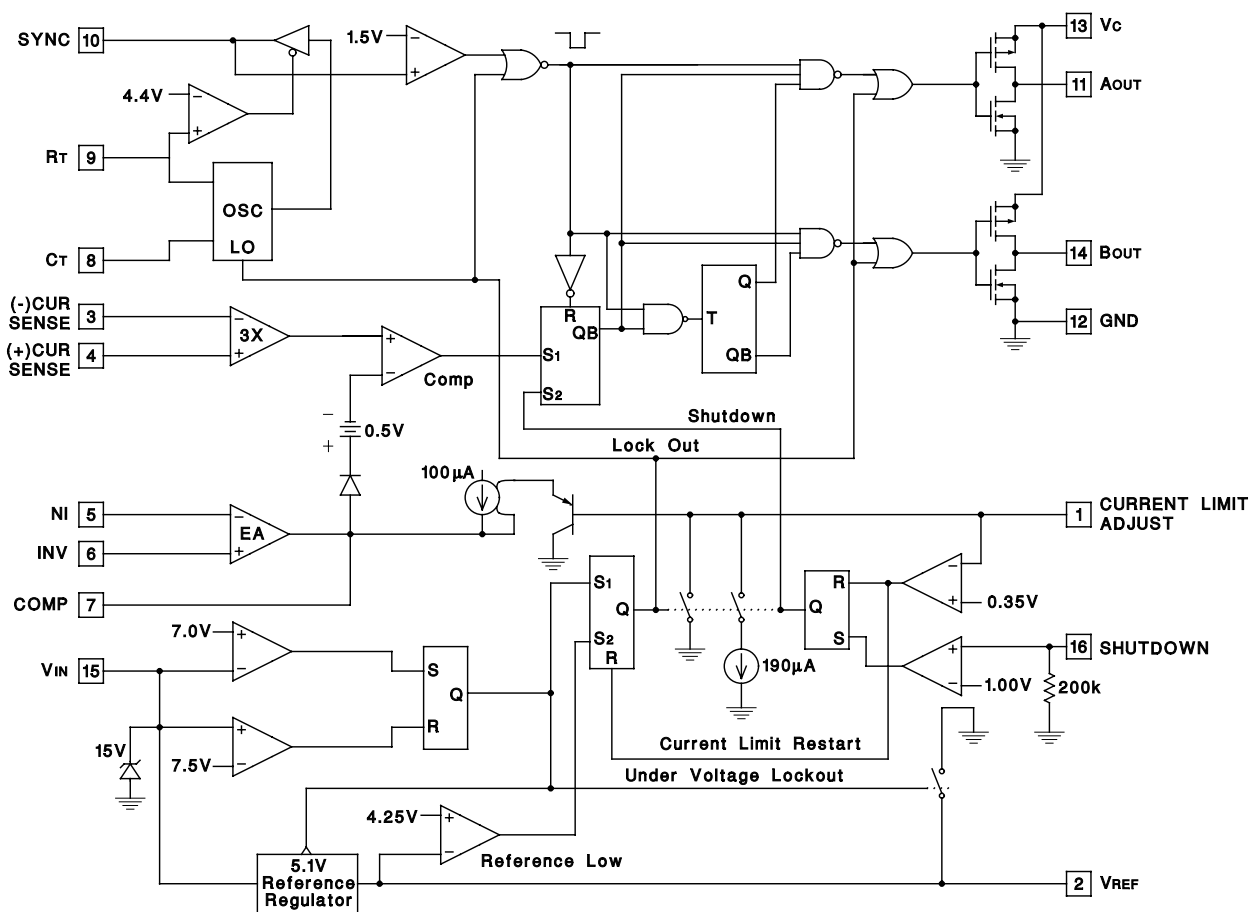
### DEVICE DIFFERENCES

For designers familiar with the UC3846 or UC3856 devices, this section will provide a quick overview of necessary design changes to incorporate the UCC3806.

1) **UVLO:** Three parameters should be observed here. The start up voltage threshold is 8.0V with an operating hysteresis of 0.75V. The absolute maximum voltage for  $V_{\text{IN}}$  (pin 15, IC power) is 15V and for  $V_{\text{C}}$  (pin 13, gate drive voltage), 18V.

2) **DEAD TIME** ( $t_{\text{d}}$ ) is determined by the timing capacitor ( $C_{\text{T}}$ ).

$t_{\text{d}} = 961C_{\text{T}}$  (approximately)



UCC1806 Block Diagram

3) **SWITCHING FREQUENCY** ( $f_s$ ) may be found by using the equation

$$f_s = \frac{1}{2R_T C_T + t_d}$$

4) **SHUTDOWN** threshold voltage on pin 16 has been raised to 1.0V.

5) **GATE DRIVES**: The maximum gate drive current is  $\pm 500\text{mA}$ .

6) **CURRENT LIMIT**: As in the UC3846 and UC3856, R1 and R2 (see Figure 5) program the threshold for primary current limit and determine whether the IC will latch off or retry. When a shutdown signal is generated, a  $190\mu\text{A}$  current source to ground pulls down on pin 1. If the voltage on the current limit adjust pin (pin 1) remains above 350mV the IC will remain latched and power must be cycled to restart. If the voltage on the current limit adjust pin falls below 350mV, then the IC will attempt a re-start.

**DESCRIPTION**

**SUPPLYING POWER**

Power can be applied to the UCC3806 by a single source or by two separate sources, one for the IC

supply and another for the FET drive outputs. In either case, adequate local capacitive bypassing is required. The IC supply voltage is internally limited by a 15 volt shunt regulator circuit. This is advantageous in off-line applications where the IC is powered-up by a resistor to the high voltage input. Shunted supply current in the IC must be limited to 10mA maximum. The IC's ground should be separated from any high current or noisy ground paths, but at the same electrical potential. This is best done by routing a local ground for the UCC3806 circuitry and then connecting this to a single point system ground.

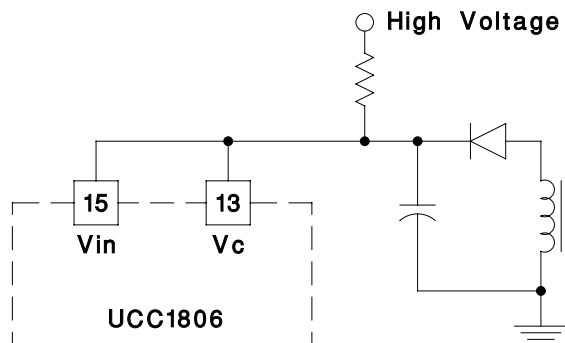


Figure 1. Supplying Power

### UNDER VOLTAGE LOCKOUT (UVLO)

A minimum of 8V is needed to start the UCC3806, and once operational, the IC operates down to 7.25V. Below this level the UCC3806 will turn off and again require at least 8V to re-start. Care must be taken to be sure that the voltage source can supply adequate current to maintain operation or the IC will cross its turn-off undervoltage lockout threshold and shut down. The most obvious symptom where this problem occurs is when the entire power supply pulses on and off. Depending on the storage capacitor size and bias supply circuitry, the supply may eventually continue to run or may simply hiccup. A good design will include a large capacitor across the IC power inputs to store energy long enough to avoid UVLO. Note that the gate drive requirements of most power MOSFETs will usually use more current than the IC draws by itself, and must not be overlooked. Please refer to application note U-93 and U-137 for more details.

### SELF-BIASING, ACTIVE LOW OUTPUTS DURING UNDER VOLTAGE LOCKOUT.

During any undervoltage lockout the UCC3806 outputs are actively held low to eliminate problems caused by a power MOSFET switch device inadvertently turning on. As with other Unitrode PWM IC's, gate drive outputs cannot pull high until the IC has been properly turned on. This self-biasing circuitry derives its power from the MOSFET gate voltage which is attempting to rise. Note that this protection feature is also activated when the supply voltage falls below the UVLO point, causing the IC to turn off.

### REFERENCE VOLTAGE

The UCC3806 provides a  $5.1V \pm 1\%$  reference output. Bypass capacitors with low impedance (ESL and ESR) and good high frequency response should be used. Generally, a ceramic monolithic or MLC capacitor with short leads to the IC ground pin is required even if the reference is not externally used. Note that the maximum current available from the reference pin is 10mA. Erratic operation can be caused by exceeding the maximum current or from connecting very noisy loads to the VREF pin without adequate bypassing and filtering.

### OSCILLATOR

The oscillator timing section of the UCC3806 is similar to its predecessors yet uses different voltage thresholds throughout. Frequency is programmed by selecting the values of two timing components;  $C_T$ , the timing capacitor and  $R_T$ , the timing resistor. Current flowing from the internal 1.25V reference at the  $R_T$  pin divided by the value of  $R_T$  is mirrored to the timing capacitor pin ( $C_T$ ).

This causes a linear charging of  $C_T$  from 0V to 2.5V, the lower and upper oscillator thresholds. Note that the current mirror is limited to a maximum of  $100\mu A$  so  $R_T$  must be greater than 12.5k.

Oscillator discharge is facilitated by switching on a 2.6mA current sink from  $C_T$  to ground. This causes a linear discharge of  $C_T$  to zero and then initiates the next switching cycle. Dead time occurs during the discharge time of the capacitor during which time both outputs are active low. Subjecting other IC pins to excessive noise or pulling some points below ground may reset the oscillator or cause periodic termination.  $f_s$  and  $t_d$  may be approximated by:

$$f_s = \frac{1}{2R_T C_T + t_d} \quad t_d = 961 C_T$$

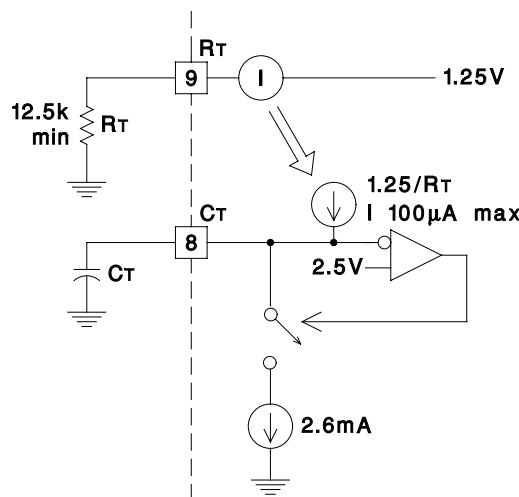


Figure 2. Frequency and Deadtime Programming

### SYNCHRONIZATION

The SYNC pin allows external synchronization of the UCC3806 to an outside control signal with TTL compatible thresholds. The oscillator  $C_T$  pin must be grounded in order to use the SYNC input feature. The internal clock is reset and a deadtime generated by applying a voltage greater than 2V (high) to the SYNC pin. Returning this input to a voltage less than 0.8V toggles the output flip-flop and initiates a new switching cycle.

External synchronization may be sourced from the SYNC pin. The oscillator output goes to the SYNC pin and affects the outputs as described above. Another UCC3806 may be connected to the SYNC pin in order to match the frequency of the master device. Other circuits or devices may use the characteristics of the SYNC pin. A high output state is at least 2.4V with 5mA current sourced and low output state 0.4V maximum with a 1mA sink.

**OUTPUT DRIVER SECTION**

The two UCC3806 alternating outputs consist of totem-pole MOSFET pairs. Duty cycle may be varied from 0 to 98% where minimum dead time is determined by the timing capacitor value. Both outputs use MOS transistor switches with inherent anti parallel body diodes to clamp voltage swings to the supply rails. This may allow operation without the use of clamp Schottky diodes on each gate drive as recommended with all bipolar ICs. Drive currents of  $\pm 500\text{mA}$  peak with rise and fall times of 65ns are typical performance specifications.

**CURRENT AMPLIFIER SECTION**

Slew rate limiting on the current sense amplifier output is featured in the UCC3806 device. This allows direct connection to the current sense resistor or current transformer with minimal filtering. Parasitic leading edge inductive spikes can cause false triggering in most PWM IC's and thus require significant filtering.

As with other current mode PWM's, the UCC3806 can be configured for a variety of control techniques. The more common examples are peak current mode control, direct duty cycle control (voltage mode), and gaining popularity is average current mode control. Slope compensation can be added by dividing down the oscillator sawtooth waveform and summing a portion of it to the peak switch current signal.

High efficiency current sensing can be obtained by developing a small amplitude current sense signal, well below the 1 volt maximum of the IC. A DC pedestal can be added to raise the current signal, gaining noise immunity. One easy method of achieving this is to add resistors from output A and output B to the positive current sense input in a system where the negative current sense pin is grounded. Note that this pedestal will vary with changes in the IC collector supply voltage,  $V_c$ . Another method to add a DC level to the current

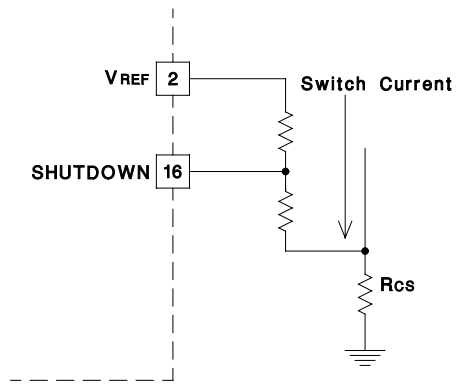


Figure 3B. Level Shifted Shutdown

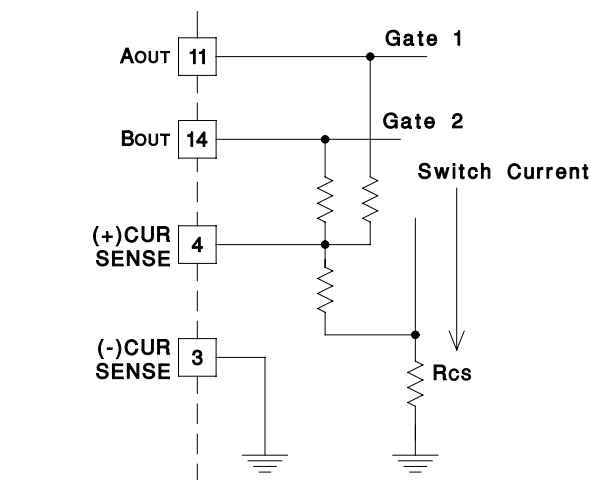


Figure 3C. Adding a Pedestal from Gate Drives

sense input or the current limit input is to use a resistive divider from  $V_{REF}$ .

**PROTECTION CIRCUITRY**

By adjusting the pulse-by-pulse current limiting, a converter can be protected against short circuit conditions. The UCC3806 terminates the PWM output protecting the switching device and other power components when sensed switch current reaches the 1 volt current limit threshold. The ratio of this signal to actual switch current is determined by the current sense resistor value. Additionally, the

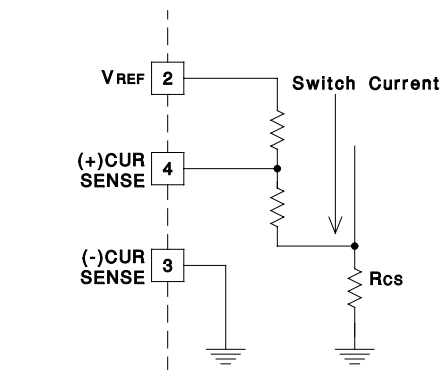


Figure 3A. Level Shifted Current Sense

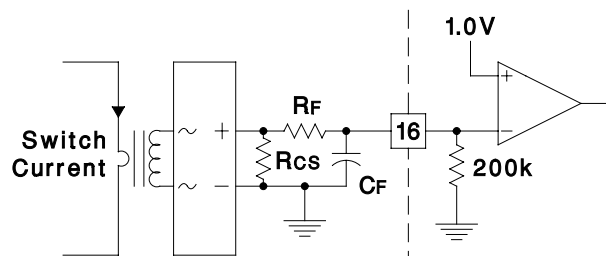


Figure 4. Overcurrent Shutdown

SHUTDOWN feature can be incorporated for further protection as shown in Figure 4.

The pulse-by-pulse current sense amplifier allows differential voltage sensing for ungrounded sense resistors. The current amplifier will terminate the ON-time when it's differential voltage reaches that set at the current limit input. Pulse by pulse current limiting is programmed by two resistors at the current limit. These resistors also set the shutdown mode to either latching or non-latching shutdown. To choose Values of R1 and R2:

$$V_{CS} = (V_{pin1} - 0.5)/3$$

$$I_{CL} = \left( \left( \frac{R_2 \cdot V_{REF}}{R_1 + R_2} \right) - 0.5 \right) / 3R_s$$

During Shutdown:

$$V_{pin1} = \frac{V_{REF} - 190(10^{-6})R_1}{1 + \frac{R_1}{R_2}}$$

Latch Mode:  $V_{pin1} > 350mV$   
 Non-Latch Mode:  $V_{pin1} < 350mV$

A SHUTDOWN pin is provided for enhanced protection. Pin 16 can be programmed to force a shutdown when it's voltage exceeds 1V, and latching or non-latching modes are programmable options. When a shutdown is triggered, a 190µA current sink is connected to the current limit pin. If the voltage on pin 1 remains above 350mV, then the IC remains latched and outputs are held actively low. If the voltage is allowed to fall below 350mV, then the IC will reset and initiate a re-start. Of course, a wider margin is recommended to guarantee that resistor tolerances and external noise do not affect this mode selection. Again, a bypass capacitor from pin 1 to ground can also help eliminate problems from external noise.

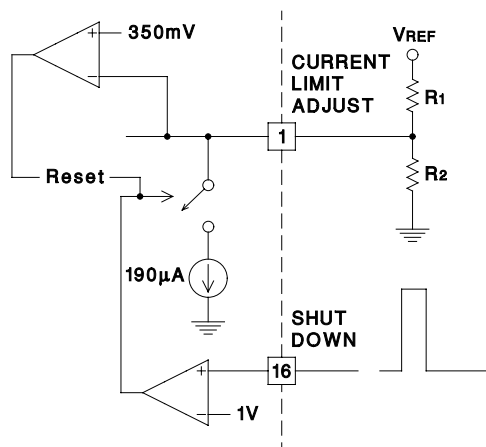


Figure 5. Shutdown Mode Programming

**SOFT START**

Several methods of soft starting of a converter are possible with the UCC3806, and two common examples are shown. In the first example, an R/C network isolated by a PNP transistor sinks current from the output of the error amplifier. In the second, an R/C network alone is used on the error amplifier non-inverting (E/A+) input. This ramps up the non-inverting input of the op-amp to reduce the slew of output voltages and delivers true closed loop controlled start-up. In both cases, the diode provides automatic capacitor discharge when the VREF turns off, typical of a power-up or shutdown condition.

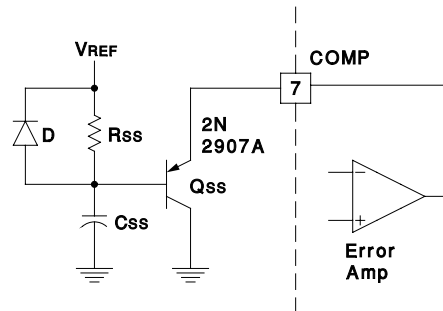


Figure 6. Buffered Soft Start

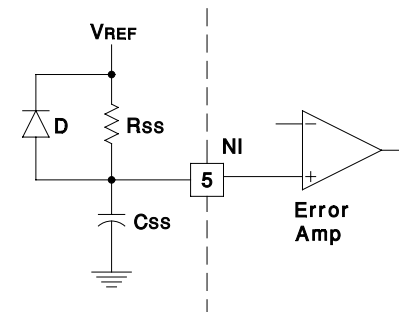


Figure 7. Closed Loop Soft Start

**APPLICATIONS**

**Push-Pull Converter**

One of the most common uses for the UCC3806 is in an isolated Push-Pull configuration utilizing current mode control. A summation of the components and their functions follows.

Resistors Rg1 and Rg2 limit the output current to 0.5A. Rv limits current to the IC to 10mA. RT and CT set frequency and dead time. Note that oscillator waveforms may become non-linear at higher frequencies and so RT and CT should be selected to obtain the desired frequency. Rss and Css are used to ramp up the reference on the error amp so the output voltage comes up in an orderly manner. R1 and R2 program the pulse by pulse current limit for primary peak current. R3 and R4 set a shutdown triggered by excessive primary current. These levels should be set to assure that a shut-

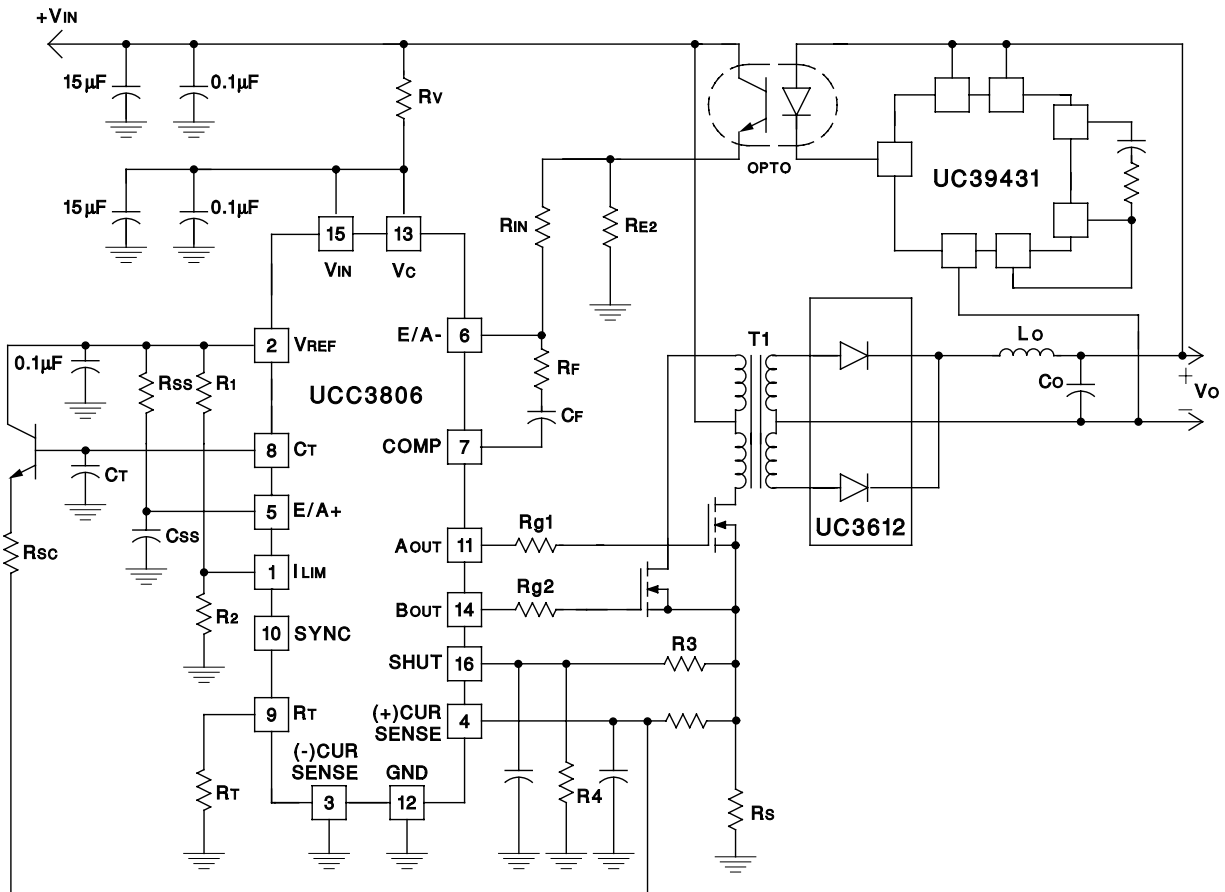


Figure 8

down will be triggered before the pulse by pulse current limit threshold is reached. R1 and R2 determine latched or non-latched shutdown once shutdown is tripped. Slope compensation is shown and may be necessary in order to avoid sub-harmonic oscillations when duty cycles greater than 50% occur. Note that bypass capacitors are used in several locations to filter noise around the UCC3806 circuitry. The value of these capacitors will vary depending on input and output variables, layout, and power level.

**Non-Isolated Autotransformer Converter**

When isolation is not needed but a voltage step up desired, a simple push-pull configuration may be used with a non-isolated transformer to step up the input to output voltage. Figure 9 shows how a UCC3806 may be used to achieve a very efficient converter ideal for battery applications. Because of the voltage step up, output regulation is maintained even when input voltage falls below output voltage. Notice that the UCC3806 is otherwise used in a very conventional application here. Circuit set up follows the same simple rules as a conventional transformer isolated converter. Efficiencies over 90% can be realized for low power converters similar to this example.

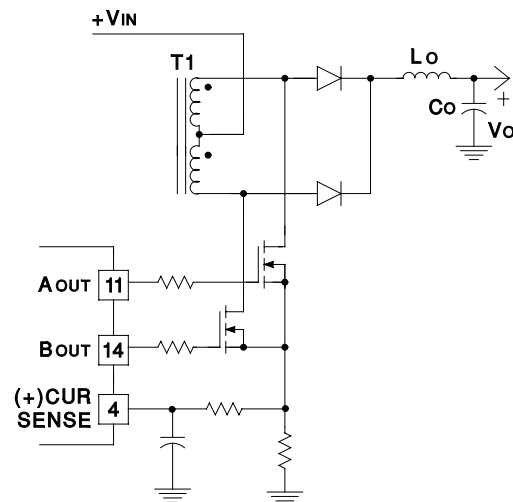


Figure 9. Autotransformer Converter

**Self Contained Low Power Converter**

A non-isolated converter of Figure 10 demonstrates the versatility of the UCC3806 FET output stage. In this application, the lower drive FET of each output totem pole is used as a synchronous rectifier along with the parasitic body diode, and no external diodes or switches are used. Interleaved inductors are incorporated and operated in the continuous current mode. Inductor current must not

become discontinuous, or current will reverse direction and circulate into the IC. When this occurs, the other inductor circulates current into the lower output FET creating excessive heating and forcing the IC to overcome backwards current when turn-

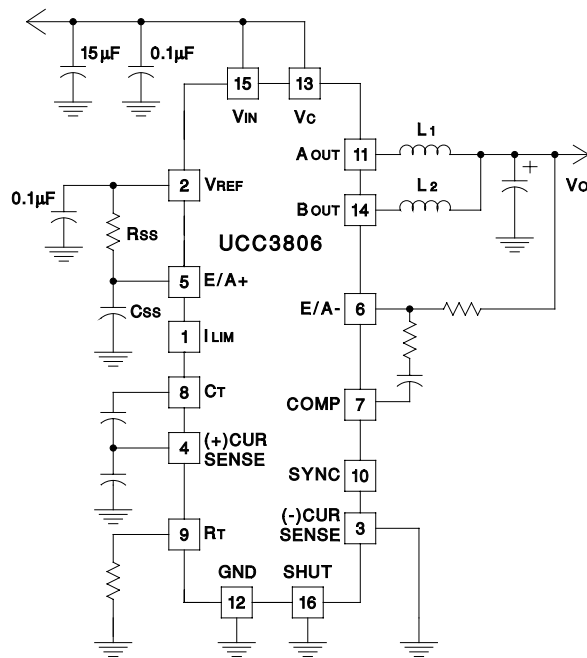


Figure 10

ing on again.

### Summary

BiCMOS technology in the UCC3806 has added a new dimension to PWM IC's available today. This IC enables the designer to optimize circuits by allowing higher switch frequencies and decreasing IC delays. This breakthrough in technology brings a dramatic reduction in IC operating current and the ability to use larger resistor values in support cir-

cuitry which further cuts power loss. Less parts can be used by eliminating Schottky diodes which protect Bipolar IC's as well as the possible elimination of current sense filtering. The UCC3806 remains pin for pin compatible with the familiar UC3846 and possesses all of the desirable functions found in that popular PWM control IC. These features include a 500mA output drive capability, current mode control, fully differential current sense amplifier, pulse by pulse current limiting under voltage lock out and built in shutdown circuitry.

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