ELEGANTLY SIMPLE OFF-LINE BIAS SUPPLY FOR VERY LOW POWER APPLICATIONS

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INTRODUCTION

Generating a low power, low voltage bias supply in an off-line application may not seem like a major design challenge – at first glance. However, obtaining an efficient, cost effective and compact 1 Watt supply can be a frustrating ordeal as the various approaches are evaluated. A simple transformerless technique, like the Buck regulator, requires a rather complex high side switch which can be difficult to drive. Narrow duty cycles are another inescapable problem with a significant step down in input to output voltage.

The Flyback converter can provide a relatively simple solution for this low power application, but it requires more costly coupled windings instead of a single inductor to perform the voltage conversion. Other topologies too, have their own unique sets of problems. For example, the SEPIC Converter is a viable option, but needs a high voltage blocking capacitor and two inductors, in addition to the high voltage switch. It will also require current mode control for stability as opposed to simpler control techniques. Charge pump circuits are another possibility, but are generally much noisier, deliver poor efficiency and often use a high side switch. This Application Note will present a novel conversion technique to achieve the desired low voltage, low power bias supply while meeting the design goal of low cost with minimal complexity.

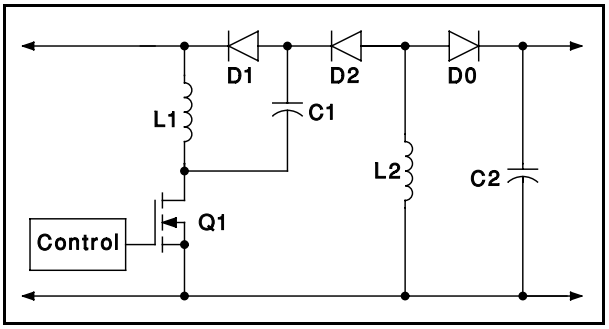

Figure 1. Cascaded Flybacks

Approach : The basic converter shown in Figure 1 is a cascaded Flyback Converter operated in the discontinuous current mode. Two flyback stages are placed in a series configuration to complete the voltage transformation. Inductor L1 of the first stage is switched across the input voltage when MOSFET (Q1) turns on. Energy is stored in L1 as its current rises linearly until the switch is turned off. When this occurs, inductor L1 discharges its energy into capacitor C1, and diode D1 is conducting. In steady state operation the switching action develops a net DC voltage across C1, the "output" capacitor of the first Flyback converter, C1.

The inductor of the second stage (L2) is also switched across capacitor C1 while the MOSFET is on. Although the voltage across inductor L2 is negative with respect to ground, energy is stored in L2 as the current linearly rises. When the switch is turned off, inductor L2 discharges to the output capacitor of this second Flyback stage, C2. A regulated DC output voltage is obtained across C2 and controlled by varying the ON-time of switch Q1. Voltage and current waveforms for this converter are shown in Figure 2 for completeness.

This cascaded Flyback converter can be controlled by a number of popular techniques which include Duty Cycle (Voltage Mode) Control or Current Mode Control, and can be operated in either fixed or variable frequency modes. A novel control technique will be introduced to greatly simplify the circuit complexity, and is implemented in the UCC3889 Bias Control IC with complete details to follow.

CONVERTER DESIGN EQUATIONS

Circuit components are primarily determined by several key factors; switching frequency, output power, efficiency and duty cycle. First, the voltage conversion relationship for the Flyback topology is reviewed.

Duty Cycle :

Duty cycle (d) = $\frac{t_{ON}}{t_{PERIOD}}$

where $t_{PERIOD} = t_{ON} + t_{OFF}$, or $\frac{1}{f_{SWITCHING}}$

For the Flyback topology, the duty cycle can be approximated by the following relationship:

$$V_{OUT} = V_{IN} \bullet \frac{d}{1 - d}$$

The cascaded Flyback conversion technique utilizes the output of the first Flyback converter as the input to the second stage. The voltage transformation of the two Flyback converters in series can be approximated by :

$$V_{OUT} = V_{IN} \left(\frac{d}{1 - d} \right)^2$$

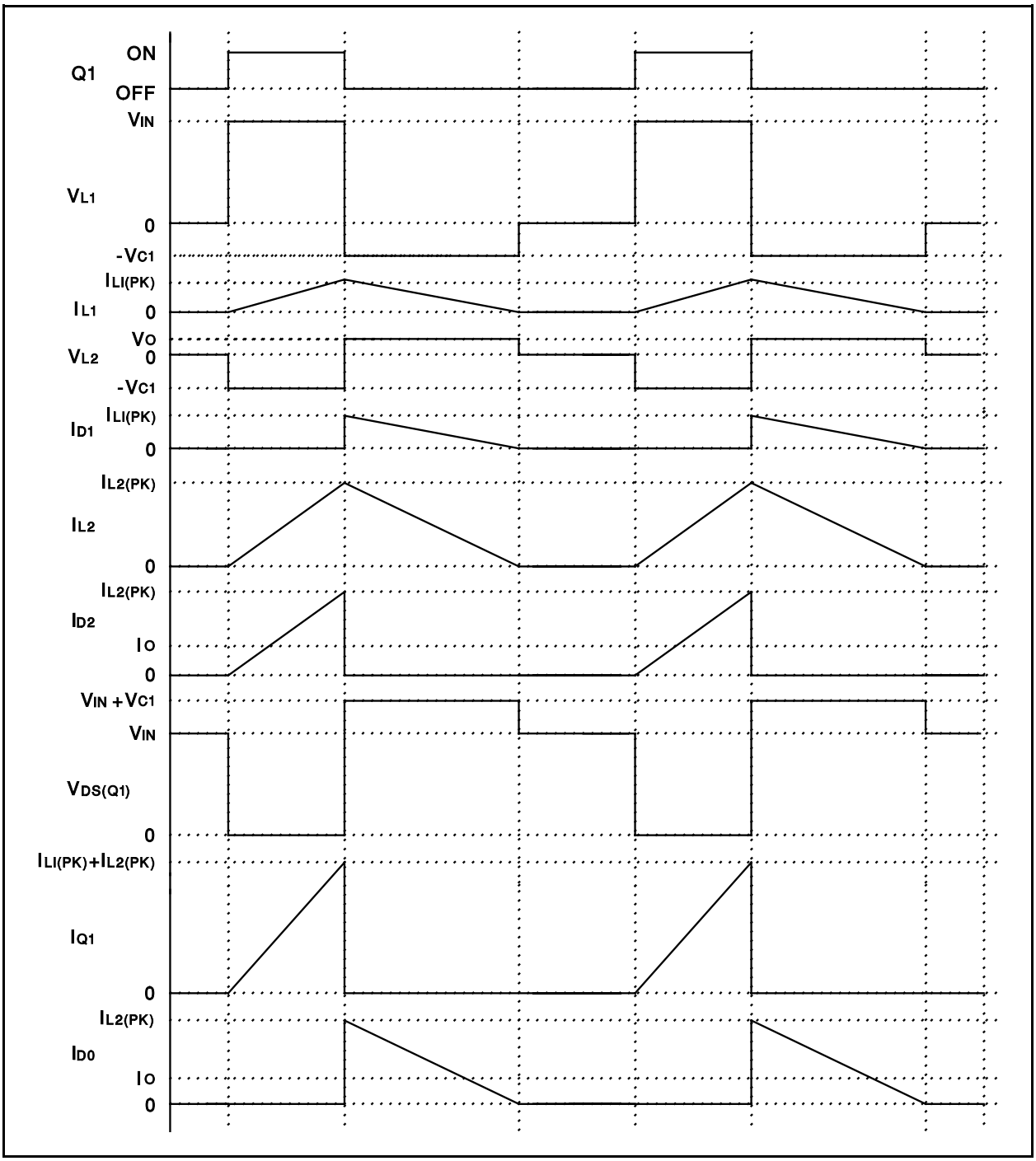

Figure 2. Converter Waveforms

This equation can be rearranged to solve for the duty cycle with respect to VIN and V**OUT** as:

$$\text{duty cycle} = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

Input Power :

$$P_{IN} = \frac{P_{IN}}{n} \text{ ; where } n = \text{efficiency}$$

Input Current :

$$I_{IN} = \frac{P_{IN}}{V_{IN}} \text{ ; or } I_{IN} = \frac{P_{OUT}}{(V_{IN} \bullet n)}$$

Peak Inductor Current :

The peak inductor current changes with line and load conditions according to the following relationship :

$$I_{LPK} = \frac{2 \bullet I_{IN}}{d}$$

Inductor Value :

The inductor values are obtained from the equation :

$$L = \frac{V \bullet \Delta t}{\Delta I}$$

Any set of operating conditions can be used to solve this, and other equations. It is often easiest to standardize on using low line, full load conditions when the inductor (L1) is charging during the switch ON-time.

$$L = V_{INmin} \bullet \frac{t_{ON}}{I_{LPK}}$$

The second Flyback inductor value (L2) is obtained using this equation but by substituting the output voltage of the first converter (V**OUT**1) for VIN.

OTHER COMPONENTS

Capacitors are selected to adequately provide a filtered DC voltage with little ripple, and to handle the ripple current without excessive self heating. Similarly, diode selection is based upon the maximum reverse voltage, forward current and acceptable recovery times for this application. The main switch (Q1) must withstand the high flyback voltage of the first converter and exhibit low conduction loss. Most 600V MOSFET's with less than 10 ohms of on-resistance (Rds on) are good candidates for this low power application.

CONTROL SECTION

The block diagram of the UCC3889 Off-line Power Supply Controller is shown in Figure 3. This IC incorporates several innovative features to reduce external circuitry and complexity while providing control to regulate the output voltage. A variable ON-time and variable OFF-time control algorithm is used to perform regulation. The switch ON-time is

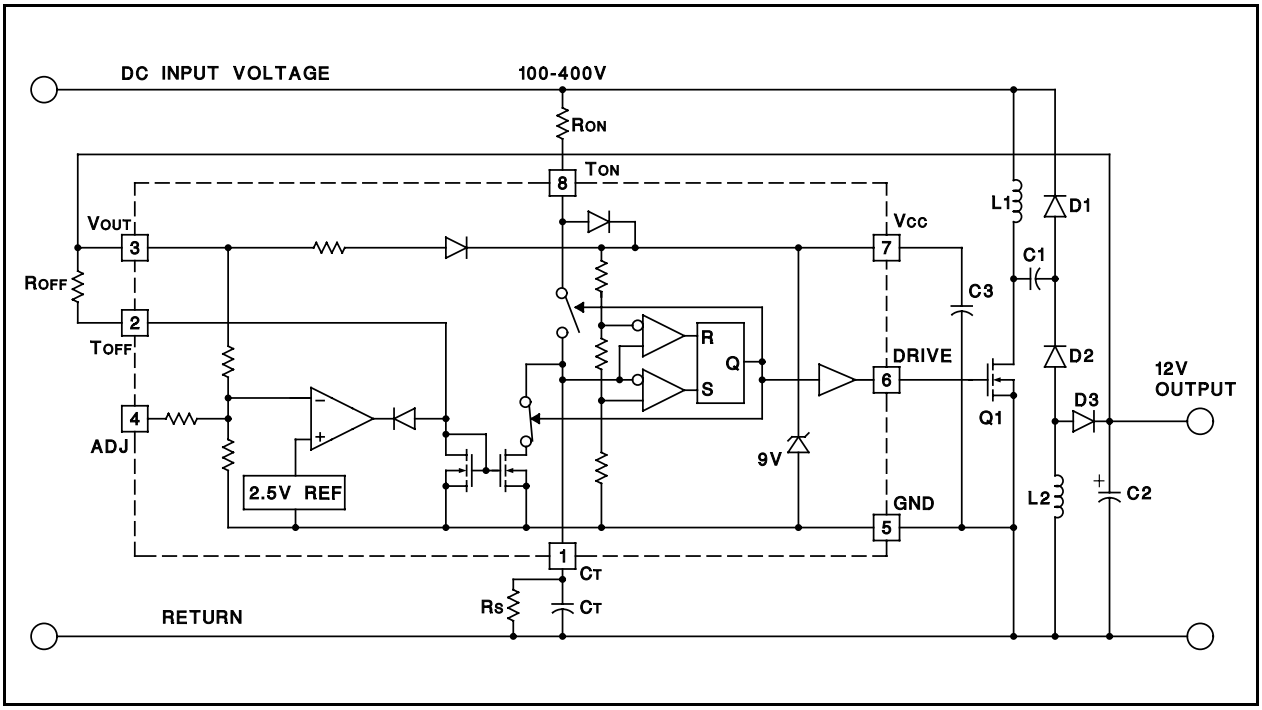

Figure 3. UCC1889 Typical Application

varied inversely with the supply input voltage, whereas the OFF-time is varied inversely with the supply's output voltage. This results in inherent short circuit protection, input voltage feedforward and a greatly simplified control technique. Operation and programming of these key features will be explored in more thorough detail.

POWERING THE UCC3889 CONTROLLER

Note that the UCC3889 is powered by connecting a resistor from the IC's TON pin to the high voltage supply, and not from the VCC connection. An internal switch directs the current from TON to either VCC or to a current mirror used for a timing function, and further details are presented in the TIMING section. Prior to turn-on, this switch is positioned to connect TON to VCC, steering the current into the VCC supply capacitor.

This BiCMOS Control IC consumes less than 250 microamps from the input supply while V**CC** is below it's 8.5 volt undervoltage lockout (UVLO) turn-on threshold. Once on, the IC typically draws only 1.5 milliamps from V**OUT**, and has a UVLO turn-off threshold of 6.3 volts. The V**CC** supply capacitor, CVcc, must maintain the IC supply voltage within it's 2.2 volt UVLO hysteresis region during the start-up of the converter.

Additionally, the minimum line voltage to begin operation of the converter can be programmed. RON, the timing circuit programming resistor also functions to program a current indicative of the AC input line voltage. Turn on occurs when this current reaches 220µA typically, so select the value of RON accordingly. This protection feature therefore will require a minimum current drawn by the IC from the line at all times, so the worst case power dissipation for RON will be at high line.

Two other noteworthy features are the IC's internal 9V zener clamp diode between V**CC** and ground, and the switched current source and diode from V**OUT** to V**CC**. The zener eliminates the need for external overvoltage protection when powered from a current source (resistor) to a high voltage supply, typical of an off-line converter. It also clamps the supply voltage when normally powered from the converter's output voltage. When V**OUT** rises above V**CC**, a switched internal current source is enabled thus limiting the current shunted to ground by the zener clamp diode. This helps minimize wasted power which would otherwise reduce overall efficiency and raise the IC's junction temperature. The series diode also prevents V**CC** from powering V**OUT** during start-up and short circuited output conditions.

GATE DRIVE OUTPUT

A CMOS totempole output stage is incorporated in this IC which provides a rail-to-rail voltage swing of the DRIVE output. A 200mA peak sink current and a 150mA peak source current will adequately drive MOSFETs gates for this low power application. Typical rise and fall times into a 1 nanoFarad load are 35 and 25 nanoseconds respectively.

Schottky clamp diodes to protect the IC's gate drive output from swings below ground and above VCC are NOT needed. The internal body diodes of the CMOS output stage transistors provide sufficient clamping.

OSCILLATOR AND TIMING FUNCTIONS

Programming begins with a selection of the highest operating frequency which will typically occur at low line and full load. As either the load is decreased, or input line increased, the switching frequency will adjust to regulate the output voltage. Therefore, the first parameter to determine is the switching frequency, FS. A good first approximation is 100kHz which will be used for this example.

Fs = 100kHz at low line, full load

The switching frequency selection will determine the exact values of the converter inductors (L1 and L2) in addition to the exact ON-time and OFF-time. Once the inductor values are calculated, the IC can be programmed to deliver the specific control timing functions, T**ON** and TOFF. Likewise, the selected ON and OFF times can be used to determine the exact inductor values needed to facilitate the power conversion.

Switch ON-time is developed by charging a timing capacitor from a constant current source. The exact charging current is varied directly with the converter input voltage to deliver a constant volt-second charging of the timing capacitor. This characteristic will exhibit input voltage feedforward and immunize the output from changes in line voltage.

During the charging period of the timing capacitor, the voltage at TON is approximately 4.5 volts. Note that only eighty percent (80%) of the current into the TON pin is used to charge the timing capacitor. The other twenty percent is diverted to the minimum line voltage detection circuitry which is described in the Protection Circuits portion of this Application Note. The exact timing capacitor charging current is therefore :

$$I(C_{T+}) = 0.8 \bullet \frac{(V_{IN} - 4.5)}{Rt_{ON}}$$

The timing capacitor has a peak to peak amplitude of approximately 3.7 volts for high noise immunity. It begins charging from a lower threshold of 1.3 volts to it's upper threshold of 5.0 volts. While the timing capacitor is charging, the IC's output is high and the converter switch is on. The control circuit ON-time is programmed according to the following formula:

$$t_{ON} = \frac{C_T \bullet 3.7}{I(C_{T+})}$$

This can also be expressed as :

$$t_{ON} = \frac{4.6 \bullet C_T \bullet Rt_{ON}}{V_{IN} - 4.5}$$

The ON-time must correspond to the time required to charge the inductors to a peak current value necessary to maintain regulation of the output voltage for any given set of line and load conditions. Note that the exact voltage at TON will rise from about 2.5 to 6.5 volts while the timing capacitor is charging, so these equations are approximations.

Once the timing capacitor crosses the upper oscillator threshold, the IC output goes low and the main switch is turned off. The timing capacitor is then discharged by a current programmed at the TOFF pin. This discharge current is varied as a function of the converter's output voltage to perform regulation, facilitate startup and provide protection against overload and short circuit conditions. Discharge current is programmed by a resistor (ROFF) from the TOFF pin to ground according to the following equation:

$$I(C_{T-}) = \frac{V_{OUT} - 0.7}{R_{OFF}}$$

The OFF-time is expressed as :

$$t_{OFF} = \frac{3.7 \bullet C_T \bullet R_{OFF}}{V_{OUT} - 0.7}$$

The total conversion period is a sum of the ON-time and OFF-time for a given set of operating conditions. Combining equations, this can be stated as:

$$t_{PERIOD} = 3.7 \bullet C_T \bullet \left(\frac{Rt_{ON}}{0.8 \bullet (V_{IN} - 4.5)} + \frac{Rt_{OFF}}{V_{OUT} - 0.7} \right)$$

Since one percent resistors are more readily available than capacitors with such a tight tolerance, it is advisable to first select the timing capacitor. Also, resistor values should be kept as high as possible to minimize oscillator currents to attain high overall efficiency, especially in a low power application. A good first approximation is to use 150pF for the timing capacitor value which will "home-in" on timing resistor values between 200k and 2meg ohms for approximately 100kHz operation.

C_T = 150pF (first approximation)

REGULATING THE OUTPUT VOLTAGE

The converter output voltage can be regulated in two different modes, depending on the application. In it's simplest configuration, the output voltage is connected to the IC's VOUT pin and the ADJ pin is unused. An internal 116k/30k ohm resistor network is used to divide the output voltage down for comparison to a precision 2.5 volt reference at the transconductance (gm) amplifier. It's output alters the timing capacitor discharge current to adjust the Off-time in response to any changes in the converter output voltage. In this configuration with the ADJ pin "floating", the output voltage is regulated at 12 volts. This level was selected for general purposes and is compatible with many applications.

Another simple configuration of this control circuit is to ground the ADJ pin. An additional 50kΩ is then placed in parallel with the 30kΩ internal divider resistor thus lowering the impedance to about 18.75kΩ. Grounding the ADJ pin will regulate the converter output voltage at approximately 18 volts instead of 12 volts, as with the ADJ pin floating. This amplitude was selected for use with many popular off-line PWMs as this converters principal load which utilize a 16 volt turn-on threshold. After accommodating their UVLO tolerances, eighteen volts was selected to fulfill nearly all PWM undervoltage lockout requirements.

The converter output voltage can be programmed for any level above 2.5 volts with two parts. An external resistive divider network between VOUT, ADJ and GND is all that's needed. This should be a lower impedance than the IC's internal divider network to null out any inaccuracies due to initial tolerance. By proper IC layout design and procedures, resistor ratios within the device will be maintained quite accurately although their exact values can vary significantly. For this reason, best results are obtained by using lower impedances externally than the 116k, 30k and 50k used within the UCC3889.

CLOSING THE FEEDBACK LOOP

An internal transconductance amplifier (gm type) is used to maintain regulation of the output voltage. The converter's output voltage is divided down by the 116k and 30k ohm resistor network and fed to the inverting input of the error amplifier. This statement applies for the simple configuration where the ADJ pin is unused and left floating. For all other applications which utilize the ADJ pin for programming the output voltage, then the 50k ohm series resistance must be accommodated in the design

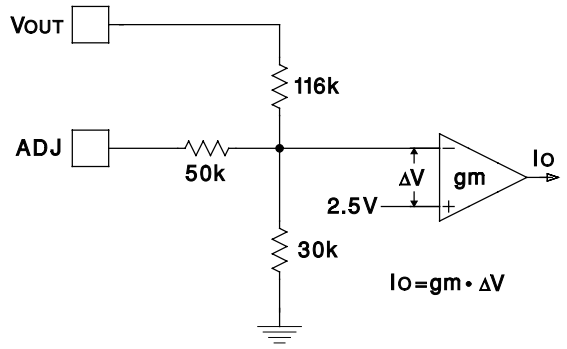

Figure 4. Adjust Pin Details

equations, as shown in Figure 4. For either case, the noninverting error amplifier input is internally tied to a precise 2.5 volt reference. The corresponding amplifier output current is the transconductance of the amplifier (gm) multiplied by the difference in amplifier input voltages (ΔV) and is expressed as:

$$I(E/A)_{OUT} = gm \bullet \Delta V, \text{ where } gm = 1mA/V$$

The error amplifier output current is used to modulate the discharge current of the timing capacitor and perform regulation. This current is subtracted from the capacitor's maximum discharge current which is programmed by ROFF, as shown in Figure 5. Note that the maximum discharge current is limited to 225 microamps within the IC, so a value below this should be used.

When the converter output voltage is low, the timing capacitor discharge current is also low. This is typical of start-up and short circuit conditions. Low discharge current indicates a long discharge time, or OFF-time for CT, corresponding to a low duty cycle. This feature delivers excellent protection under either of these conditions. As the output voltage increases, so does the discharge current. This has the effect of widening the duty cycle in response to the output voltage being lower than it's ideal setpoint. More energy is transferred as the duty cycle widens which continues to raise the output voltage.

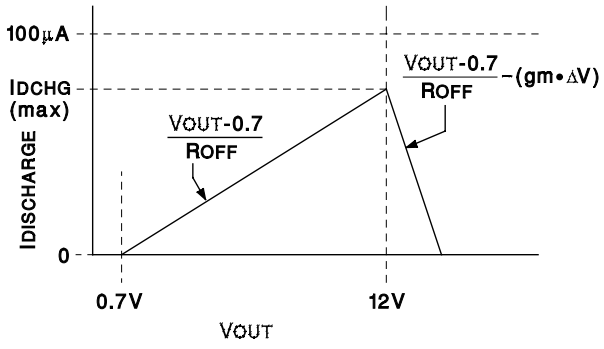

Figure 5. Discharge I vs. VOUT

As the exact point of regulation is reached, the timing capacitor discharge current will decrease as shown in Figure 5. This has the effect of reducing the effective duty cycle in response to the output voltage getting above the ideal threshold. If the output voltage continues to climb, then the discharge current is reduced even further. This will result in a longer OFF-time, or further reduced duty cycle, thus bringing the output voltage back to it's set point. Note that this operational mode also provides overvoltage protection.

PROTECTION CIRCUITRY

For an eight pin device, this UCC3889 features a number of internal protection features. As highlighted in previous sections, the IC has a 9V zener clamp on its supply rail. There is also a diode isolating VCC from the normal power source (VOUT) to keep the IC alive in case of a shorted output or overload condition. A switched current source also protects the zener from the low impedance present at VOUT.

Undervoltage lockout guarantees that the IC does not turn on until all internal circuits are properly biased for normal operation. It also insures an adequate gate drive amplitude is present to the main switch. This is performed by the "VCC OK" comparator as indicated in the UCC3889 block diagram, Figure 3.

Low line lockout protection is also contained within the IC to prevent operation during brown-out conditions and at power down. This eliminates the potential for excessively low frequency operation which can cause saturation of the inductors and abnormally high currents within the power stage. One-fifth of the current flowing into TON is used in conjunction with the "V LINE OK" comparator to detect this situation. Note that this conditional test is performed at every oscillator clock cycle during the charging of the timing capacitor. To further reduce power consumption, the current used for detection of low line, in addition to CT's charging current are switched off while the oscillator discharges each cycle.

Once a low line fault triggers the "V LINE OK" comparator, a 0.5 millisecond fault delay period begins. During this time the IC output is held off regardless of the oscillator operation. This delay limits the converter's retry rate during a brownout to around 2 kilohertz which is a significant reduction in comparison to the switching frequency. In addition, the ON-time of the converter is reduced to 600ns independent of the input line voltage.

Further details and specifications can be obtained on the device's datasheet.

DESIGN EXAMPLE

V_{IN} = 80 to 132VAC, or 100 to 180VDC

V_{OUT} = 12VDC

P_{OUT} = 1 Watt maximum

$F_{SWITCHING}$ = 100kHz

Efficiency = 50% (estimate)

Low line, full load condition will be used to begin the design procedure.

Step 1. Calculate Maximum Duty Cycle

$$\text{DutyCycle (d)} = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

$$d(max) = \frac{1}{1+\sqrt{\frac{100}{12}}} = \frac{1}{3.887} =$$

d(max) = 0.257 (roughly 26%)

Step 2. Calculate t_{ON}(max)

$$F_{SWITCHING} = \frac{1}{t_{PERIOD}} = \frac{1}{10\mu s} = 100kHz$$

$$t_{ON}(max) = \frac{d(max)}{F_{SWITCHING}}$$

$$t_{ON}(max) = \frac{0.257}{100kHz} = 2.57\mu s$$

Step 3. Calculate t_{OFF}(min)

$t_{OFF}(min) = t_{PERIOD} - t_{ON}(max)$

$t_{OFF}(min) = 10\mu s - 2.57\mu s = 7.43\mu s$

Step 4. Calculate the Maximum Input Power

$$P_{IN}(max) = \frac{P_{OUT}}{n(efficiency)} = \frac{1W}{0.5} = 2W$$

Step 5. Calculate the Input Current at Low Line

$$I_{IN} = \frac{P_{IN}}{V_{IN}(min)}$$

$$I_{IN} = \frac{2W}{100V} = 0.020A$$

Step 6. Calculate the Peak Inductor Current, I_{L1}(pk)

$$I_{L1}(pk) = 2 \bullet \frac{I_{IN}}{d} = 2 \bullet \frac{0.020}{0.257} = 0.156A$$

Step 7. Calculate the First Inductor Value (L1)

$$L1 = \frac{V_{IN} \bullet t_{ON}(max)}{I_{L1}(pk)} = 100 \bullet 2.57 \bullet \frac{10^{-6}}{0.156} = 1.67mH$$

Step 8. Calculate the Output Voltage of the First Flyback Stage

Since the volt-second products of the ON-time and OFF-time must balance for any inductor, then $V_{IN} \bullet t_{ON} = V_{OUT} \bullet t_{OFF}$, where V_{OUT} is VC1.

$$VC1 = V_{IN} \bullet \frac{t_{ON}}{t_{OFF}} = 100 \bullet \frac{2.57\mu s}{7.43\mu s} = 34.6V$$

Note that the second inductor (L2) is switched across this voltage while the main switch is on, so VC1 is the applied voltage to the second Flyback stage. Although this capacitor is switched between the lower and upper supply rails, the voltage rating of C1 is much lower than the input. The worst case can be easily calculated using the previous equation for VC1, but note that the IC will adjust the duty cycle to minimize this voltage change over line and load ranges. Specifically, the switching frequency will adjust, so a high voltage capacitor is not needed for normal operation.

Step 9. Calculate the Peak Current in the Second Inductor (L2)

$$I_{L2}(pk) = 2 \bullet \frac{I_{OUT}}{1 - d}$$

$$\text{where } I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{1W}{12V} = 0.083A$$

$$I_{L2}(pk) = \frac{2 \bullet I_{OUT}}{d} = \frac{2 \bullet 0.083}{1 - 0.257} = 0.223A$$

Step 10. Calculate the Second Inductor Value (L2) using the Output Voltage of the First Stage, ON-time and Required Peak Current of L2.

$$L2 = VC1 \bullet \frac{t_{ON}}{I_{L2}(pk)} = \frac{34.6 \bullet 2.57 \bullet 10^{-6}}{0.223} = 398\mu H$$

Step 11. Verify the Estimated Output Voltage, V_{OUT}

$$V_{OUT} = \frac{V_{IN}(stage\ 2) \bullet d}{1 - d}$$

$$V_{OUT} = \frac{34.6 \bullet 0.257}{0.743} \approx 12.0V$$

Note that this is an approximation and does not account for the output rectifier voltage drop nor any other losses. The control circuit will adjust for these losses since it is operating closed loop and modify the OFF-time, hence duty cycle, accordingly.

PROGRAMMING THE UCC3889 FUNCTIONS

The timing functions of the IC will be programmed according to the timing intervals which

have been calculated for 100kHz operation. A 150pF timing capacitor has been selected as a starting point to simplify the design process. The specific ON-time and OFF-time programming resistors are obtained from the previous equations by inserting the appropriate times and capacitor value.

Step 12. Calculate R_{TON}

$$R_{TON} = \frac{t_{ON} \bullet (V_{IN} - 4.5)}{4.6 \bullet C_T}$$

$$R_{TON} = \frac{2.57 \bullet 10^{-6} \bullet (100 - 4.5)}{4.6 \bullet 150 \bullet 10^{-12}}$$

R_{TON} = 348.9k (use 330kΩ)

Step 13. Calculate R_{OFF}

$$R_{OFF} = \frac{t_{OFF} \bullet (V_{OUT} - 0.7)}{3.7 \bullet C_T}$$

$$R_{OFF} = \frac{7.43 \bullet 10^{-6} \bullet (12 - 0.7)}{3.7 \bullet 150 \bullet 10^{-12}}$$

R_{OFF} = 149.3k (use 150k)

Step 14. Calculate R_{DCHG}

A resistor placed in parallel with the timing capacitor is used to discharge C_T when the converter output voltage goes to zero. This also sets the maximum OFF-time of the switch and is used to program the minimum frequency for startup and short circuit protection. A one millisecond (1ms) duration will be used for this example.

$$R_{DCHG} \approx \frac{t_{OFFmax}}{3.7 \bullet C_T}$$

R_{DCHG} = 1.78 meg (use 1.8 or 2 meg)

PROGRAMMING THE OTHER PINS

An output voltage of 12VDC has been selected which does not require a resistor divider for feedback. The IC's ADJ pin is open for this application. Also, the MOSFET gate will be directly connected to the IC's output and no gate drive resistor is needed. Typical 0.1µF bypassing will be used at the IC's supply voltage, V_{CC}. A tight prototype layout is also recommended as good design practice.

PROTOTYPE ASSEMBLY

The entire 1 Watt off-line power supply can be built with as few as 16 parts for a 110VAC only input as shown in Figure 6. Using surface mount assembly techniques and a tight PC board layout, the completed assembly requires about one square inch (1" sq.of area). A performance evaluation for this example is summarized below.

UNIVERSAL INPUT VOLTAGE (80 to 265VAC)

Due to the higher voltage input (373Vpk), L1 and R_{TON} will be broken-up into series components which can conservatively handle the applied voltage. For example, three identical 1/4W resistors will be used as R_{TON} due to the maximum voltage rating of 200 volts each. Inductor L1 is divided into two very inexpensive axial type inductors also placed in series to withstand the high voltage. All other lower voltage components are similar to the 110VAC only application, and are readily available, standard types used in the industry.

The bulk input capacitor should be conservatively rated for 450VDC, and the input diodes are 800V types. Since the circuit operates in the discontinuous inductor current mode, diode switching speed is not very critical. However, diodes should have recovery times below a quarter of a microsecond (trr < 250ns) for efficient high frequency operation, and rated for the proper reverse voltage. Standard

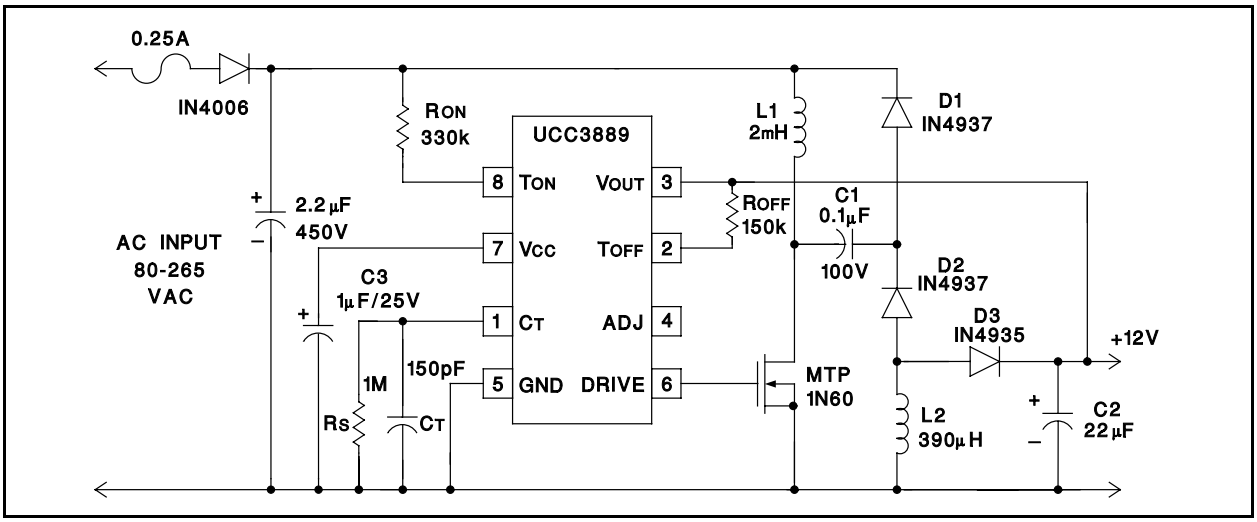

Figure 6. Design Example

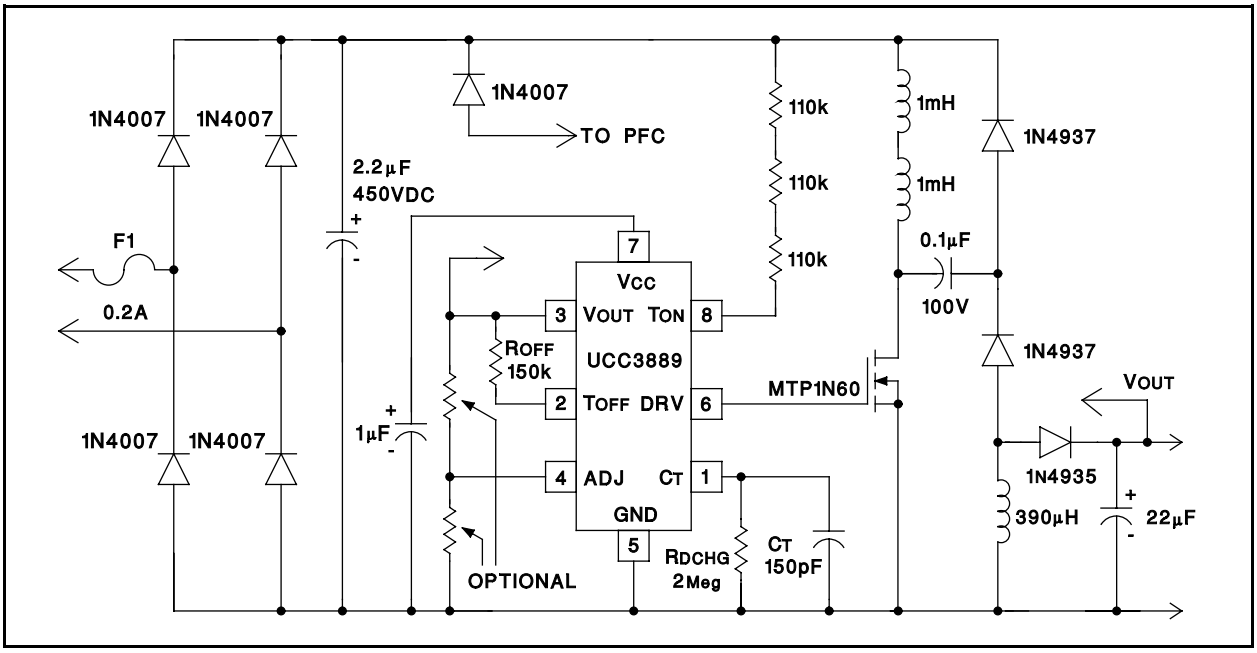

Figure 7. Typical 110/220VAC Application

1N4937 type 600V diodes can be used in the high voltage switching sections, and a lower voltage 1N4935 is a good selection for the output diode. To simplify manufacturing, 1N4937s can be used for all three rectifier applications. The complete schematic and list of components is shown in figure 7. Measured performance is indicated above.

UCC3889 Application Circuit Performance Measurements

110VAC (only) and 110/220 Universal AC input Nonisolated models

VIN (VAC)	VOUT (VDC)	POUT (W)	EFFCY (approx)
78 (both)	12.16	0.58	45%
	12.15	0.81	47%
	12.11	1.00	47%
128 (both)	12.22	0.59	45%
	12.23	0.82	45%
	12.24	1.02	44%
170 (110/220 only)	12.24	0.59	44%
	12.25	0.82	44%
	12.26	1.03	44%
264 (110/220 only)	12.24	0.59	40%
	12.26	0.82	42%
	12.28	1.034	43%

VOUT nominal = 12.195V, ±0.7% (±85mV)
Efficiency nominal = 44%

ISOLATING THE OUTPUT VOLTAGE

An isolated output voltage is obtainable with this UCC3889 controlled cascaded Flyback conversion technique. While several possibilities exist, one of the easiest places to attain isolation is at the inductor used in the second power conversion stage, as shown in Figure 8. Due to its lower inductance than the first stage, fewer turns are required and generally a smaller core can be utilized. Note, however, that the core size could be predominantly determined by the isolation requirements and not the stored energy requirements of the system. Designers are encouraged to pursue various core geometry options depending on the specific isolation voltage, safety agency and creepage/clearance distance requirements.

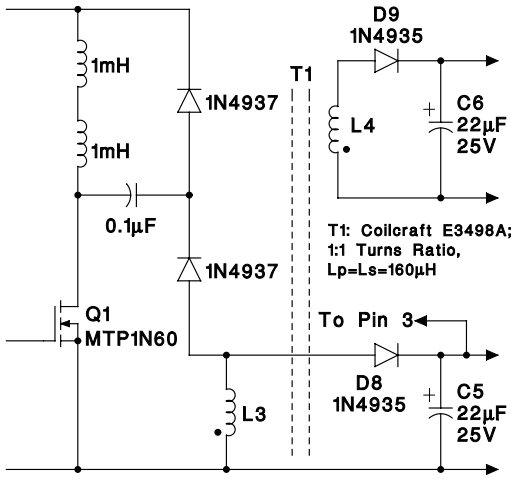

Figure 8. Isolated Output

One rather quick, inexpensive and effective way to provide an isolated output is to use an "off-the-shelf" isolation transformer which meets the design specifications. Many standard "Common Mode Line Chokes" used for EMI filters and suppression meet the appropriate voltage isolation requirements. One example of this is the Coilcraft "EE Style" series of line chokes. Specifically, their E3496A through E3498A coupled chokes have inductances between 168µH and 468µH, and can handle currents from 2.5 to 4 amps. As stated previously, there are a variety of other manufacturers, core styles and ratings to choose from, in addition to designing one's own.

REGULATING THE ISOLATED OUTPUT

Maintaining adequate regulation of the isolated output voltage over all line and load conditions without any feedback path to the IC via optocoupler (etc.) is possible. If both windings of the isolating inductor were perfectly coupled then the voltages of each would look identical regardless of which one was being loaded. As is always the case, truly perfect magnetic coupling cannot be obtained, resulting in detrimental series, leakage inductance. This detracts from the ability for one winding to perfectly track the other which will degrade output voltage regulation. These effects are minimized by a low leakage inductance design, but some finite leakage is to be expected, especially with high voltage isolation between windings.

Preloading of the "feedback" winding which powers the UCC3889 IC and provides the voltage feedback information will improve regulation of the isolated output over all load conditions. While this does reduce overall efficiency, the small penalty may be an acceptable compromise for the improvement in regulation.

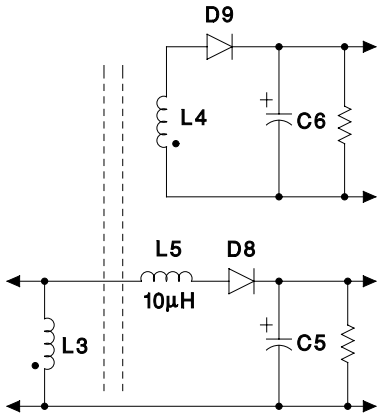

Figure 9. Adding Series Inductance to Improve Cross Regulation

The best option to improve regulation is to add some series inductance to the "feedback" winding as shown in Figure 9. Note that when placed as shown, the inductance is not part of the circuit while the coupled inductor is charging, but only during the discharge. This additional inductance has the effect of steering all ripple current (hence stored energy) to the isolated output which is more heavily loaded. Energy is transferred to where it is needed most, at the load, and not to the control circuit. By varying the series inductance and preloading of each output, excellent regulation of the isolated output voltage can be achieved without requiring a separate feedback path.

An isolated version of the universal input range application circuit of Figure 10 was constructed and

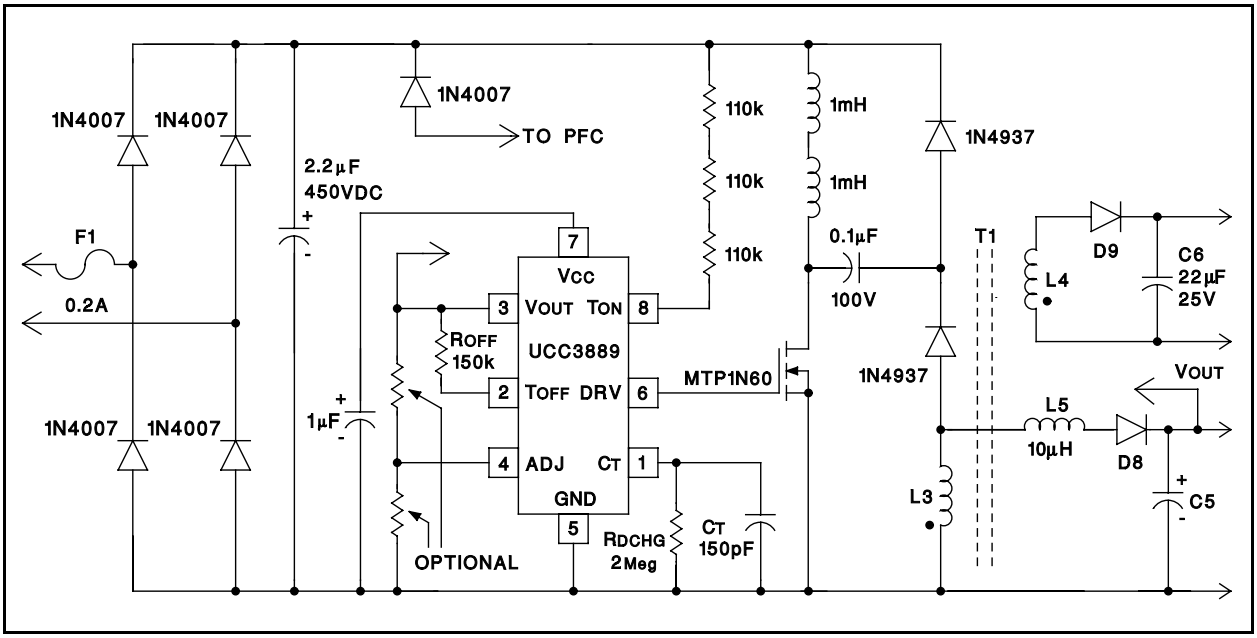

Figure 10. Isolated Output with Universal AC Input Range

tested. Performance results are shown below for comparison to the nonisolated version.

UCC3889 Application Circuit Performance Measurements

110/220 Universal AC Input with Isolated Output

VIN (VAC)	VNONISO (VDC)	VISO (VDC)	POUT (W)	EFFCY (approx)
78	12.37	12.07	0.41	45%
	12.31	11.85	0.63	46%
	12.26	11.63	0.82	47%
	12.26	11.33	0.99	51%
156	12.39	12.14	0.42	44%
	12.36	12.00	0.64	45%
	12.37	11.80	0.85	46%
	12.37	11.72	1.06	44%
195	12.42	11.77	0.39	43%
	12.39	11.59	0.60	44%
	12.36	11.33	0.78	44%
	12.33	11.42	1.00	45%
240	12.43	11.819	0.39	39%
	12.41	11.697	0.61	42%
	12.39	11.605	0.81	43%
	12.38	11.626	1.04	43%

Nonisolated V_{OUT} nominal = 12.349V, ±0.7% (±85mV)
Isolated VOUT nominal = 11.74V, ±3.4% (±400mV)
Efficiency nominal = 45%
Main Transformer = COILCRAFT E3498A "Common Mode EMI Filter Choke", Turns Ratio = 1:1, Lp = Ls = 160µH (approx), 3750VAC Isolation

EFFICIENCY

The efficiency measurements indicate the overall ratio of output power divided by the input power, and are typically around 45%. Note that this figure includes the power lost in the timing resistor (RTON**) connecting the input supply voltage to the UCC3889 for initial startup and continuous input line voltage detection. The power consumed to perform this function is approximately 30 milliwatts at low line, but nearly 400 milliwatts at high line. Once this loss is accounted for, the remaining losses demonstrate that this converter runs between 51% and 63% efficiency at high line, depending on load. It is clear that this cascaded flyback conversion technique is a highly efficient solution to low power applications, especially with a high voltage input.**

OTHER APPLICATIONS

Although primarily designed for off-line applications, the UCC3889 Bias Supply Controller and the cascaded Flyback Conversion technique are equally applicable for low power DC/DC converters. Typical usages are to generate a bias supply for the main PWM controller, or to deliver a regulated, low power output supply. The simple implementation of this control technique is further applicable to numerous other topologies including conventional Flyback, Forward and other single switch converters.

SUMMARY

The task of generating a low power, low voltage bias supply can be greatly simplified using this novel cascaded Flyback converter technique. Inexpensive, readily available standard components can be used in cost sensitive applications, while miniature surface mount devices are best suited where size is a premium. Furthermore, this approach can be utilized to generate an isolated low power supply without the complexity of voltage feedback circuitry. Finally, a sophisticated 8 pin IC, the UCC3889 Bias Supply Controller has been introduced to minimize external components while providing complete protection of the converter and regulation of the output voltage.

NOTES

1. The control technique implemented by the UCC3889 Control IC is used under agreement from Lambda Electronics and is patent pending. Designs incorporating this control technique are not in violation of this patent provided that the UCC3889 is used as the control device.

2. COILCRAFT's phone number is :
   1-800-322-2645 (U.S.).

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