

The UC3855 incorporates all of the control functions required to design a ZVT power stage with average current mode control. Average current mode control has been chosen for its ability to accurately program the input current while avoiding the slope compensation and poor noise immunity of other methods [5,6].

ZVT TECHNIQUE

ZVT Boost Converter Power Stage

The ZVT boost converter operates the same as a conventional boost converter throughout its switching cycle except during the switch transitions. Figure 1 shows the ZVT boost power stage. The ZVT network, consisting of Q_{ZVT} , $D2$, L_r , and C_r , provides active snubbing of the boost diode and main switch. The ZVT circuit operation has been described in [4, 7, 8] and will be reviewed here for completeness. Referring to Figure 2, the following timing intervals can be defined:

ZVT Timing

$t_0 - t_1$ During the time prior to t_0 , the main switch is off and diode D1 is conducting the full load current. At t_0 , the auxiliary switch (Q_{ZVT}) is turned on. With the auxiliary switch on, the current in L_r ramps up linearly to I_{IN} . During this time the current in

diode D1 is ramping down. When the diode current reaches zero the diode turns off (i.e. soft switching of D1). In the practical circuit some reverse recovery of the diode will occur since the diode needs time to remove the junction charge. The voltage across the ZVT inductor is V_O , and therefore the time required to ramp up to I_{in} is:

$$t_{01} = \frac{I_{IN}}{\left(\frac{V_O}{L_r}\right)}$$

$t_1 - t_2$ At t_1 , the L_r current has reached I_{IN} and L_r and C_r will begin to resonate. This resonant cycle discharges C_r until its voltage equals zero. The dv/dt of the drain voltage is controlled by C_r (C_r is the combination of the external C_{DS} and C_{OSS}). The current through L_r continues to increase while C_r discharges. The time required for the drain voltage to reach zero is 1/4 of the resonant period. At the end of this period the body diode of the main switch turns on.

$$t_{12} = \frac{\pi}{2} \cdot \sqrt{L_r C_r}$$

$t_2 - t_3$ At the beginning of this interval the switch drain voltage has reached 0V and the body diode is turned on. The current through the body diode is being driven by the ZVT inductor. The voltage

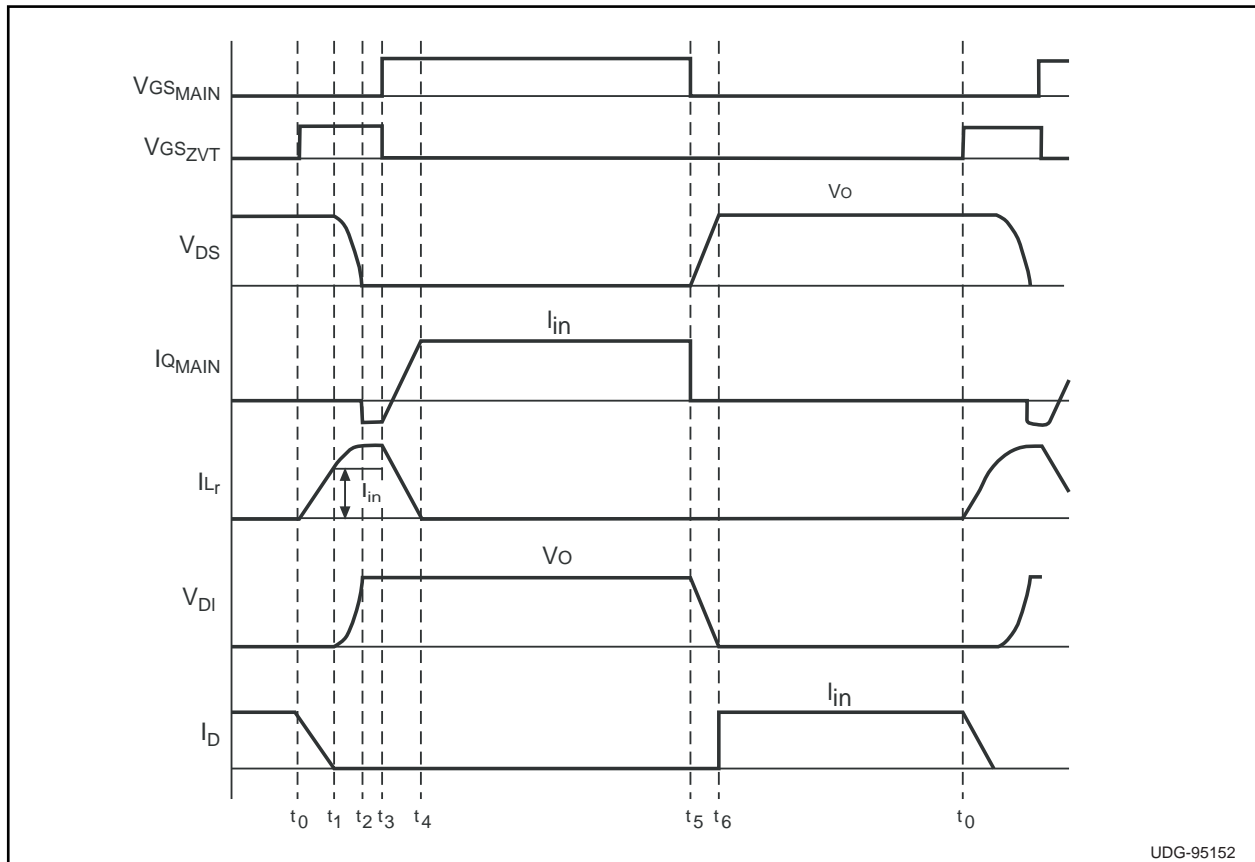


Figure 2. ZVT Timing Diagram

across the inductor is zero and therefore the current freewheels. At this time, the main switch can be turned on to achieve zero voltage switching.

$t_3 - t_4$ At t_3 , the UC3855 senses that the drain voltage of Q_{MAIN} has fallen to zero and turns on the MAIN switch while turning off the ZVT switch. After the ZVT switch turns off, the energy in L_r is discharged linearly through D2 to the load.

$t_4 - t_5$ At t_4 , the current in D2 goes to zero. When this occurs, the circuit is operating like a conventional boost converter. In a practical circuit however, L_r will resonate with C_{OSS} of the ZVT switch driving the node at the anode of D1 negative (since the opposite end of L_r is clamped to zero). This effect will be discussed in the ZVT circuit design section.

$t_5 - t_6$ This stage is also exactly like a conventional boost converter. The main switch turns off. The Q_{MAIN} drain-to-source node capacitance charges to V_O and the main diode begins to supply current to the load. Since the node capacitance initially holds the drain voltage to zero, the turn off losses are significantly reduced.

It can be seen through the above description that the operation of the converter differs from the conventional boost only during the turn-on switch transitions. The main power stage components experience no more voltage or current stress than normal, and the switch and diode both experience soft switching transitions. Having significantly reduced the switching losses, the operating frequency can be increased without an efficiency penalty. The diode also operates with much lower losses and therefore will operate at a lower temperature, increasing reliability. The soft switching transitions also reduce EMI, primarily caused by hard turn-off of the boost diode.

Control Circuit Requirements

In order to maintain zero voltage switching for the main switch, the ZVT switch must be on until the voltage on C_r resonates to zero. This can be accomplished by using a fixed delay equal to t_{ZVT} at low line and maximum load.

$$t_{\text{ZVT}} = \frac{I_{\text{INp}} \cdot L_r}{V_O} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_r}$$

However, this would give a longer than necessary delay at lighter load or higher line conditions, and therefore would increase the ZVT circuit conduction loss and increase the peak current stress. The UC3855 allows for a variable t_{ZVT} by sensing when the Q_{MAIN} drain voltage has fallen to zero. Once the voltage falls below the ZVS pin threshold volt-

age (2.5V), the ZVT gate drive signal is terminated and the main switch gate drive goes high. The control waveforms are shown in Figure 3. The switching period begins when the oscillator begins to discharge, and the ZVT gate drive goes high at the beginning of the discharge period. The ZVT signal will stay high until the ZVS pin senses the zero voltage condition or until the discharge period is over (the oscillator discharge time is the maximum ZVT pulse width). This allows the ZVT switch to be on only for as long as necessary.

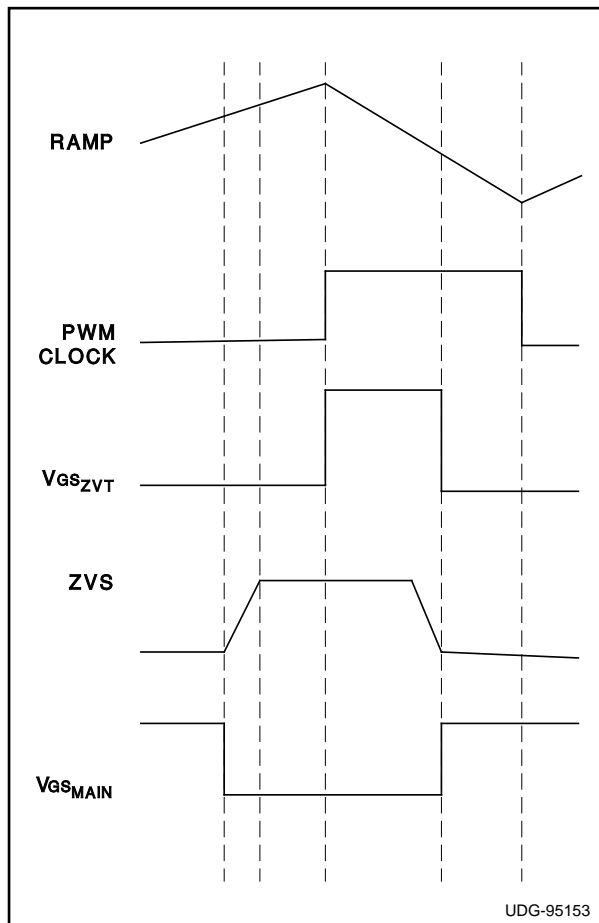


Figure 3. ZVT Control Waveforms

CONTROL CIRCUIT OPERATION AND DESIGN

Figure 4 shows the UC3855A/B block diagram (pin numbers correspond to DIL-20 packages). It shows a controller which incorporates the basic PFC circuitry, including average current mode control, and the drive circuitry to facilitate ZVT operation. The IC also has current waveform synthesizer circuitry to simplify current sensing, as well as overvoltage and overcurrent protection. In the following sections the control IC will be broken down into functional blocks and individually reviewed.

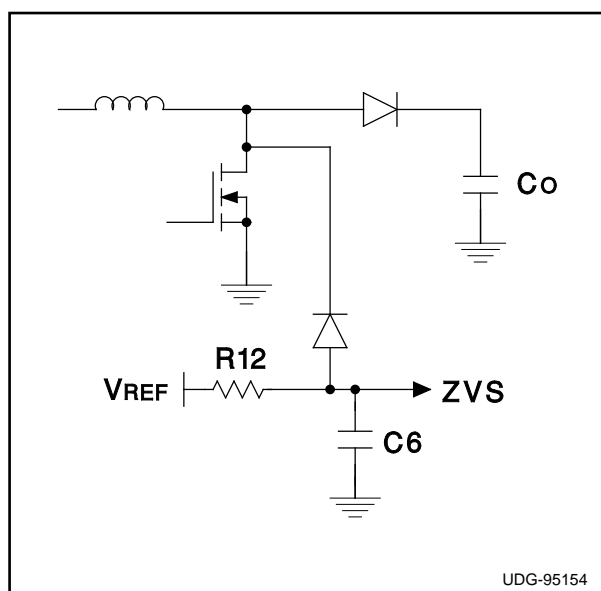


Figure 5. ZVS Sensing Circuit

The RC time constant should be fast enough to reach 2.5V at maximum duty cycle. The drain voltage is limited by the node capacitance which slows down the dv/dt across the main MOSFET, which reduces the high speed requirement on the ZVS circuit. The maximum ZVS pin voltage should be limited to V_{REF} , otherwise the ZVS circuitry can become latched and will not operate properly.

An alternative method for ZVS operation, is to sense the drain voltage through a simple voltage divider. This voltage will still have to be filtered (and clamped) however, so as not to inject noise into the ZVS pin.

Refer back to Figure 3 for the timing waveforms.

GATE DRIVES

The main drive can source $1.5A_{PK}$ and the ZVT drive is $0.75A_{PK}$. The main switch drive impedance requirements are reduced due to ZVT operation. At turn-on the drain voltage is at zero volts and therefore the Miller capacitance effect is not an issue, and during turn-off, the dv/dt is limited by the resonant capacitor. Since the ZVT MOSFET is generally at least two die sizes smaller than the main switch, its drive requirements are met with a lower peak current capability.

Multiplier / Divider Circuit

The multiplier section of the UC3855A/B is identical to the UC3854A/B. It incorporates input voltage feedforward (through the VRMS input) to eliminate loop gain dependence on the input voltage. There

are only three parameters (V_{VRMS} , I_{IAC} , and R_{IMO}) that need to be defined to properly set up the IC.

VRMS

The multiplier programs the line current and therefore effects the power drawn from the line. The VRMS pin is programmed by looking at the system power limits. Referring to the block diagram (Figure 4), the multiplier output equation is:

$$I_{IMO} = \frac{I_{IAC} \cdot (V_{EA} - 1.5)}{V_{VRMS}^2}$$

The power limit function is set by the maximum output voltage of the voltage loop error amplifier, V_{EA} (6V). The power limiting function is easily explained by looking at what happens for a given value of V_{EA} . If the AC line decreases by a factor of two, the feedforward voltage decreases by one fourth. This increases multiplier output current (and therefore line current) by two. The power drawn from the line has therefore remained constant. Conversely, if the load increases and the line stays constant, V_{EA} will increase, causing more line current to be drawn. It can be seen then, that V_{EA} is a voltage proportional to input power.

Normally the multiplier is set to limit maximum power at low line, corresponding to maximum error amplifier output voltage. The multiplier equation can be solved for the feedforward voltage that corresponds to maximum error amplifier voltage and maximum multiplier current (internally limited to 2 times I_{IAC}).

$$V_{VRMS}^2 = \frac{I_{IAC} \cdot (V_{EA} - 1.5)}{2 \cdot (I_{IAC})}$$

$$V_{VRMS} = 1.5V$$

Knowing the VRMS voltage at low line defines the voltage divider from the line to VRMS pin. This feedforward voltage must be relatively free of ripple in order to reduce the amount of second order harmonic that is present at the multiplier input (which in turn would cause 3rd order harmonics in the input current) [9]. The filtering will produce a dc voltage at the VRMS pin. Since the input voltage is defined in terms of its RMS value, the dc to RMS factor (0.9) must be taken into account [9]. For example, if the low line voltage is 85V, the attenuation required is:

$$\frac{85V_{RMS} \cdot (0.9)}{1.5 \cdot V_{DC}} = 51:1$$

At a high line of 270V, this will correspond to $V_{VRMS} = 4.76V$. The common mode range of the VRMS input is 0V to 5.5V. The calculated range is therefore within the accepted limits.

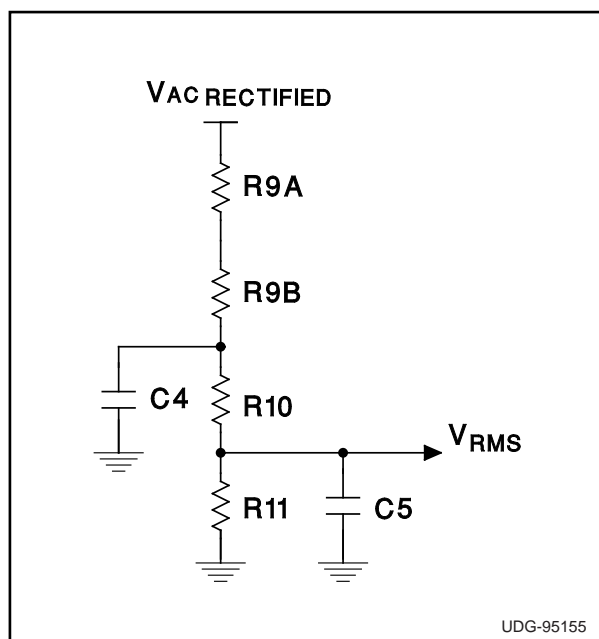


Figure 6. VRMS Circuit

A two pole filter is recommended to provide adequate attenuation without degrading the feedforward transient response. A single pole filter will require a pole at too low of a frequency to still allow VRMS to respond quickly enough to changes in line voltage.

The filter poles can be calculated once the distortion contribution from VRMS is determined. If the feedforward circuit's contribution to the total distortion is limited to 1.5%, the required attenuation of the filter can be calculated. Recall that the percentage of 2nd harmonic in a full wave rectified sine wave is approximately 66.7% of the dc value. The percentage of second harmonic will translate to the same percent 3rd harmonic distortion in the input current waveform [9]. Therefore, the filter attenuation required is:

$$\frac{1.5\%}{66.7\%} = 0.0025$$

The individual stages should have an attenuation of $\sqrt{0.0025}$ or 0.15. For a single stage filter:

$$A_V = \frac{f_c}{f} \Rightarrow f_c = 120\text{Hz} (0.15) = 18\text{Hz}$$

Referring to Figure 6 the components correspond to R9A = R9B = 390k Ω , R10 = 120k Ω , and R11 = 18k Ω with C4 = 0.082 μF and C5 = 0.47 μF .

I_{IAC}

The value of I_{IAC} is chosen to be 500 μA at high line. This value is somewhat arbitrary, however it

should be kept below 1mA to stay within the linear region of the multiplier. This corresponds to a total resistance of approximately 766k Ω from the line to IAC pin.

R_{IMO}

The multiplier output resistor can be calculated by recognizing that at low line and maximum load current, the multiplier output voltage will equal 1V (in order to stay below the undercurrent trip point). This will also correspond to the maximum sense voltage of the current transformer. The multiplier current under this condition is equal to $1\text{V} / R_{IMO}$, and can be equated with the multiplier equation which yields:

$$\frac{1\text{V}}{R_{IMO}} = \frac{I_{IAC} \cdot (V_{EA} - 1.5)}{V_{VRMS}^2}$$

At low line I_{IAC} will equal 156 μA (if low line = 85V and I_{IAC} was set to 500 μA at 270V), V_{EA} will be at its maximum of 6V, and V_{VRMS} will be 1.5V. Therefore R_{IMO} equals 3.2k Ω .

Current Synthesizer

Current sensing is simplified due to the current synthesis function built into the UC3855A/B. Switch current is the same as inductor current when the switch is on and can be sensed using a single current transformer. The current synthesizer charges a capacitor (CI) with a current proportional to the switch current when the switch is on. During the switch off-time, the inductor current waveform is reconstructed by the controller. To get an accurate measure of the inductor current then, all that is required is to reconstruct the down slope of the inductor current, which is given by:

$$\frac{\Delta i}{\Delta t} = \frac{V_{OUT} - V_{AC}}{L}$$

Discharging CI with a current proportional to $V_{OUT} - V_{AC}$ will allow reconstruction of the inductor current waveform. The capacitor down slope is :

$$\frac{\Delta v}{\Delta t} = \frac{I_{DIS}}{CI}$$

The UC3855A/B develops I_{DIS} by subtracting $I_{IAC}/4$, from a current proportional to V_{OUT} . The voltage at the RVS pin is regulated at 3V and therefore picking the RVS resistor will set the current proportional to V_{OUT} .

$$I_{DIS} = \frac{3\text{V}}{R_{RVS}} - \frac{I_{IAC}}{4}$$

The ratio of the current in R_{RVS} to $I_{IAC}/4$ should equal the ratio of V_{OUT} to V_{AC} . Therefore if

$I_{IAC} / 4$ is $125\mu\text{A}$, the current through R_{RVS} should be set to $130\mu\text{A}$.

$$R_{RVS} = \frac{3\text{V}}{130\mu\text{A}} = 23\text{k}\Omega, \text{ use } 22\text{k}\Omega$$

Equating inductor current slope with capacitor voltage slope, and recognizing that maximum slope occurs when V_{AC} equals zero, CI can be solved for:

$$CI = \frac{3 \cdot L \cdot N}{R_{RVS} \cdot V_{OUT} \cdot R_S}$$

where N is the current transformer (CT) turns ratio, (N_s / N_p) and R_S is the current sense resistor.

The current synthesizer has approximately 20mV of offset. This offset can cause distortion at the zero crossing of the line current. To null out this offset, a resistor can be connected between V_{REF} and the IMO pin. The resistor value is calculated based on R_{IMO} and the offset at the output of the synthesizer. For a 20mV offset and $R_{IMO} = 3.3\text{k}$ a resistor from V_{REF} to IMO of $1.2\text{M}\Omega$ will cancel the offset.

Current Sensing

Current Transformer

As was seen in the previous section, synthesizing inductor current with the UC3855A/B is quite simple. Only switch current needs to be sensed direct-

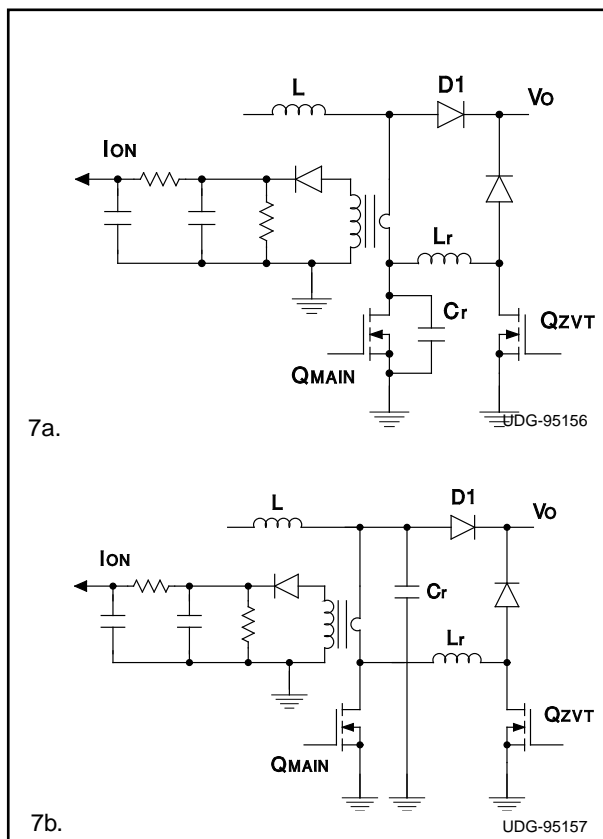


Figure 7. Current Transformer Sensing.

ly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation.

Several issues should be kept in mind when implementing the current transformer. At frequencies of a couple hundred kilohertz, core reset needs to be addressed. Contributing to the difficulty is the very high duty cycles inherent in a power factor correction circuit. In addition, the ZVT circuit can complicate the sensing/reset function. When the ZVT circuit turns on, it draws current from the line. In order to minimize line current distortion, this current should be measured. Placing the resonant inductor after the current transformer will ensure that the ZVT circuit current is measured. Similarly, when the main switch turns off, current will continue to flow into the resonant capacitor. While it is important to measure this current, if the capacitor is connected to the drain of the MOSFET, below the current transformer, this current will “eat” into the minimal reset time available at line zero crossings, where duty cycles are approaching 100%. This configuration is shown in Figure 7a. If the current transformer does not have enough time to reset, it can begin to saturate and lose accuracy, even if complete saturation is avoided, causing distortion at the zero crossings. A better configuration is shown in Figure 7b. In this circuit, the capacitor current will be measured when it discharges during the ZVT circuit on time. Since this occurs at the beginning of the switching cycle, the current transformer doesn’t lose any of its reset time. Connecting C_r above the current transformer will not adversely affect the MOSFET dv/dt control. Since the IC is controlling average current, it doesn’t matter whether the capacitor current is measured at the beginning or end of the switching cycle.

Figure 7 also shows that filtering is added to the transformer secondary in order to reduce noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.

In addition to position and reset considerations, actual current transformer construction must be considered. Using current transformers that have been designed and manufactured for operation at 20kHz will not give good performance at switching frequencies of 100kHz and greater. Low frequency designs generally have too much leakage inductance to be used for high frequency operation and can cause inaccurate sensing and/or noise problems.

Resistive Sensing

Resistive sensing is still possible with the UC3855A/B. Since both inputs to the current error amplifier are available to the user, resistive sensing

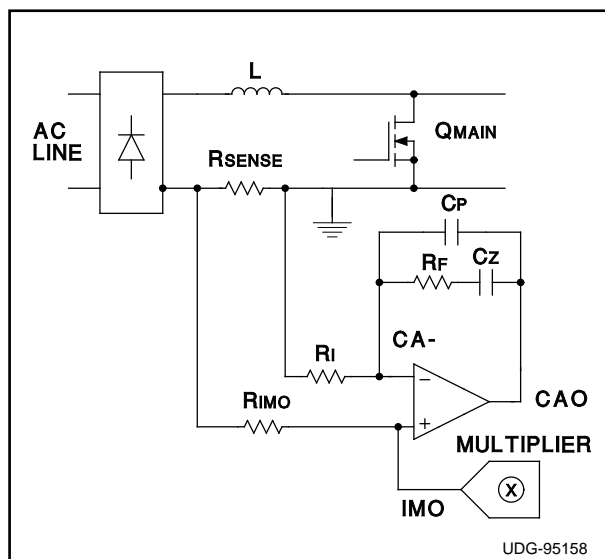


Figure 8. Resistive Sensing

is easy to implement. Figure 8 shows the typical configuration. The common mode range of the current error amplifier is -0.3V to 5.0V . The R_{IMO} value will remain the same as was calculated above if the maximum signal level remains at 1V . This will also allow the resistively sensed signal to be fed into ION and used for peak current limiting. It is recommended that the RVS resistor still be connected and a resistor connected from CS to ground in order to eliminate the possibility of noise being injected into these high impedance nodes.

Current Error Amplifier

The current error amplifier ensures that the input current drawn from the line follows the sinusoidal reference. The positive input to the amplifier is the multiplier output. The negative input is connected to the output of the current synthesizer (CS) through a resistor (usually the same value as R_{IMO}). The output of the current error amplifier is compared to the sawtooth waveform at the PWM comparator and terminates the duty cycle accordingly. At zero crossings of the line, the duty cycle will be at its maximum. Since the duty cycle is approaching 100%, proper reset of the current transformer will become increasingly difficult. Standard PWM controllers terminate the duty cycle during the oscillator discharge time, however, due to the ZVT operation, the UC3855A/B is capable of achieving 100% on-time. If the duty cycle is allowed to approach 100%, the current transformer will begin to saturate and cause the current error amplifier to “believe” that less current is being drawn from the line than is being commanded. This will cause the current amplifier to overcompensate, causing line current distortion at the zero crossings.

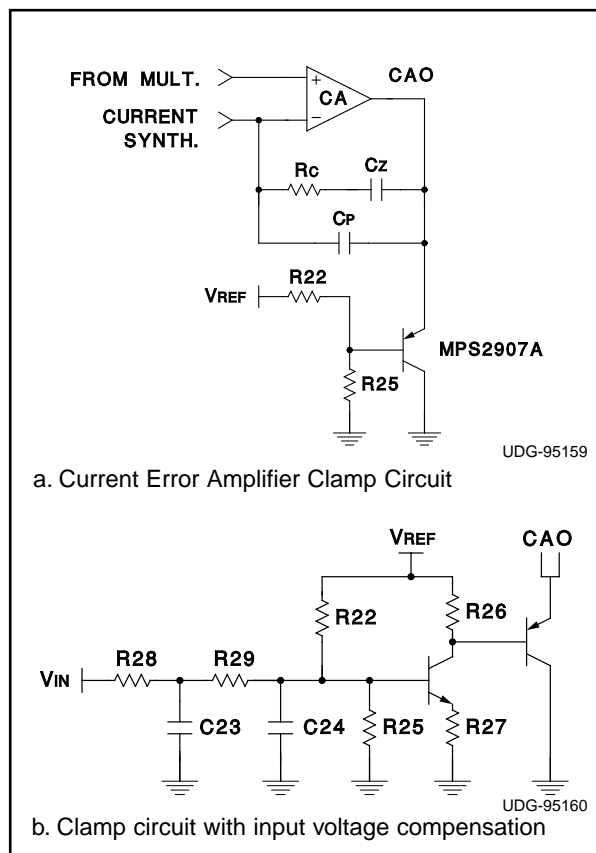


Figure 9. Clamp Circuit

In addition, if the current transformer saturates, the current limiting function will be lost. For these reasons it is recommended that the output of the current amplifier be clamped externally, to limit the maximum duty cycle. Figure 9 shows a typical clamp circuit.

The clamp circuit in Figure 9a will perform quite well (see Table 1), however if better performance is required, or if it's required to operate over a wide line range, the circuit in Figure 9b can be used. This circuit adjusts the clamp voltage to be inversely proportional to line voltage.

The procedure for setting the clamp voltage is quite easy. If during initial startup the current amplifier clamp is set to a relatively low value ($\approx 4\text{V}$) the system will operate but with excessive zero crossing distortion. Once the system is operating, the clamp voltage can be increased until the current transformer is not saturating, and line current has an acceptable level of THD. Once the clamp voltage is set, operation with other ICs will be repeatable. In the experimental breadboard built for universal line operation and 500W output, the single stage clamp was set to 5.6V (at low line and maximum load) and an acceptable level ($< 10\%$) of THD was measured over all line and load conditions. The clamp volt-

age is being set below the peak of the PWM comparator ramp (nominally 6.5V) to limit D_{MAX} . Setting the clamp voltage too low will cause excess zero crossing distortion due to the amplifier not being able to command enough line current.

Figures 10a and 10b show the current amplifier operation with and without the clamp, while Figure

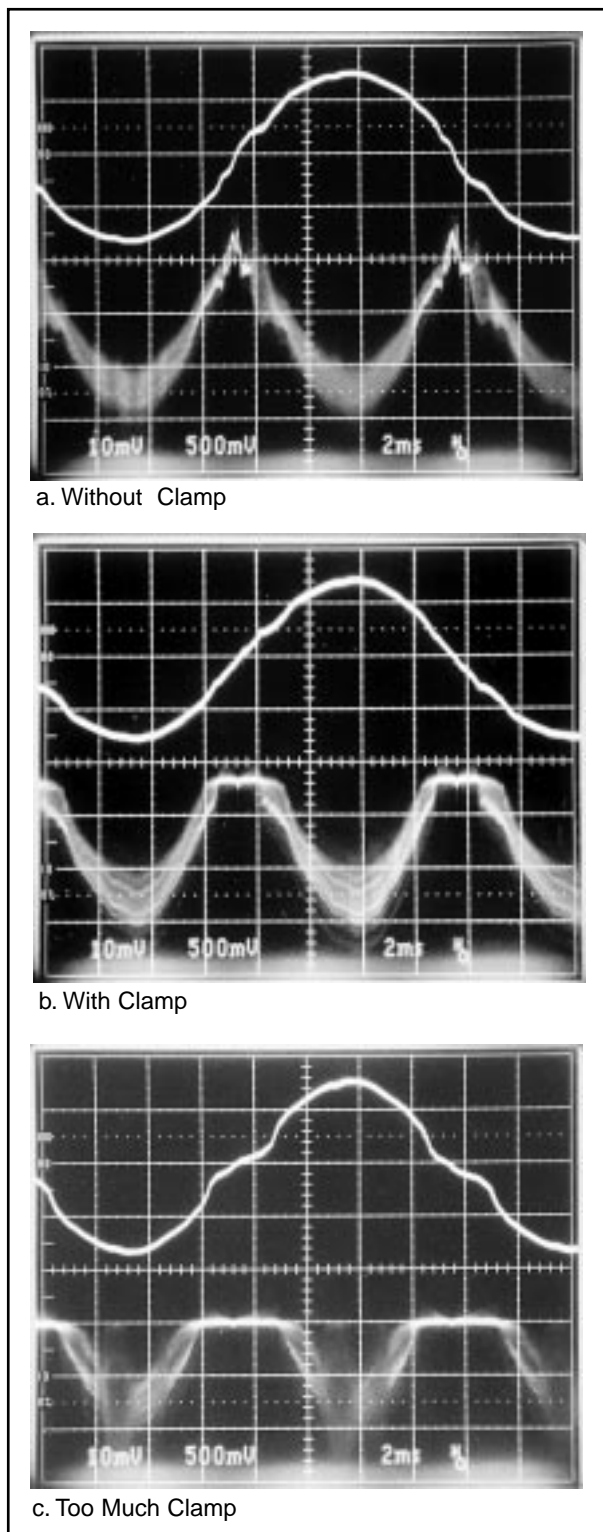


Figure 10. C/A Clamp Circuit Effects on I Line

10c shows the effect of clamping the amplifier output voltage too low (top waveform is line current, bottom is V_{CAO}). Setting the clamp too high will have the same effect as having no clamp.

The procedure for setting the two stage clamp circuit is the same except that the voltage contribution from the line must be factored in. The line voltage will only have to contribute 100mV to 200mV of clamp voltage for line compensation.

At very light or no load conditions, the average current drawn from the line is lower than can normally be commanded by the current error amplifier. To prevent an overvoltage condition from occurring, the IC goes into a pulse skipping mode if the output voltage of the error amplifier goes below $\approx 1V$. Pulse skipping can also occur at high line and low load conditions. When C_{AO} goes below 1V, the pulse skipping comparator is activated. The output of the comparator goes to an input of an OR gate in the OVP/ENABLE circuit, causing the output of that OR gate to go high. This signal prevents the ZVT and main gate drives from going high.

The procedure for compensating the current error amplifier will be covered in the Design Procedure section (IV).

Voltage Error Amplifier

The output voltage is sensed by the V_{SENSE} input to the voltage error amplifier and compared to an internally generated reference of 3V. The output of the amplifier, V_{EA} , (at a given input voltage) will vary proportionally with output power. The output voltage range for the voltage error amplifier is approximately 0.1V to 6V. The output of the amplifier is one of the multiplier inputs, and an input voltage below 1.5V will inhibit the multiplier output. The design procedure for compensating the voltage loop will be outlined in the Design Procedure section.

Protection Circuitry

OVP/ENABLE

The UC3855A/B combines the enable and OVP function into one pin. It requires a minimum of 1.8V to enable the IC, and below this voltage, the reference is held low and the oscillator is disabled. A voltage above 7.5V will interrupt the gate drive. The resistor divider should be sized for 7.5V when an over voltage condition is reached, this will allow startup at a reasonable line voltage. For example, if an overvoltage condition is defined as an output voltage exceeding 450V, then the voltage divider from V_{OUT} to the OVP pin is 60:1. This divider will allow startup at a line voltage of $76V_{RMS}$ ($108V_{PK}$).

Current Limit

The UC3855A/B has pulse by pulse current limiting. The multiplier power limit determines the maximum average power drawn from the line. However, during transients or overload conditions, a peak current limiting function is necessary. This function is implemented by sensing the switch current and feeding this value into ION, to a current limiting comparator that terminates the gate drive signal if the switch current signal exceeds 1.5V (nominal).

Soft Start

In order to ensure a smooth, controlled startup, the UC3855A/B provides a soft-start (SS) function. The SS pin sources 1.5μA into an external capacitor. This capacitor limits the supply voltage to the voltage loop error amplifier, which effectively limits the output voltage of the amplifier and therefore the maximum commanded output voltage. This allows the output voltage to ramp up in a controlled fashion.

Undervoltage Lockout

The UC3855A has a 15.5V (nominal) turn-on threshold with 6V of hysteresis while the UC3855B turns on at 10.5V with 0.5V of hysteresis.

TYPICAL APPLICATION

A typical application will be designed in order to illustrate the design procedure and highlight the design parameters that need to be defined. The design specifications are:

- $V_{IN} = 85 - 270 \text{ VAC}$
- $V_O = 410 \text{ VDC}$
- $P_{omax} = 500\text{W}$
- $F_S = 250\text{kHz}$
- $\text{Eff} > 95\%$
- $\text{Pf} > 0.993$
- $\text{THD} < 12\%$

The above specifications represent a common universal input voltage, medium power application. The switching frequency of 250kHz is now possible due to the soft switching, zero voltage transitions. The Pf and THD numbers correspond to achievable line correction with the UC3855.

Design Procedure

This design procedure is a summary of what was presented in [8]. However, several values have been changed in order to consolidate component values and/or specify more readily available parts.

1. Power Stage Design

Inductor Design

The power stage inductor design in a ZVT converter is identical to the conventional boost converter. The inductance required is determined by the amount of switching ripple desired, and allowing more ripple will reduce the inductor value. The worst case for peak current occurs at low line, maximum load. Peak power is equal to twice the average power and V_{PK} is $\sqrt{2} V_{RMS}$. To calculate input current, assume an efficiency of 95%.

$$I_{PK} = \frac{2 \cdot P_{IN}}{\sqrt{2} \cdot V_{INmin}} = \frac{\sqrt{2} \cdot \left(\frac{500}{0.95} \right)}{85}$$

$$= 8.7\text{A (60Hz component)}$$

A good compromise between current ripple and peak current is to allow a 20% ripple to average ratio. This will also keep the peak switch current less than 10A.

$$\Delta I_L = 0.2 \cdot (8.7\text{A}) = 1.7\text{A}_{pp}$$

Rearranging the conversion ratio for the boost converter to solve for D yields :

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{410 - \sqrt{2} \cdot 85}{410} = 0.71$$

We can now calculate the required inductance.

$$L = \frac{V_{IN} \cdot D \cdot T_S}{\Delta I} = \frac{\sqrt{2} \cdot 85\text{V} \cdot (0.71 \cdot 4\mu\text{s})}{1.7\text{A}}$$

$$= 200\mu\text{H}$$

Output Capacitor Selection

The value of output capacitor effects both hold-up time and output voltage ripple. If hold up time (t_H) is the main criteria, the following equation will give a value for C_O :

$$C_O = \frac{2 \cdot P_O \cdot t_H}{V_O^2 - V_{MIN}^2}$$

In this example a compromise between holdup time and capacitor size was made and a capacitor value of 440μF was selected. The capacitor bank consists of two 220μF, 450V DC capacitors in parallel.

Power MOSFET & Diode Selection

The main MOSFET selected is an Advanced Power Technology's APT5020BN (or equivalent). This is a

500V, 23A device, with $R_{DS(on)} = 0.20\Omega$ (25°C) and $C_{OSS} \approx 500\text{pF}$ in a TO-247 package. A 5.1 Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn-on with a Schottky diode and 2.7 Ω resistor in parallel with the resistor to speed up turn-off. A Schottky is also placed from GTOUT to ground to prevent the pin from being driven below ground, and should be placed as close to the IC as possible.

The boost diode selected is the International Rectifier HFA15TB60, a 15A, 600V ultrafast diode (or equivalent). Recall that a converter employing ZVT benefits from soft switching of the diode. With ZVT, the boost diode has a negligible impact on switching losses, and therefore a slower diode could potentially be used. However, there are still valid reasons for using an ultra fast diode in this application.

The ZVT inductor is sized according to the recovery time of the diode, and a slower diode will require a larger inductor. This will require a correspondingly longer Q_{ZVT} on-time, which increases conduction loss. A larger inductor will also require a longer time to discharge. To ensure complete discharge of the resonant inductor, the main switch minimum on-time should be approximately equal to the ZVT circuit on-time. This yields:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T}$$

D_{MIN} effects the minimum allowable output voltage for the boost converter to continue operating. The ZVT circuit on-time is a strong function of t_{rr} , and therefore choosing an ultra fast diode will keep the resonant circuit losses to a minimum and cause the least impact on the output voltage. The effective system duty cycle is primarily a function of the main switch on-time, since for a large portion of the resonant circuit's on-time, the voltage at the anode of the boost diode is held up by the resonant capacitor.

These considerations suggest a diode with a recovery time less than 75ns. Average output current in this design is less than 1.2A with a peak current of 9.2A. The conduction loss associated with the diode is approximately 2.2W.

While an ultra fast diode is being used, the diode is operating with significantly reduced switching losses. This will increase the overall system efficiency and reduce the peak stress of the diode.

2. ZVT Circuit Design

Resonant Inductor

The ZVT circuit design is straightforward. The circuit is performing an active snubber function and,

as such, the inductor is designed to provide soft turn off of the diode. The ZVT capacitor is selected to provide soft switching of the MOSFET.

The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the ZVT switch turns on, the input current is diverted from the boost diode to the ZVT inductor. The inductor value can be calculated by determining how fast the diode can be turned off. The diode's turn-off time is given by its reverse recovery time. Calculating an exact value for L_r is difficult due to the variation in reverse recovery characteristics within the actual circuit as well as variations in how reverse recovery is specified from manufacturer to manufacturer. An example of circuit conditions effecting the reverse recovery is the natural snubbing action of the resonant capacitor, which limits the dv/dt at the anode of the diode. A good initial estimate is to allow the inductor current to ramp up to the diode current within three times the diode's specified reverse recovery time. One constraint on the maximum inductance value is its affect on the minimum duty cycle. As was shown in the diode selection section, the L-C time constant effects D_{MIN} and therefore V_{Omin} . Making L_r too large will also increase the conduction time of the ZVT MOSFET, increasing the resonant circuit conduction losses. As the value of L_r is reduced, the diode will experience more reverse recovery current, and the peak current through the inductor and ZVT MOSFET will increase. As the peak current is increased, the amount of energy stored in the inductor will also increase ($E = 1/2 \cdot L \cdot I^2$). This energy should be kept to a minimum in order to reduce the amount of parasitic ringing in this node at turn-off.

The reverse recovery of the diode is partially a function of its turn-off di/dt . If a controlled di/dt is assumed, the reverse recovery time of this diode can be estimated to be approximately 60ns. If the inductor limits the rise time to 180ns ($3 \cdot t_{rr}$), the inductance can be calculated.

$$\frac{di}{dt} = \frac{I_{INp}}{3 \cdot t_{rr}} = 53A/\mu\text{s}$$

$$I_{INp} = I_{pk} + \frac{1}{2} \Delta I$$

$$L_r = \frac{V_O}{di/dt} = \frac{410V}{53A/\mu\text{s}} = 7.7\mu\text{H}$$

The inductor design is limited by core loss and resultant temperature rise, not saturating flux density. This is due to the high AC current component and the relatively high operating frequency. A good design procedure is outlined in [10] and is beyond

the scope of this review. Several points will be mentioned however. The core material should be a good high frequency, low loss material such as gapped ferrite or molypermalloy powder (MPP). Powder iron cores will generally not be acceptable in this application. The less expensive Magnetics Kool Mu material, although exhibiting higher losses than the MPP material, can also be used. The higher loss material will actually tend to damp the resonant ringing at the turn off of the ZVT switch. The inductor winding construction is also optimized by keeping interwinding capacitance to a minimum. This reduces the node capacitance at turn off and reduces the amount of damping required.

The inductor current can be found by analyzing the resonant circuit formed by L_r and C_r and recognizing that the resonant cycle begins when the current reaches I_{IN} .

$$I_{L_r} = I_{IN} + \frac{V_O}{Z_n} \cdot \sin\omega t$$

$$\text{where } Z_n = \sqrt{L_r/C_r}, \quad \omega = \sqrt{\frac{1}{L_r \cdot C_r}}$$

The peak current then is equal to I_{IN} plus the output voltage divided by the resonant circuit's characteristic impedance. Decreasing L_r or increasing C_r will increase the peak current. The inductor was designed using a Magnetics, Inc. MPP core 55209 with 33 turns for an inductance of $8\mu\text{H}$. The inductor should be constructed with Litz wire or several strands of small magnet wire to minimize high frequency effects.

Resonant Capacitor

The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The APT5020BN has approximately 500pF of output capacitance, and an external capacitance of 500pF was added across the device. This capacitor limits the dv/dt at turn-off and consequently reduces the Miller effect. In addition, it reduces turn-off losses since the switch current is diverted to the capacitor. The capacitor must be a good high frequency capacitor, and low ESR and ESL are required. It must also be capable of handling the relatively large charging current at turn-off. Two good choices are polypropylene film or a ceramic material.

This combination of L and C yields a resonant quarter cycle of:

$$\frac{\pi}{2} \sqrt{L_r \cdot C_r} = 140\text{ns}$$

The resonant circuit's impact on the output voltage can now be calculated. Recall that to ensure discharge of the resonant inductor at high line:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T} \quad (1)$$

and for a boost converter:

$$V_{O_{MIN}} = \frac{V_{INpk}}{1 - D_{MIN}} \quad (2)$$

Substituting (1) into (2) and solving for V_O produces:

$$V_{O_{MIN}} = \frac{(L_r \cdot I_{INp} + V_{INp} \cdot T)}{\left(T - t_{rr} - \frac{\pi}{2} \cdot \sqrt{L_r \cdot C_r}\right)} \quad (3)$$

Equation (3) can be solved using the previously established values and yields a minimum output voltage of 405V. This suggests a design value of 410V for V_O .

ZVT Switch and Rectifier Selection

The ZVT switch also experiences minimal turn-on loss due to the discharge of its drain-to-source capacitance. However, it doesn't experience high current and voltage overlap since the turn-on current is limited by the resonant inductor. The switch does experience turn-off and conduction losses however. Although the peak switch current is actually higher than the main switch current, the duty cycle is small, keeping conduction losses low. The ZVT switch will be one or two die sizes smaller than the main switch due to the low average drain current. The ZVT switch on-time is :

$$t_{ZVT} = \frac{I_{INp} \cdot L_r}{V_O} + \frac{\pi}{2} \cdot \sqrt{L_r C_r}$$

The peak ZVT switch current is equal to the peak ZVT inductor current. A conservative approximation of the switch RMS current is made by assuming a square wave signal. The RMS of the current is approximated by:

$$I_{RMS} \approx I_{L_{pk}} \cdot \sqrt{\frac{t_{ZVT}}{T}}$$

This corresponds to a peak of approximately 14A at maximum load and maximum ZVT on-time, however, the RMS is only 3.9A. An appropriate device in this application is the Motorola MTP8N50E, a 500V, 8A device with an $R_{DS(ON)}$ of 0.8Ω . As with the main MOSFET, a 5.1Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn on and a Schottky diode and resistor is placed in parallel with the resistor to speed up turn-off. A Schottky is also placed from ZVTOUT to ground to

prevent the pin from being driven below ground. This diode should be placed as close to the IC as possible.

The rectifiers needed for the ZVT circuit also experience relatively low RMS current. Diode D2 returns the energy stored in the resonant inductor during t_{ZVT} to the load. D2 should be an ultra-fast recovery diode and is usually chosen to be of similar speed as D1. The diode selected for D2 is a Motorola MURH860; a 600V device with a $t_{rr} \approx 35\text{ns}$.

Diode D3 blocks current from flowing up through the Q_{ZVT} body diode when the inductor resets, it sees the same peak and RMS current as Q_{ZVT} . D3 should be a fast recovery diode to decouple the drain to source capacitance of Q_{ZVT} from the resonant inductor. Energy stored in the D3 anode node capacitance will resonate with the ZVT inductor when the ZVT switch turns off. Minimizing this effect will reduce the amount of snubbing required at this node. The diode chosen here was the MUR460. This is a 600V, 4 amp device with $t_{rr} \approx 75\text{ns}$.

To summarize, both diodes in the ZVT circuit experience low RMS current. The main selection criteria in addition to the blocking voltage (in both cases equal to V_O) is reverse recovery time. Choosing devices with fast recovery times will reduce parasitic oscillations, losses, and EMI.

ZVT Snubber Circuit

The ZVT circuit requires some method for damping the parasitic oscillations that occur after the ZVT inductor current goes to zero. Figure 10a shows the ZVT inductor current and diode D2 anode voltage without adequate damping. The figure shows that as the inductor current begins to discharge (when Q_{ZVT} turns off) to the output, the anode volt-

age is at V_{OUT} (since D2 is conducting). As the inductor current passes through zero, the voltage rings negative since the opposite end of the inductor is clamped to 0V through the main switch body diode. The anode voltage can easily ring negatively to twice the output voltage. This increases the reverse voltage stress on the diode to three times the output voltage! Keeping the energy in the node capacitance to a minimum and using fast recovery diodes will reduce the ringing and improve the circuit performance.

Several methods of damping this oscillation have been proposed [4,7]. In this circuit two methods, the saturable reactor and resistive damping were investigated. A 51Ω , 10W noninductive resistor was connected through a diode from ground to the anode of D2. The saturable reactor was placed in series with the resonant inductor and implemented with 8 turns on a Toshiba saturable core SA 14 x 8 x 4.5. The resistive damping method prevents the node from oscillating. However, it does not prevent current from flowing in D2 while D1 is conducting (due to the dv/dt across L_r when Q_{MAIN} turns off). If current flows through D2 during this time it will experience reverse recovery current when Q_{ZVT} turns on. The saturable reactor prevents this current flow due to its high impedance. L_S also decouples L_r from the node capacitance, which prevents the node from oscillating.

The saturable reactor works well without the resistive damping and was the method chosen in this design. With the saturable reactor damping the circuit properly, the resistive damping can be eliminated. However, since L_S is designed to saturate each switching cycle, the core loss is largely material dependent and can cause significant temperature

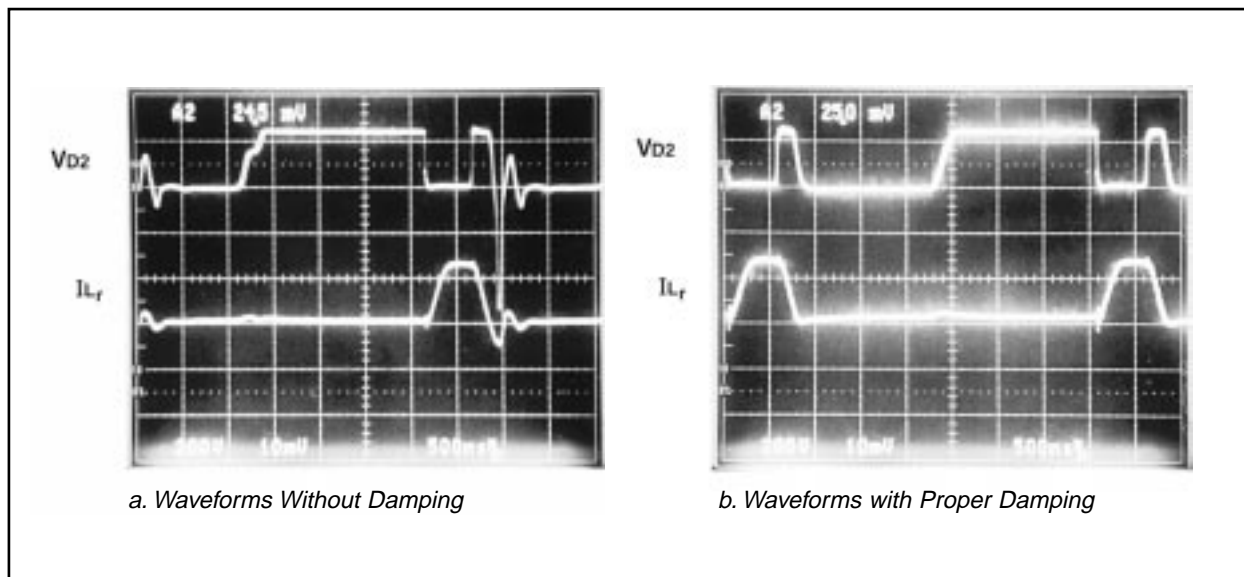


Figure 11. ZVT Ringing Waveforms

rise of the core. In this circuit, heatsinking of the core was required. An alternative design was also tried using the larger MS 18 x 12 x 4.5 which ran cooler although it also required heatsinking. Optimization of this circuit can significantly reduce the losses in the ZVT circuit. In this design, damping network losses were approximately 2W. Figure 10b shows the same circuit condition with the node damped with L_S .

ZVS Circuit

The ZVS circuit components are chosen next. In this example, a 1k Ω resistor is used to pull up the ZVS pin. The capacitor chosen is 500pF. This combination will require approximately 200ns to charge up to the 2.5V threshold.

$$t = -R \cdot C \cdot \ln \left(\frac{1 - V_{\text{THRESHOLD}}}{V_{\text{REF}}} \right)$$

3. Oscillator Frequency

Calculate CT:

The switching frequency selected is 250kHz.

$$CT = \frac{1}{11200 \cdot 250\text{kHz}} = 357\text{pF, use } 330\text{pF}$$

4. Multiplier/Divider Circuit

Calculate the VRMS resistor divider:

Set VRMS = 1.5V at low line (85VRMS)

$$\text{divider} = \frac{85V_{\text{RMS}} \cdot 0.9}{1.5 V_{\text{DC}}} = 51:1$$

The voltage divider can be solved if one of the resistors is defined (since there are two equations and three unknowns). Letting the lower resistor in the divider = 18k Ω :

$$R_{\text{TOTAL}} = 18\text{k}\Omega \cdot 51 = 918\text{k}\Omega$$

Letting R10 = 120k Ω , gives:

$$R9 = 918\text{k}\Omega - 120\text{k}\Omega - 18\text{k}\Omega = 780\text{k}\Omega$$

R9 is split into two resistors (each 390k Ω) to reduce their voltage stress.

Calculate the capacitor values to place the filter poles at 18Hz:

$$C5 = \frac{1}{2\pi \cdot f_p \cdot R_{11}} = \frac{1}{2\pi \cdot 18\text{Hz} \cdot 18\text{k}\Omega} \\ = 0.49\mu\text{F, use } 0.47\mu\text{F}$$

$$C4 = \frac{1}{2\pi \cdot f_p \cdot R_{\text{eq}}} = \frac{1}{2\pi \cdot 18\text{Hz} \cdot 117\text{k}\Omega} \\ = 75\text{nF, use } 0.082\mu\text{F}$$

where $R_{\text{eq}} = R9 || (R10 + R11) = 117\text{k}\Omega$

In order to consolidate capacitor values C4 could be chosen to be 0.1 μF without degrading the system performance.

Calculate the IAC resistor:

Set $I_{\text{IAC}} = 500\mu\text{A}$ at high line.

$$R = \frac{\sqrt{2} \cdot 270\text{V}}{500\mu\text{A}} = 764\text{k}\Omega$$

Use 2, 390k Ω resistors in series to reduce voltage stress.

Calculate R_{IMO} :

At low line $I_{\text{IAC}} = 156\mu\text{A}$ and the output of the multiplier should equal 1V. With low line and maximum load, V_{EA} will be at its maximum of 6V, therefore, using the multiplier output equation:

$$\frac{1\text{V}}{R_{\text{IMO}}} = \frac{I_{\text{IAC}} \cdot (V_{\text{EA}} - 1.5)}{V_{\text{VRMS}}^2}$$

$$R_{\text{IMO}} = \frac{1.5^2}{156\mu\text{A} \cdot (6 - 1.5)} = 3.2\text{k}\Omega, \text{ use } 3.3\text{k}\Omega$$

A 1000pF capacitor is placed in parallel with R_{IMO} for noise filtering. Since the voltage across R_{IMO} is the output of the multiplier and is the reference for the current error amplifier, the RC pole frequency should be placed well above the 120Hz multiplier signal.

5. Current Synthesizer

First, chose a turns ratio for the current transformer. The current transformer is designed to produce 1V at peak input current. This allows sufficient margin before the current limit trip point (1.4V) is reached. If $I_{\text{PK}} = 9.5\text{A}$ a turns ratio of 50 : 1 would be appropriate. This turns ratio will keep the sense network losses less than 150mW and allow the use of a 1/4 watt resistor. Solving for the sense resistor yields:

$$R_S = \frac{1\text{V}}{\frac{I_{\text{sw}}}{N}} = \frac{1\text{V}}{\frac{9.5}{50}} \approx 5.1\Omega$$

Recall from the previous current synthesizer section that $R_{\text{VS}} = 22\text{k}\Omega$. The current synthesizer capacitor can now be calculated:

$$C_I = \frac{3 \cdot L \cdot N}{R_{\text{VS}} \cdot V_{\text{OUT}} \cdot R_S} \\ = \frac{3 \cdot 200\mu\text{H} \cdot 50}{22\text{k}\Omega \cdot 410\text{V} \cdot 5.1\Omega} = 633\text{pF, use } 680\text{pF}$$

6. Control Loop Design

Small Signal Model

The small signal model of the ZVT PFC boost converter is similar to the standard PFC boost converter model. The two converters operate exactly the

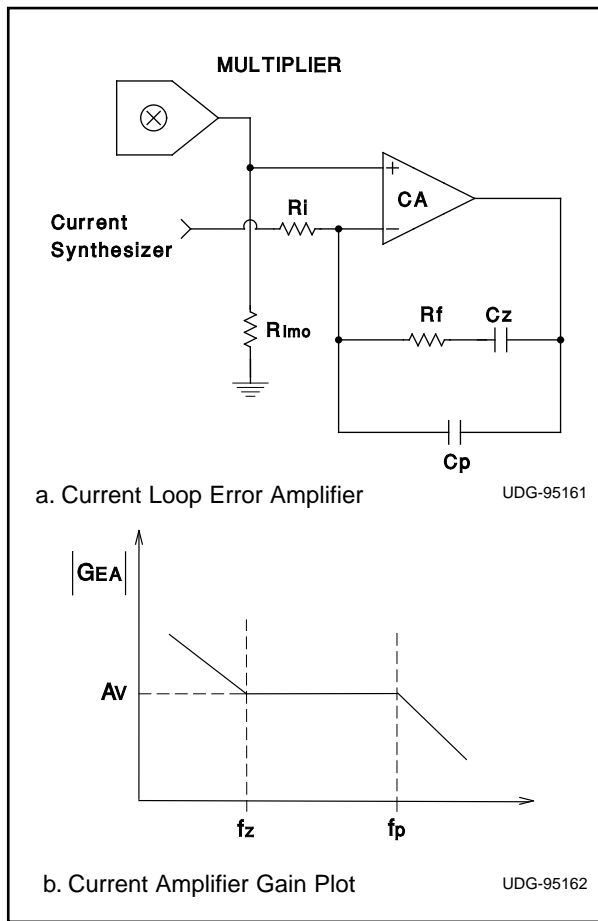


Figure 12. Current Error Amplifier Schematic

same throughout most of the switching cycle and only during the switching transitions is there any difference. This allows the design of the control loops to proceed following the standard techniques outlined in [9].

Current Loop Design

Excellent references on the current loop design are found in [5,9,11]. The design of the average current mode control loop begins with choosing a cross-over frequency. In this example the switching frequency is 250kHz, so the unity gain cross over frequency could be chosen to be as high as 40kHz (1/6 of the switching frequency). In this circuit however, the cross over is chosen to be 10kHz. Since the main job of the current loop is to track the line current, a 10kHz bandwidth is quite adequate for this application.

Once the cross over frequency (f_c) is known, the next thing to do is calculate the gain of the power stage. The small signal model of the power stage

including the current sense network is given below. This model does not include the sampling effect at one half the switching frequency [12] but is a good approximation at the frequencies of interest.

$$G_{id}(s) = \frac{V_O \cdot R_{SENSE}}{s \cdot L \cdot V_{SE}}$$

The UC3855A/B has an oscillator ramp of $5.2V_{pp}$ (V_{SE}). The R_{SENSE} term, is the attenuation from actual input current to sensed current (i.e. it includes the current transformer turns ratio). Using the previously determined component values and solving for the power stage gain at f_c yields a gain of 0.63 at 10kHz. In order to have a gain of 1 at f_c , the error amplifier must have a gain of 1/0.63 at 10kHz. The error amplifier is shown in Figure 12a with the frequency response in Figure 12b. The resistor R_i is equal to $3.3k\Omega$ so the feedback resistor is chosen to be $5.6k\Omega$. A zero is placed at the cross over frequency to give a phase margin of 45 degrees. To reduce switching noise a pole is placed at one-half the switching frequency. The following summarizes the design procedure.

$$1. |G_{id}(s)| = \frac{410V \cdot 0.10}{2 \cdot \pi \cdot 10kHz \cdot 200\mu H \cdot 5.2} = 0.63$$

$$2. G_{EA} = \frac{1}{|G_{id}(s)|} = 1.58 \Rightarrow Av = \frac{R_f}{R_i}$$

$$\therefore R_f = \frac{R_i}{|G_{id}(s)|} \approx 5.6k\Omega$$

$$3. f_z = f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_z}$$

$$C_z = \frac{1}{2 \cdot \pi \cdot 10kHz \cdot 5.6k\Omega} \approx 2200pF$$

$$4. f_p = \frac{1}{2 \cdot \pi \cdot R_f \left(\frac{C_z \cdot C_p}{C_z + C_p} \right)} = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_p}$$

$$C_p = \frac{1}{2 \cdot \pi \cdot 5.6k\Omega \cdot 125kHz} \approx 220pF$$

Voltage Loop Design

The design of the voltage loop follows the procedure given in [5]. The first step is to determine the amount of ripple on the output capacitor.

$$v_{Opk} = \frac{P_{IN} \cdot X_{Co}}{V_O}$$

$$V_{Opk} = \frac{525}{2 \cdot \pi \cdot 120 \cdot 410\mu \cdot 410} = 4.14V_{PK}$$

$$= 8.3V_{pp}$$

In order to meet the 3% THD specification, the distortion due to output ripple voltage feeding through the voltage error amplifier will be limited to 0.75%. This allows 1.5% from the multiplier and 0.75% from miscellaneous sources. A 1.5% second harmonic on the error amplifier will result in 0.75% 3rd harmonic distortion at the input. At full load, the peak error amplifier ripple voltage allowed is:

$$V_{EApk} = \% \text{ ripple} \cdot V_{VEA} = 0.015 \cdot (6 - 1)$$

$$= 0.075V$$

The error amplifier gain at 120Hz is the allowable error amplifier ripple voltage divided by the output ripple voltage, or 0.009 (-41 dB). The error amplifier input resistor was chosen to be 1.36MΩ to keep power dissipation low and allow a small value for the compensation capacitor. Two 681kΩ resistors in series are used to reduce the voltage stress. The voltage error amplifier schematic is shown in Figure 13, with the 120Hz gain determined by the inte-

grator function of C_f and R_i . This network has a single pole roll off and the capacitor value is easily found to give the desired gain at 120Hz.

$$C_f = \frac{1}{2 \cdot \pi \cdot f \cdot G_{VEA} \cdot R_i}$$

$$C_f = \frac{1}{2 \cdot \pi \cdot 120\text{Hz} \cdot 0.009 \cdot 1.36M\Omega}$$

$$\approx 0.1\mu F$$

The crossover frequency can now be calculated recognizing that a pole (due to the combination of C_f and R_f) will be placed at the cross over frequency to provide adequate phase margin. The pole placement will determine the phase margin since the power stage has a single pole response with the associated 90 degree phase lag. If the error amplifier pole is placed at the crossover frequency, the overall loop gain will have a 45 degree phase margin. The power stage gain is given by:

$$G_{PS}(s) = \frac{V_o}{V_{VEA}} = \frac{P_{IN}}{\Delta V_{EA} \cdot V_o \cdot (s \cdot C_o)}$$

The voltage loop gain (T_V) is the product of the power stage gain and the error amplifier gain. To find the cross over frequency, solve for f and set equal to 1.

$$T_V = 1 = G_{PS}(s) \cdot G_{VEA}(s)$$

The error amplifier gain is:

$$G_{VEA} = \frac{-j}{2 \cdot \pi \cdot f \cdot R_i \cdot C_f} = \frac{-j \cdot 1.17}{f}$$

$$\therefore T_V = 1 = \frac{-j \cdot 92.6}{f} \cdot \left(\frac{-j \cdot 1.17}{f} \right) = \frac{108}{f^2}$$

The cross over frequency then is approximately 11Hz, so the resistor, R_f , can be calculated to place the pole at f_c .

$$R_f = \frac{1}{2 \cdot \pi \cdot 11\text{Hz} \cdot 0.1\mu F} \approx 140k\Omega$$

Finally, the resistor R_D (10kΩ) sets the DC output voltage to 410V.

7. OVP/ENABLE

An output voltage exceeding 450V is defined as an overvoltage condition. To trip the OVP comparator at 450V requires a divider of:

$$\frac{7.5V}{450V} = 60:1$$

Letting the lower resistor in the divider = 33kΩ, the top resistor then is 2MΩ, two 1MΩ resistors are

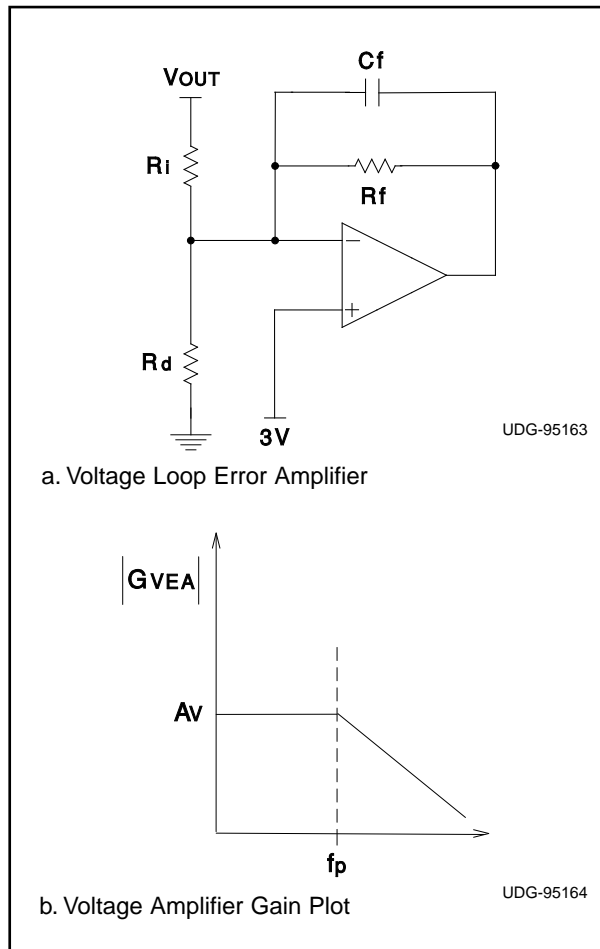


Figure 13. Voltage Error Amplifier

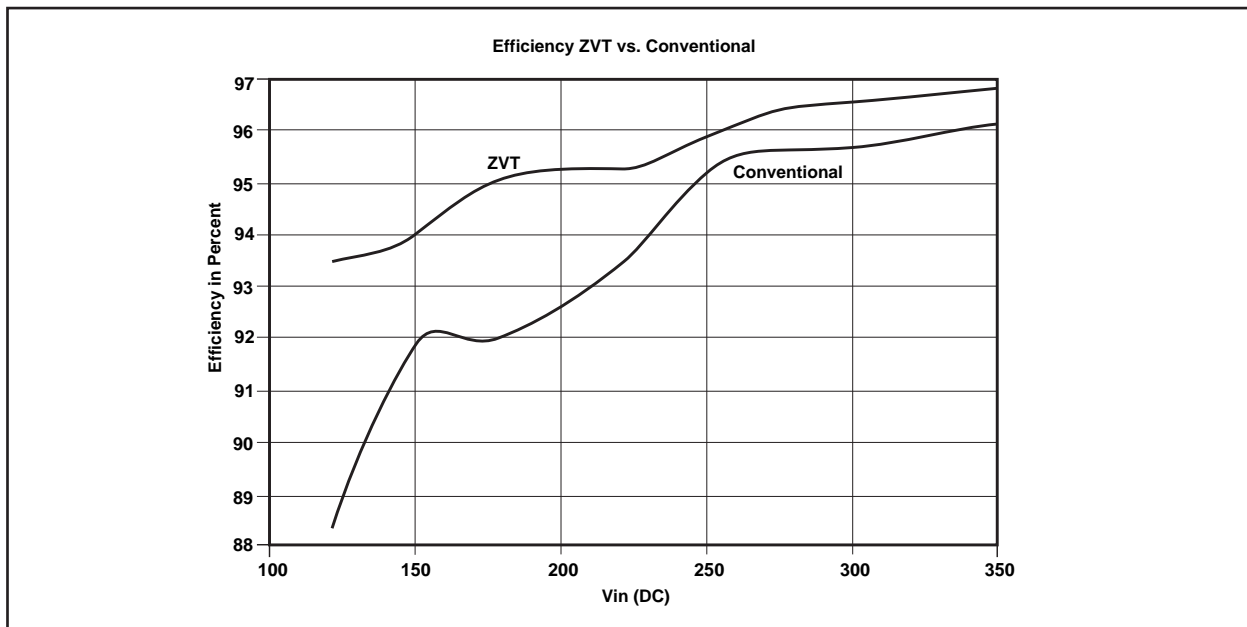


Figure 14. Efficiency Data

used in series to reduce the voltage stress. A 10nF capacitor is placed in parallel with the 33kΩ resistor for noise filtering.

With this divider the converter will start at 76V_{RMS}, which will allow startup well below low line.

EXPERIMENTAL RESULTS

The example converter was constructed to demonstrate circuit performance. The circuit performed well and was tested over the full line and load ranges.

Figure 14 shows efficiency data for the ZVT vs. a conventional boost converter, which was derived by simply removing the ZVT components. The conventional circuit needed to be cooled with a fan in order to stabilize the power semiconductor temperatures. It can be seen from the data that the ZVT circuit has a significant advantage over the conven-

tional converter at low line. At higher line voltages the advantage is reduced until the two power stages converge at high line. This is understandable and consistent with the other reported data [4,13]. At low line, the higher input current contributes to higher switching losses in the conventional converter. The ZVT converter however, does not experience increased switching losses (conduction losses increase for both converters at low line).

Figure 15 shows the ZVT and main switch gate drives as well as the main switch drain to source voltage. The ZVT gate drive goes high prior to the main switch and drives the drain voltage to zero before the main switch turns on. It should also be noted that the drain to source voltage waveform is very clean with no overshoot or ringing, which will reduce EMI and voltage stress on the device. The ZVT circuit waveforms are shown in Figure 16. Current in L_f is shown in the top trace. The wave-

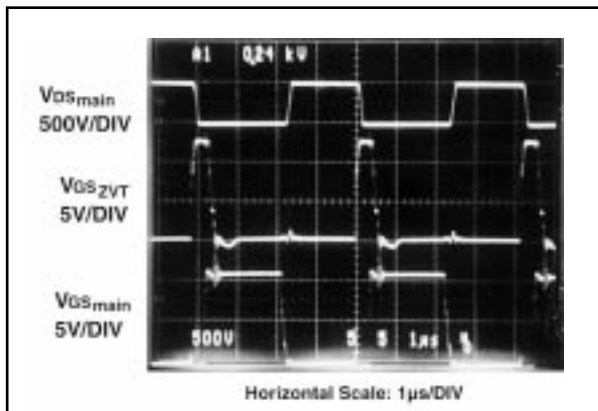


Figure 15. Power Stage Waveforms

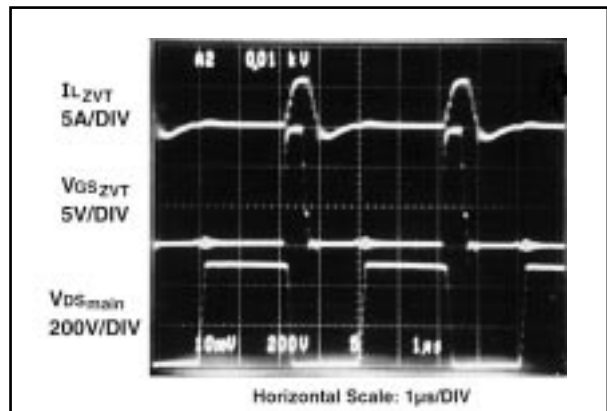


Figure 16. ZVT Waveforms

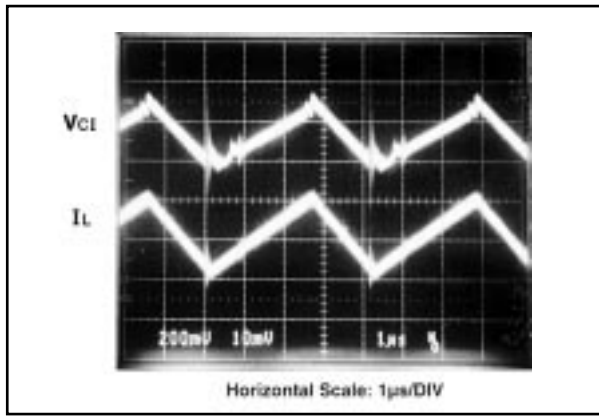


Figure 17. Current Synthesizer Waveforms

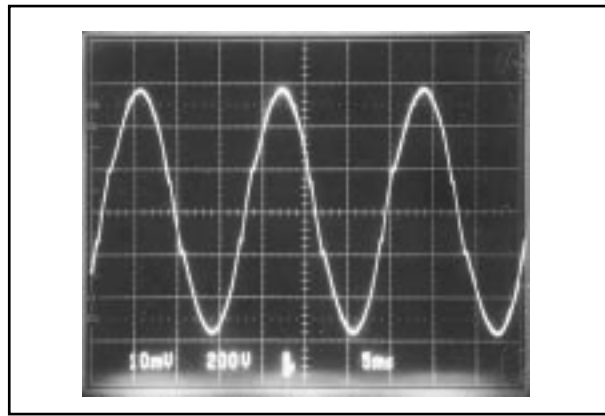


Figure 18. Line Current

forms are well damped with a peak current of approximately 6A. The current synthesizer waveforms are shown in Figure 17. The top waveform is the reconstructed waveform at CI and the bottom waveform is inductor current. The waveforms show good agreement. Any error between the reconstructed and actual waveform will be greatest at high line and is primarily caused by slight offset voltage errors in the synthesizer circuit.

Figure 18 shows the input line current at low line and maximum load, the THD and power factor are well within acceptable limits. Table 1 gives THD and pf measurements for several line and load conditions with the single stage current error amplifier clamp circuit. Table 2 shows THD and pf with the two stage clamp circuit shown in Figure 9B.

| Line(VAC) | % THD | Pf |
|-----------|-------|-------|
| 100 | 6.3 | 0.998 |
| 120 | 4.5 | 0.999 |
| 200 | 8.9 | 0.996 |
| 230 | 10 | 0.995 |

Table 1 THD and Pf vs. line, with single stage error amplifier clamp circuit.

| Line(VAC) | % THD | Pf |
|-----------|-------|-------|
| 100 | 4.95 | 0.999 |
| 120 | 5.30 | 0.998 |
| 200 | 5.45 | 0.998 |
| 230 | 5.83 | 0.998 |

Table 2 THD and Pf vs. line, with two stage error amplifier clamp circuit.

POWER STAGE COMPONENT VENDORS

| | |
|----------------------------------|---|
| L1,L2 | Magnetics, Butler, PA (412) 282-8282 |
| Spike Killer | Toshiba, Westboro, MA (508) 836-3939 |
| Q _{MAIN} | APT, Bend, OR (503) 382-8028 |
| D1 | International Rectifier, El Segundo, CA (310) 322-3331 |
| Q _{ZVT} , D2, D3, D4 | Motorola, Phoenix, AZ (602) 244-3550 |

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