UNITRODE

Programmable Hot Swap Power Manager

FEATURES

- Integrated 0.15 ohm Power MOSFET
- 3V to 8V Operation
- Digital Programmable Current Limit from 0 to 3A
- Electronic Circuit Breaker Function
- 1μA I_{CC} when Disabled
- Programmable on Time
- Programmable Start Delay
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC, Low Thermal Resistance Packaging

DESCRIPTION

The UCC3912 Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time,and start-up delay. In the event of a constant fault, the Internal fixed 3% duty cycle ratio limits average output power.

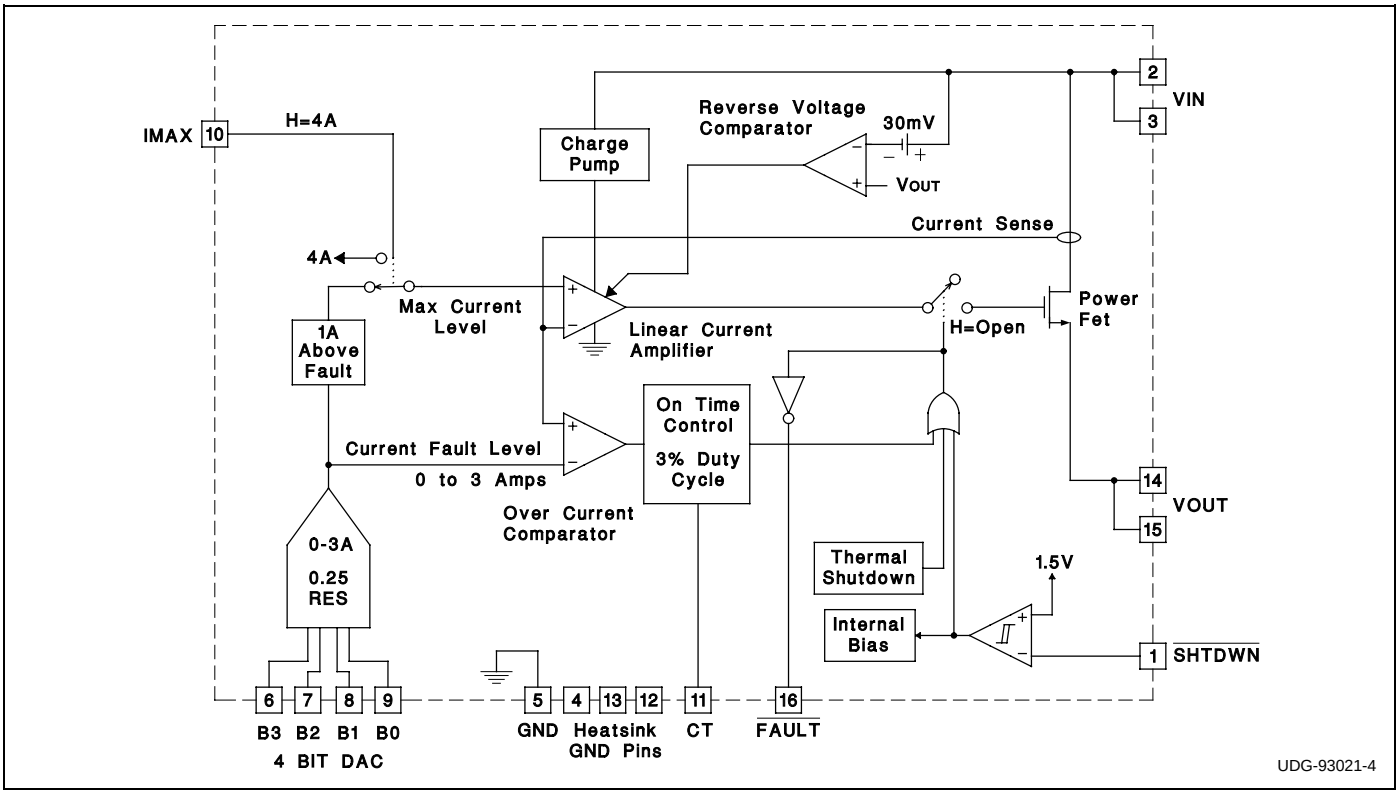
The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the fault level when driven low, and to a full 4A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15 ohms. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging C_T. Once C_T charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

The UCC3912 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI Termpwr.

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UCC3912 can be put into sleep mode drawing only 1µA of supply current. The $\overline{\text{SHTDWN}}$ pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon start-up to achieve sequencing of power. Other features include an open drain Fault output indicator, Thermal Shutdown, Under Voltage Lockout, and a low thermal resistance Small outline package.

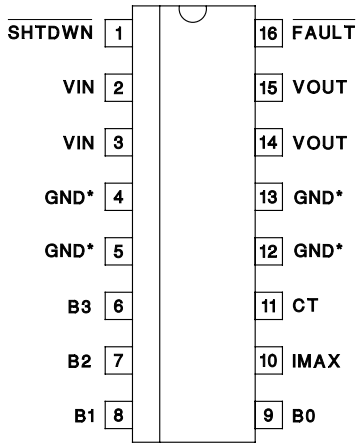
ABSOLUTE MAXIMUM RATINGS

$\overline{\text{VIN}}$ . . . . . +8 Volts
$\overline{\text{FAULT}}$ Sink Current 50mA
$\overline{\text{FAULT}}$ Voltage . . . . . –0.3 to V_{IN}
Output Current . . . . . Self Limiting
TTL Input Voltage . . . . . –0.3 to V_{IN}
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

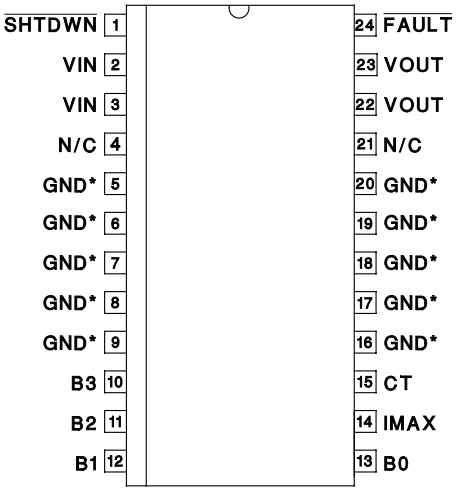
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
N, DP Package



***Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.**
For N Package, pins 4, 12, and 13 are N/C.

TSSOP-24 (Top View)
PWP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_J = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{\text{SHTDWN}}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		3.0		8.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	$\overline{\text{SHTDWN}}$ = 0.2V		0.5	5.0	µA
Output Section					
Voltage Drop	I_{OUT} = 1A		0.15	0.22	V
	I_{OUT} = 2A		0.3	0.45	V
	I_{OUT} = 3A		0.45	0.68	V
	I_{OUT} = 1A, VIN = 3V		0.17	0.27	V
	I_{OUT} = 2A, VIN = 3V		0.35	0.56	V
	I_{OUT} = 3A, VIN = 3V		0.5	0.8	V
Reverse Leakage	VIN < VOUT , VOUT = 5V		5	20	µA
Initial Start-up Time	Note 2		100		µs
Short Circuit Response	Note 2		100		ns
Thermal Shutdown	Note 2		170		°C
Thermal Hysteresis	Note 2		10		°C
DAC Section					
Output Leakage	Code = 0000-0011		0	20	µA
Trip Current	Code = 0100	0.1	0.25	0.45	A
	Code = 0101	0.25	0.50	0.75	A
	Code = 0110	0.5	0.75	1.0	A

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_J = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{SHTDWN}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC Section (cont.)					
	Code = 0111	0.75	1.00	1.25	A
	Code = 1000	1.0	1.25	1.5	A
	Code = 1001	1.25	1.50	1.75	A
	Code = 1010	1.5	1.75	2.0	A
Trip Current	Code = 1011	1.7	2.00	2.3	A
	Code = 1100	1.9	2.25	2.58	A
	Code = 1101	2.1	2.50	2.9	A
	Code = 1110	2.3	2.75	3.2	A
	Code = 1111	2.5	3.0	3.5	A
Max Output Current	Code = 0000 to 0011			0.02	mA
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 0V	0.5	1.0	1.8	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 2.4V	3.0	4.0	5.2	A
Timer Section					
CT Charge Current	V_{CT} = 1.0V	–45.0	–36.0	–27.0	µA
CT Discharge Current	V_{CT} = 1.0V	0.9	1.2	1.5	µA
Output Duty Cycle	V_{OUT} = 0V	2.0	3.0	6.0	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			100		mV
Input Current	$\overline{SHTDWN}$ = 1V		100	500	nA
Fault Output Section					
Output Leakage Current				500	nA
Low Level Output Voltage	I_{OUT} = 10mA		0.4	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High	(can be connected to V_{IN})	2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	V_{IH} = 2.4V		3	10	µA
TTL Input Low Current	V_{IL} = 0.4V			1	µA

Note 1: All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

B0 - B3: These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as FAULT = 27.8 • 10^3 • CT. Once the fault time is reached the output will shut-down for a time given by: T_{SD} = 833 • 10^3 • CT, this equates to a 3% duty cycle.

$\overline{FAULT}$: Open drain output which pulls low upon any condition which causes the output to open: Fault, Thermal Shutdown, or Shutdown.

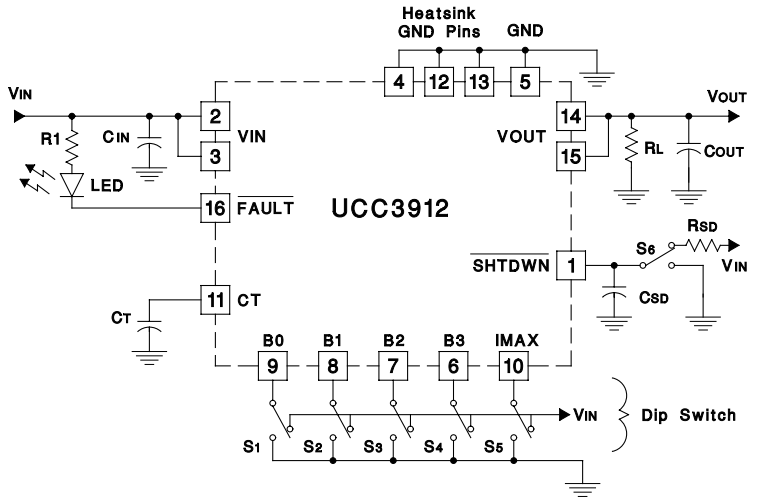
IMAX: When this pin is set to logic low the maximum sourcing current will always be 1A above the programmed fault level. When set to logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{SHTDWN}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 1µA of I_{CC}. The input threshold is hysteretic, allowing the user to program a start-up delay with an external RC circuit.

VIN: Input voltage to the UCC3912. The recommended voltage range is 3 to 8 volts. Both VIN pins should be connected together and to the power source.

VOUT: Output voltage from the UCC3912. When switched the output voltage will be approximately V_{IN} - (0.15Ω • I_{OUT}). Both VOUT pins should be connected together and to the load.

Evaluation Circuit



Note: For Demonstration Board Schematic see Design Note DN-58.

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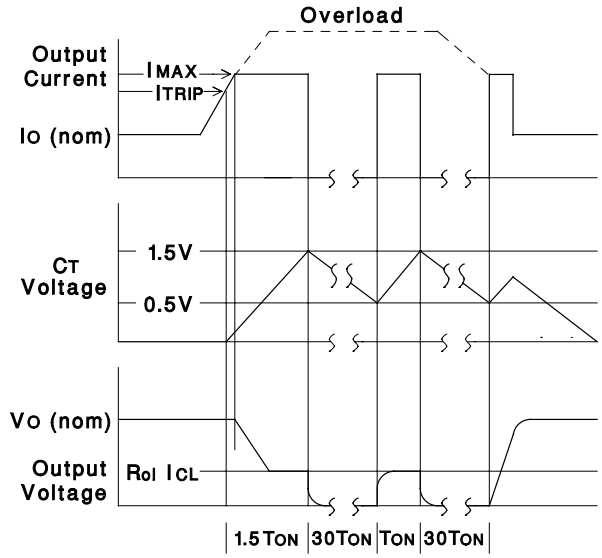
Load Current, Timing Capacitor Voltage, and Output Voltage of the UCC3912 under Fault Conditions.



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Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

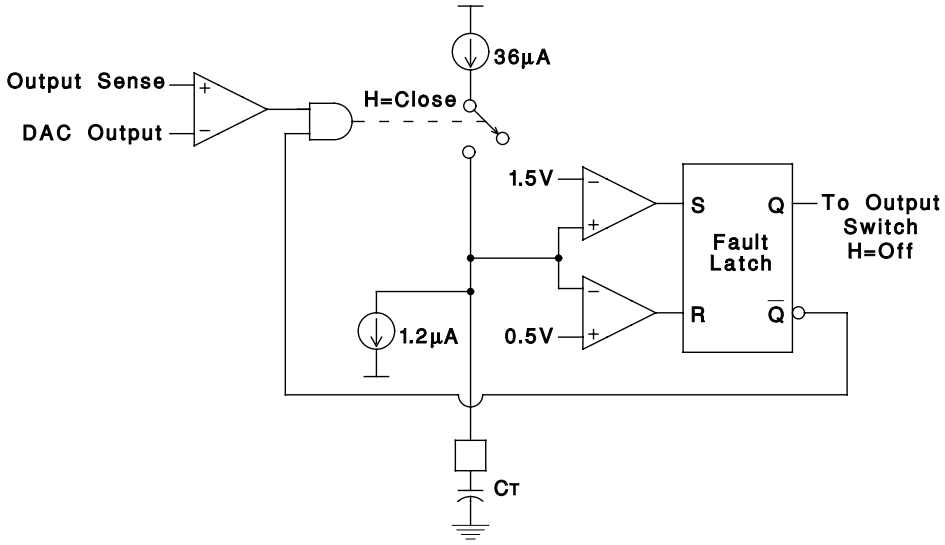
$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right) \bullet \ln$$

UCC3912 On Time Control Circuitry



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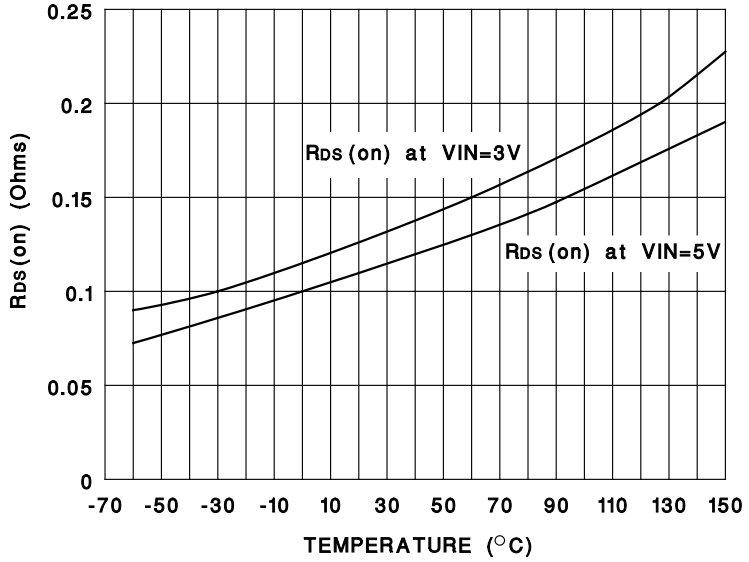
The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor C_T charges with 36µA of current. If the fault occurs for the time it takes for C_T to charge up to 1.5V, the fault latch is set and the output switch is opened. The output remains opened until C_T discharges to 0.5V with a 1.2µA current source. Once the 0.5V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present then C_T will begin charging, starting the cycle over, resulting in approximately a 3% on time.

RDS(on) vs Temperature at 2A Load Current



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SAFETY RECOMMENDATIONS

Although the UCC3912 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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