UNITRODE

UCC1917
UCC2917
UCC3917

Positive Floating Hot Swap Power Manager

PRELIMINARY

FEATURES

- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Programmable Fault Time
- Internal Charge Pump to Control External NMOS Device
- Fault Output and Catastrophic Fault Indication
- Fault Mode Programmable to Latch or Retry
- Shutdown Control
- Undervoltage Lockout

DESCRIPTION

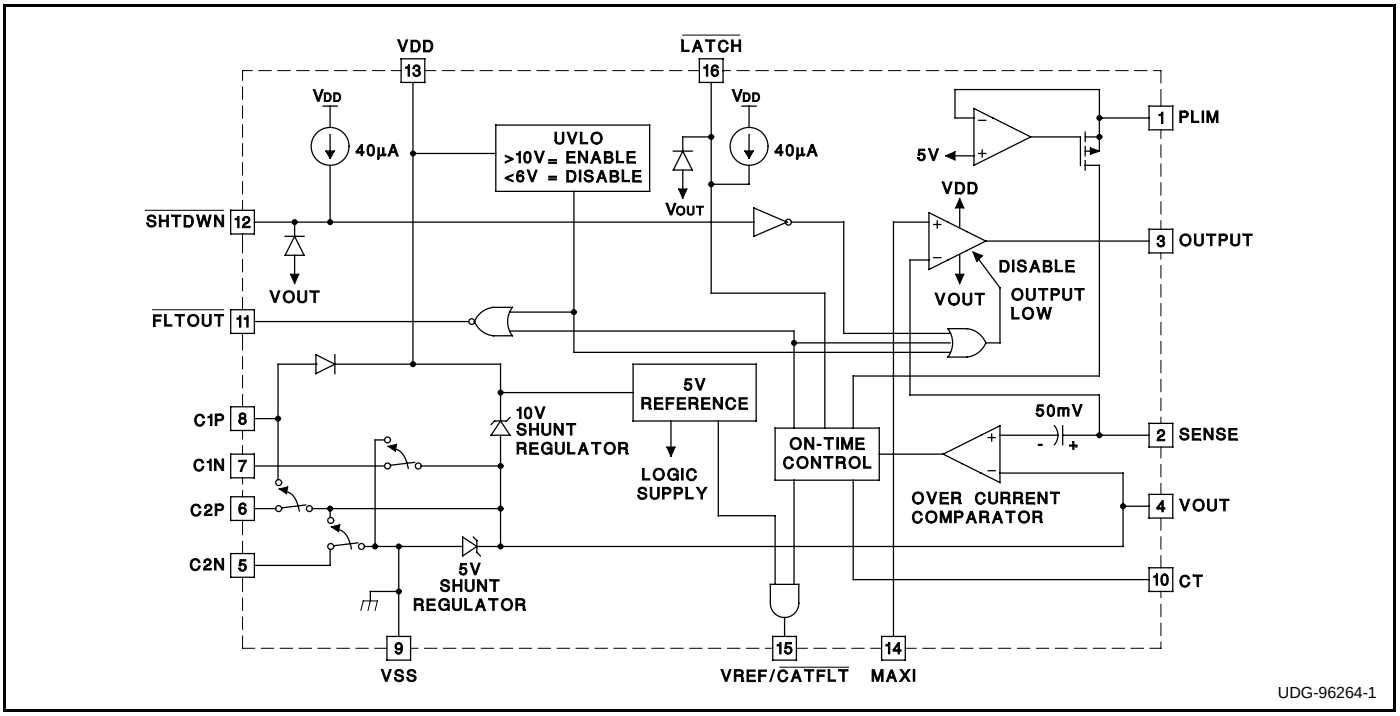
The UCC3917 family of positive floating hot swap managers provides for complete power management, hot swap, and fault handling capability for PC boards. The voltage limitation of the application is only restricted by the external component voltage limitation and not the IC. The IC provides it's own supply rail via a charge pump off of VOUT. The charge pump derives its power from the onboard 5V shunt regulator, and thus, IDD is provided by the output load. The onboard 10V shunt regulator protects the IC from excess voltage. The IC also has catastrophic fault indication to alert the user that the ability to shut off the output NMOS has been bypassed. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average NMOS power limiting. In the event of a constant fault, the internal timer will limit the on time/off time ratio from less than 0.1% to a maximum 3%, depending on the fault condition. In order to maintain constant average output power, the PLIM pin is provided to sense the drain voltage of the external NMOS through a resistor, and modulate duty cycle accordingly.

The fault level across the current sense amplifier is fixed at 50mV to minimize total drop out. Once 50mV is exceeded across the current sense resistor, the fault timer will start. The maximum allowable sourcing current is programmed with a voltage divider from the VREF/$\overline{\text{CATFLT}}$ pin to generate a fixed voltage on the MAXI pin. The current level at which the output appears as a current source is equal to V_{MAXI} divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on MAXI.

When the output current is below the fault level, the output device is switched on with full gate drive. When the output current exceeds the fault level, but is

Continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

less than maximum allowable sourcing level programmed by MAXI, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and attempts either a retry sometime later or waits for the state on the LATCH pin to charge if in latch mode. When the output current reaches the maximum sourcing current level, the output device appears as a current source.

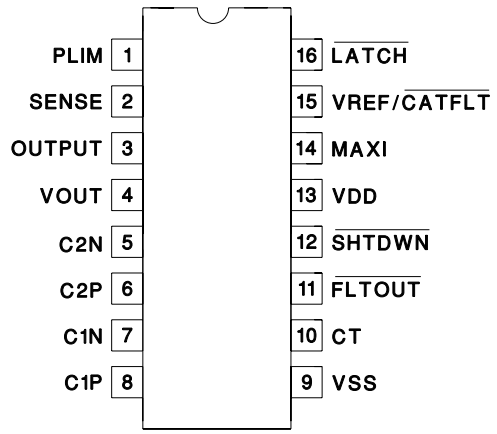
ABSOLUTE MAXIMUM RATINGS

IDD 5mA
SHTDWN Current 250µA
LATCH Current 250µA
VREF Current 250µA
PLIM Current 5mA
MAXI Input Voltage . . . . . VIN
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3917, –40°C to 85° for the UCC2917 and –55°C to 125°C for the UCC1917, C_T = 4.7nF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Section					
I_{CC}	From VOUT (Note 2)		5		mA
UVLO Turn On Threshold		8	9	10	V
UVLO Off Voltage		5.5	6.5	7.5	V
VSS Regulator Voltage		–6	–5	–4	V
Fault Timing Section					
Overcurrent Threshold	T_A = 25°C	47.5	50	53	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1V	–70	–50	–36	µA
CT Discharge Current	V_{CT} = 1V	0.9	1.5	2.1	µA
CT Fault Threshold		2.25	2.5	2.75	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition	1.7	2.7	3.7	%
Output Section					
Output High Voltage	I_{OUT} = θ	V_{IN}+6	V_{IN}+8	V_{IN}+10	V
	I_{OUT} = –500µA	V_{IN}+5	V_{IN}+7	V_{IN}+9	V
Output Low Voltage	I_{OUT} = θ		0	0.05	V
	I_{OUT} = 500µA		0.1	0.5	V
	I_{OUT} = 1mA		0.5	0.9	V
Linear Current Section					
Sense Control Votlage	MAXI = 100mV	85	100	115	mV
	MAXI = 400mV	370	400	430	mV
Input Bias	MAXI = 200mV		50	500	nA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SHUTDOWN Section					
Shutdown Threshold		2.0	2.4	2.8	V
Input Current	$\overline{SHTDWN}$ = 0V	24	40	56	µA
Shutdown Delay			100	500	ns
LATCH Section					
Latch Threshold		1.7	2	2.3	V
Input Current	LATCH = 0V	24	40	56	µA
Fault Out Section					
Fault Output High		4	5	6	V
Fault Output Low			0.01	0.05	V
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PLIMIT} = 64µA	4	5	6	V
Duty Cycle Control	I_{PLIMIT} = 64µA	0.6	1.2	1.7	%
	I_{PLIMIT} = 1mA	0.045	0.1	0.2	%
VREF/CATFLT Section					
V_{REF} Regulator Voltage		4	5	6	V
Fault Output Low			0.01	0.05	V
Output Sink Current	V_{CT} = 5V	2	5	8	mA
Overload Comporator Threshold	Relative to MAXI	140	200	260	mV

Note 1: All voltages are with respect to VOUT. Current is positive into and negative out of the specified terminal.
Note 2: Set by user with R3 and Rss

PIN DESCRIPTIONS

C1N: Negative side of the upper charge pump capacitor.

C1P: Positive side of the upper charge pump capacitor.

C2N: Negative side of the lower charge pump capacitor.

C2P: Positive side of lower charge pump capacitor.

CT: A capacitor is connected to this pin to set the maximum fault time. The maximum fault time must be more than the time to charge the external load capacitance (see Application Information). The maximum fault time is defined as

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}},$$

where I_{CH} = 36µA + I_{PLIM}, and I_{PLIM} is the current into the power limit pin. Once the fault time is reached, the output will shutdown for a time given by: $T_{SD} = 2 \bullet 10^6 \bullet CT$.

$\overline{\text{FLTOUT}}$: This pin provides fault output indication. Interface to this pin is usually performed through level shift transistors. Under a non-fault condition, $\overline{\text{FLTOUT}}$ will pull to a high state. When a fault is detected by the fault timer or the under voltage lockout, this pin will drive to a low state, indicating the output NMOS is in the off state.

$\overline{\text{LATCH}}$: Pulling this pin low causes a fault to latch until this pin is brought high or a power on reset is attempted. However, pulling this pin high before the reset time is reached will not clear the fault until the reset time is reached. Keeping $\overline{\text{LATCH}}$ high will result in normal operation of the fault timer. Users should note there will be an RC delay dependent upon the external capacitor at this pin.

MAXI: This pin programs the maximum allowable sourcing current. Since VREF/$\overline{\text{CATFLT}}$ is a regulated voltage, a voltage divider can be derived to generate the program level for MAXI. The current level at which the output appears as a current source is equal to the voltage on MAXI over the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on MAXI (to VOUT), and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUTPUT: Output device to the NMOS pass element.

PLIM: This feature ensures that the average NMOS power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element.

PIN DESCRIPTIONS (cont.)

When the voltage across the NMOS exceeds 5V, current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the 3% level.

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VOUT, a fault is sensed, and CT starts to charge.

$\overline{\text{SHTDWN}}$: This pin provides shutdown control. Interface to this pin is usually performed through level shift transistors. When shutdown is driven low, the output disables the NMOS pass device. When brought high, shutdown is disabled and the IC functions as intended. Users should note there will be an RC delay to the output dependent upon the external capacitor at this pin.

VDD: Power to the chip. On startup, power is current fed from a resistor (and a series diode) to V_{IN}. In normal operation, power will be supplied by the charge pump.

VOUT: Ground reference for the IC.

VREF/$\overline{\text{CATFLT}}$: This pin primarily provides an output reference for the programming of MAXI. Secondarily, it provides catastrophic fault output indication. Under a catastrophic fault, when the IC is unsuccessfully attempting to shutdown the NMOS pass device, this pin will pull to a low state. In an application, this pin could be connected to a second NMOS transistor in series with the main NMOS for redundancy. Due to the primary function of this pin, full gate drive would not be available to the second NMOS.

VSS: Negative reference out of the chip. Normally current fed via a resistor to ground.

APPLICATION INORMATION

Fault Timing

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3917. For simplicity, we first consider a typical fault mode where the overload comparator and the current source I3 do not come into play. A typical fault occurs once the voltage across the current sense resistor, R_S, exceeds 50mV. This causes the over current comparator to trip and the timing capacitor to charge with current source I1 plus the current from the power limiting amplifier, or PLIM amplifier. The PLIM amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{(V_{IN} - VOUT) - 5V}{R_{PL}}$$

Later, it will be shown how this feature will limit average power dissipation in the pass device. Note that under normal fault conditions where the output current is just above the fault level, VOUT ≅ V_{IN}, I_{PL} = 0, and the C_T charging current is just I1 or 50µA.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capaci-

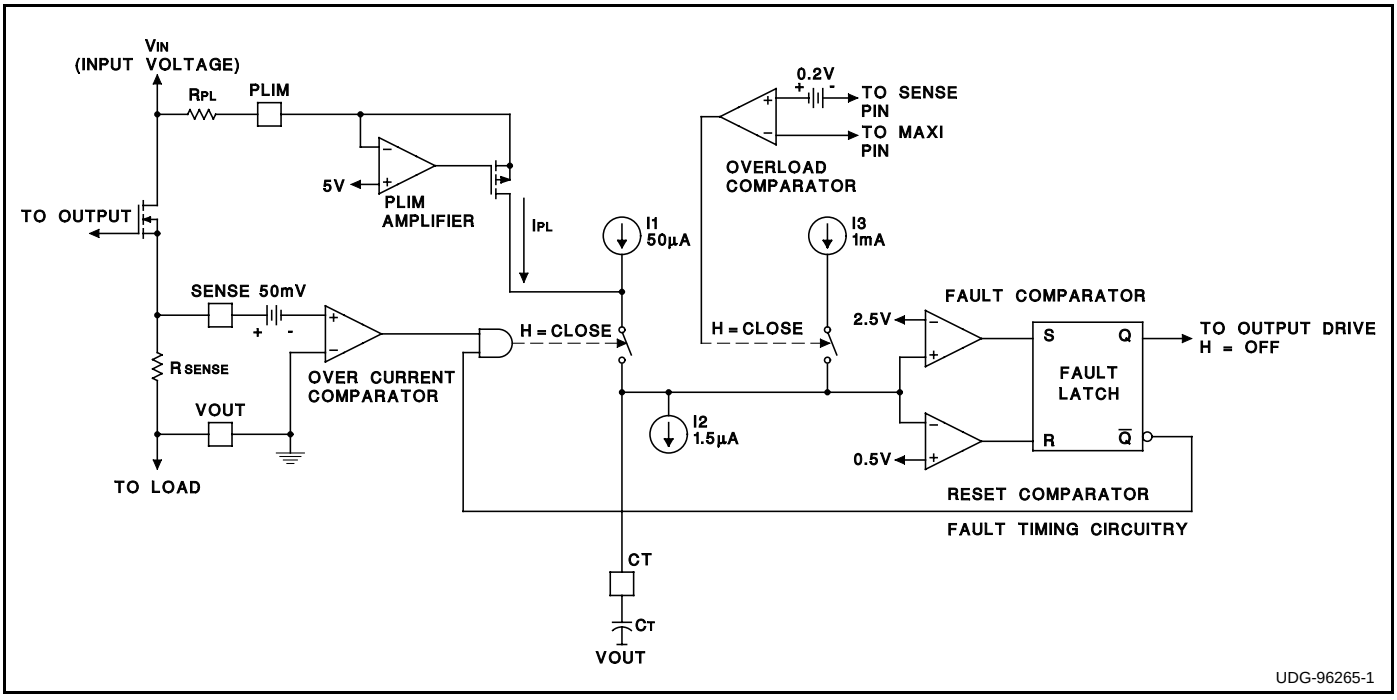


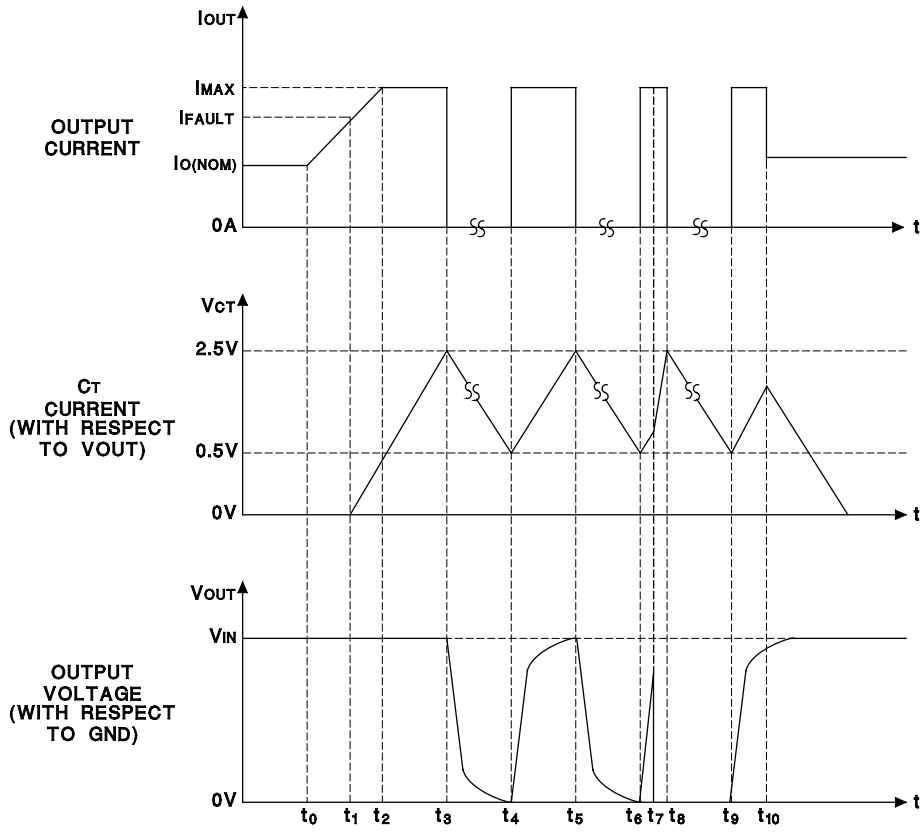
Figure 1. Fault Timing Circuitry for the UCC3917, Including Power Limit and Overload.

APPLICATION INFORMATION (cont.)

tor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with current source I2 until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets (assuming LATCH is high, otherwise the fault latch will not reset until the LATCH pin is brought high or a power-on reset occurs) which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{1.5\mu A}{I_{PL} + 50\mu A}$$

where I_{PL} is 0µA under normal operations (see Figure 2).



t0: Safe condition - output current is nominal, output voltage is at the positive rail, V_{IN}.

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 36µA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs - CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, VOUT discharges to ground.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT rises to V_{IN}.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4:

t7: Output short circuit - if VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for V_{IN} and R_{PL}.

t8: Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition - return to normal operation of the circuit breaker.

Note that t6 – t5 ≅ 36 • (t5 – t4).

Figure 2. Nominal Timing Diagram

APPLICATION INFORMATION (cont.)

However, under large transients, average power dissipation can be limiting using the PLIM pin. A proof follows, average dissipation in the pass element is given by:

$$P_{FET\ AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \text{Duty Cycle}$$

$$= (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1.5\mu A}{I_{PL} + 50\mu A}$$

Where (V_{IN} - VOUT) >> 5V,

$$I_{PL} \cong \frac{V_{IN} - VOUT}{R_{PL}}$$

and where I_{PL} >> 50µA, the duty cycle can be approximated as:

$$\frac{1.5\mu A \bullet R_{PL}}{V_{IN} - VOUT}.$$

Therefore the average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1.5\mu A \bullet R_{PL}}{V_{IN} - VOUT}$$

$$= I_{MAX} \bullet 1.5\mu A \bullet R_{PL}$$

Notice that since (V_{IN} - VOUT) cancels, average power dissipation is limited in the NMOS pass element (see Figure 3). Also, a value for R_{PL} can be roughly determined from this approximation.

$$R_{PL} = \frac{P_{FET\ AVG}}{I_{MAX} \bullet I.5\mu A} \quad \text{with}$$

$$R_{PL}(min) = \frac{V_{IN} - 5V}{5\mu A}$$

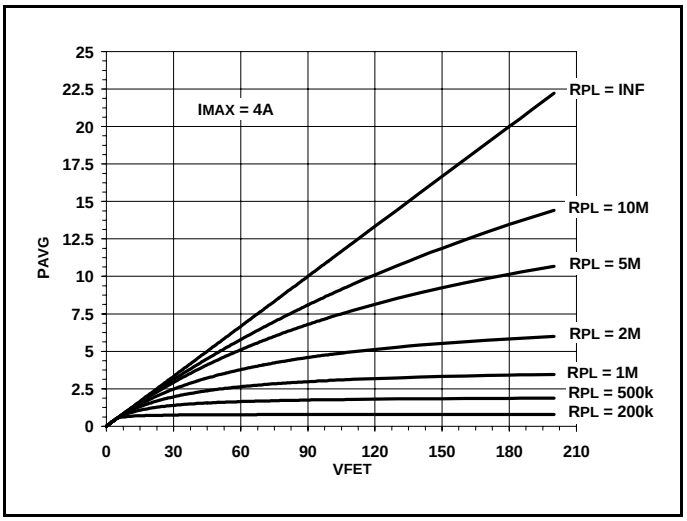


Figure 3. Plot of Average Power vs. FET Voltage for Increasing Values of R_{PL}

Overload Comparator

The linear amplifier in the UCC3917 ensures that the output NMOS does not pass more than I_{MAX} (which is V_{MAXI}/RS). In the event the output current exceeds the programmed I_{MAX} by 0.2V/RS, which can only occur if the output FET is not responding to a command from the IC, CT will begin charging with I3, 1mA, and continue to charge eventually tripping a catastrophic fault comparator not shown. This comparator will then drive VREF/CATFLT low, which can be used to build redundancy into the system if desirable (as outlined in the pin description for VREF/CATFLT).

Selecting Minimum Timing Capacitance

The startup time of the IC may not exceed the fault time for the application. Since the timing capacitor, C_T, determines the fault time, it's minimum value can be determined by first finding out the startup time. The startup time is dependent on several external components. For example, a capacitive load is required for the IC to startup, and will be referred to as C_{LOAD}. C_{IN}, also required and equal to 0.1µF, represents the capacitor between the VDD and VOUT pins.

Let IMAX be the maximum current allowable through the external NMOS device (programmed via MAXI, of course). Then, we can define the startup time of the IC as such:

Current Source Load:

$$T_{START} = \frac{1.2 \bullet C_{LOAD} \bullet V_{IN}}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = 2 \bullet R_{LOAD} \bullet C_{LOAD} \bullet \ln\left(\frac{I_{MAX} \bullet R_{LOAD}}{I_{MAX} \bullet R_{LOAD} - V_{IN}}\right)$$

The only remaining external component which may affect the minimum timing capacitor value is the optional power limiting resistor, R_{PL}. If R_{PL} is desired, it's value can be determined form the "Fault Timing" section above. Finally, the minimum timing capacitor can now be calculated.

Current Source Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (62\mu A \bullet R_{PL} + V_{IN} - 10V)}{10V \bullet R_{PL}}$$

Resistive Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (31\mu A \bullet R_{PL} + V_{IN} - 5V - I_{MAX} \bullet R_{LOAD})}{5V \bullet R_{PL}}$$

APPLICATION INFORMATION (cont.)

$$+\frac{3 \bullet R_{LOAD} V_{IN} \bullet C_{LOAD}}{5V \bullet R_{PL}}$$

If R_{PL} is not used and PLIM is left unconnected, the equations simplify to:

$$C_{Tmin} = 18.6 \times 10^{-6} \bullet T_{START}$$

for either load condition.

Selecting Other External Components

Other external components are necessary for correct operation of the IC. Referring to the application diagram at the back of the data sheet, resistors R_{SENSE}, R_{SS}, R1, R2 and R3 are required and follow certain equations with a brief description following where applicable:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$ (Sense Resistor)

$$R_{SS} = \frac{V_{IN} - 5V}{5mA}$$ (Connected between VSS and GND)

$$R3 = \frac{V_{IN} - 10}{5mA}$$ (Used in series with a diode to connect VIN to VDD)

(R1 + R2) > 20kΩ (Current limit out of VREF)

Lastly, the external capacitors used for the charge pump are required and need to equal 0.1µF, i.e. C_{IN} = CH = C1 = C2 = 0.1µF.

Level Shift Circuitry (Optional)

The level shift circuitry shown in Figure 4 and Figure 5 represents one way of performing interface to LATCH, SHTDWN, and FLTOUT. These pins provide functionality that is not necessary for normal operation of the IC but may prove useful to the application. The resistor, R, shown in both figures is used for current limiting and follows R_{MIN} = VIN/250µA. The capacitor, C, shown in both figures is optional to the level shift circuitry and keeps spurious signals from occurring during transients. It's minimum value is C_{MIN} = 0.1nF. It should be noted that the use of the capacitor, C, will cause delays into and out of these pins.

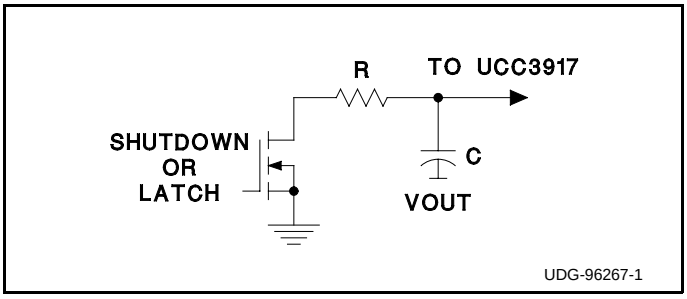


Figure 4. Potential Level Shift Circuitry to Interface to LATCH AND SHTDWN on the UCC3917

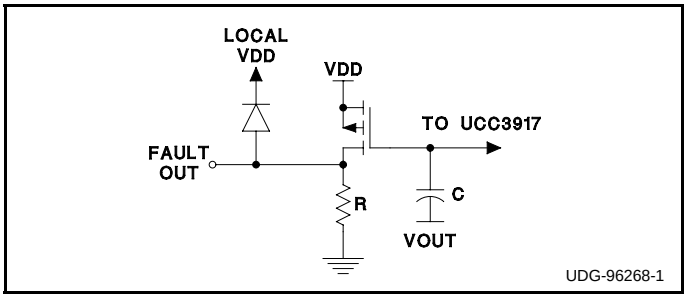


Figure 5. Potential Level Shift Circuitry to Interface to FLTOUT on the UCC3917

SAFETY RECOMMENDATIONS

Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3917 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

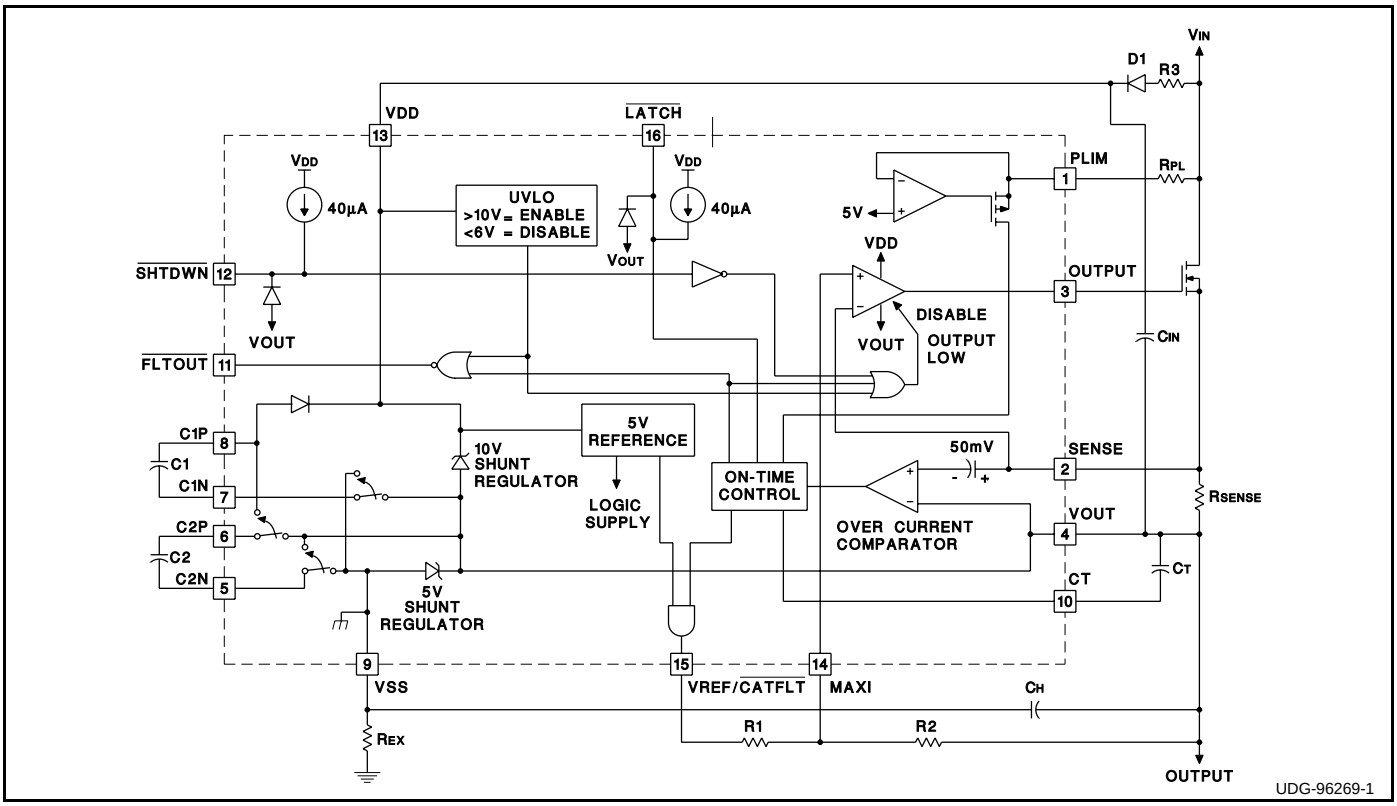


Figure 5. Positive Floating Hot Swap Power Manager

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