Full Bridge Power Amplifier

FEATURES

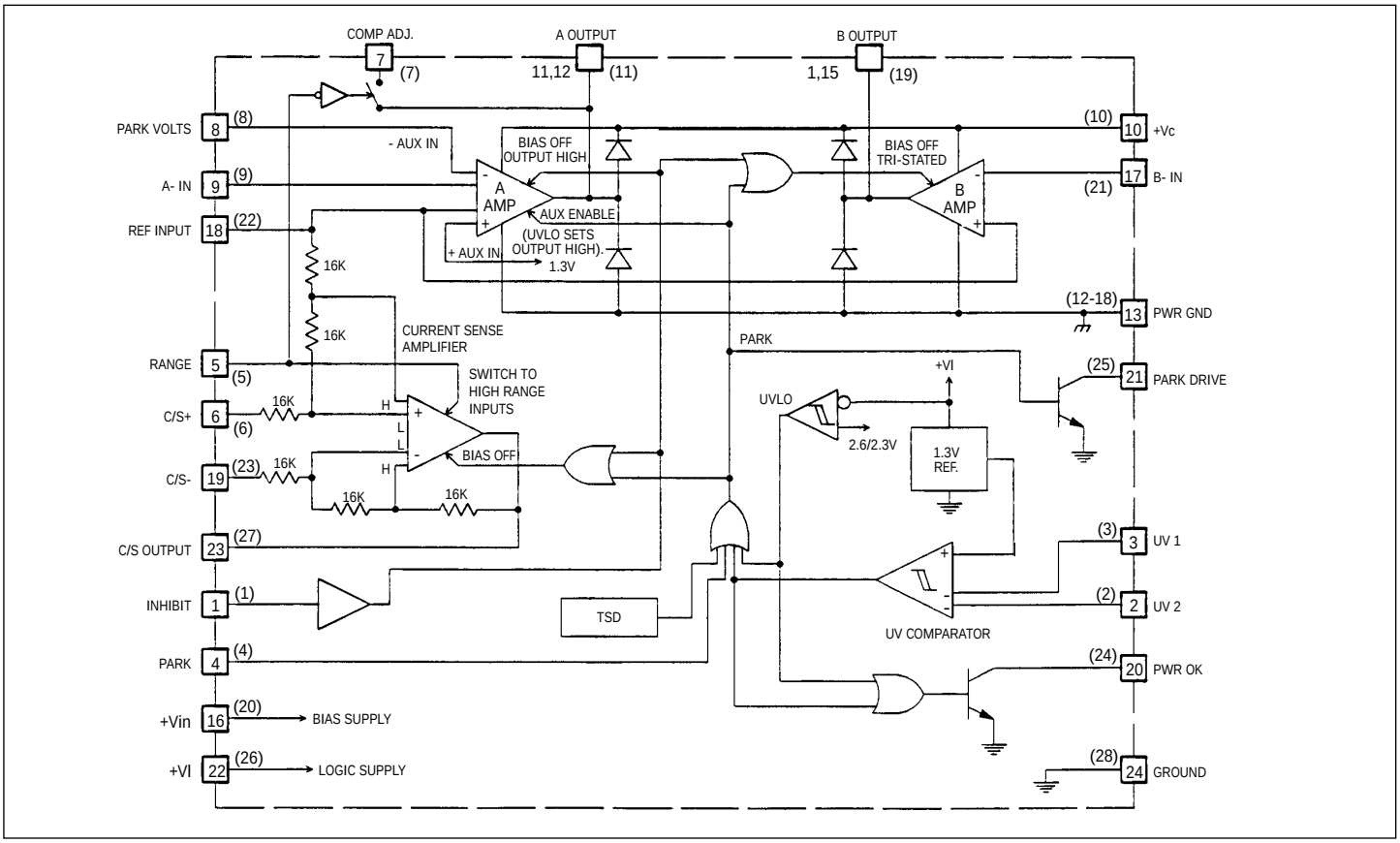
- Precision Current Control
- +/- 550mA Load Current
- 1.3V Typical Total Vsat at 550mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- 5V or 12V Operation
- 12mA Quiescent Supply Current
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

DESCRIPTION

This full-bridge power amplifier, rated for continuous output current of 0.55 Amperes, is intended for use in demanding servo applications such as head positioning for high-density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3173A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and activate the built-in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low-side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.



Pin numbers shown are for “DW” PKG., ( ) numbers are for “QP” PKG.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+Vin, +Vc, +Vl).....20V
UV Comparator, Logic Inputs, and Ref Input
maximum forced voltage.....-0.3V to 10V
maximum forced current.....+/- 10mA
B Amplifier Inverting Input.....-0.3V to +Vin + 1.0V
A Amplifier Inverting Inputs,(Aux. and normal).-0.3Vto +Vc + 1.0V
Open Collector Output Voltages 20V
A and B Output Currents (continuous)
source.....Internally Limited
sink 0.6A
Parking Drive Output Current
continuous 150mA
pulsed.....1A
Output Diode Current (pulsed).....0.6A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature .....- 55°C to +150°C
Storage Temperature.....- 65°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500uS.

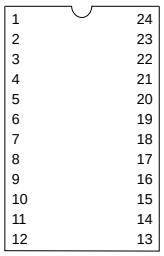
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
Thermal Resistance Junction to Leads, θjl .....15°C/W
Thermal Resistance Junction to Ambient, θja ....30°-40°C/W
DW package:
Thermal Resistance Junction to Leads, θjl ..... 35°C/W
Thermal Resistance Junction to Ambient, θja ....60°-70°C/W
FQ package:
Thermal Resistance Junction to Leads, θjl .....60°C/W
Thermal Resistance Junction to Ambient, θja .110-120°C/W

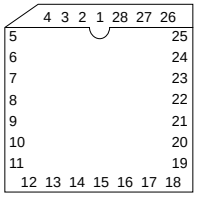
Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guide lines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAMS

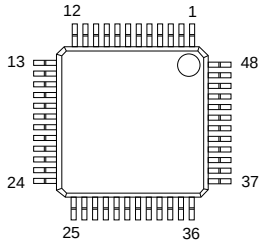
SOIC - 24 (TOP VIEW)
DW PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



TQFP-48 (TOP VIEW)
FQ PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DW	QP	FQ
INHIBIT	1	1	9
UV 2	2	2	10
UV 1	3	3	11
PARK	4	4	12
RANGE	5	5	13
C/S+	6	6	14
COMP ADJ	7	7	15
PARK VOLTS	8	8	16
A- IN	9	9	21
+Vc	10	10	22
A OUTPUT	11,12	11	26, 27
POWER GND	13	12-18	30, 31
B OUTPUT	14,15	19	34, 35
+Vin	16	20	39
B- IN	17	21	40
REF INPUT	18	22	45
C/S-	19	23	46
PWR OK	20	24	47
PARK DRIVE	21	25	48
+Vl	22	26	2
C/S OUTPUT	23	27	3
GROUND	24	28	4

Electrical Characteristics:
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+Vin Supply Current			10	13	mA
+Vc Supply Current	Iout = 0A		1.2	2.0	mA
+Vl Supply Current			0.65	1.0	mA
Total Supply Current	Supplies = 5V, Iout = 0A		12	16	mA
	Supplies = 12V, Iout = 0A		13	18	mA
+Vl UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysteresis			300		mV
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current	Max at either UV input	-1.0	-0.25		uA
UV Thresholds	low to high, other input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWR OK Vsat	Iout = 5mA, UV input low		0.15	0.45	V
PWR OK Leakage	Vout = 20V			5	uA

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER AMPLIFIERS A AND B					
Input Offset Voltage	A Amplifier, Vcm = 2.5V			4	mV
	B Amplifier, Vcm = 2.5V			12	mV
Input Bias Current	Vcm = 2.5V, Inverting inputs only	-500	-150		nA
Input Bias Current at Ref. Input	(Ref. Input - C/S+)/48Kohms, Tj = 25°C	15	21	27	uA/V
CMRR	Vcm = 1 to 10V, Supplies = 12V	70	90		dB
PSRR	+Vin = 4 to 15V, Vcm = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, Vout = 1V, Iout = 300mA to Vout = 11V, Iout = -300mA	3.0	15.0		V/mV
Gain Bandwidth Product	Note 1, A Amplifier		2.0		MHz
	Note 1, B Amplifier		1.0		MHz
Slew Rate	Note 1		1.0		V/uS
High-Side Current Limit		0.55	0.6		A
Output Saturation Voltage	High-Side, Iout = -100mA, Note 2		0.7		V
	High-Side, Iout = -300mA, Note 2		0.8		V
	High-Side, Iout = -550mA, Note 2		0.95		V
	Low-Side, Iout = 100mA		0.2		V
	Low-Side, Iout = 300mA		0.25		V
	Low-Side, Iout = 550mA		0.35		V
	Total Vsat, Iout = 100mA		0.9	1.2	V
	Total Vsat, Iout = 300mA		1.05	1.4	V
	Total Vsat, Iout = 550mA		1.3	1.7	V
+Vc to +Vin Headroom	Volts below +Vin, delta High-Side Vsat = 100mV, Iout = -550mA, Note 2	0.23	0.4		V
High-Side Diode, Vf	Id = 550mA		1.0		V
Low-Side Diode, Vf	Id = 550mA, Inhibit activated, B amplifer only		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	Vcm = 2.5V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change with Common Mode Input	Vcm = -1V to 13V, Supplies = 12V Low Range Mode			2000	uV/V
	High Range Mode			4000	uV/V
Voltage Gain	Vdiff = +1.0 to -1.0V, Vcm = 2.5V High range mode	0.485	0.50	0.515	V/V
	Low range mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, Iout = 1mA,		0.1	0.3	V
	High-Side, Iout = -1mA, Referenced to +Vin		0.1	0.3	V
PARKING FUNCTION					
Park Input Threshold Voltage		0.6	1.1	1.7	V
Park Input Threshold Current	Internal pull-up, Vin = 0.6V		50	75	uA
Park Drive Saturation Voltage	Iout = 50mA		0.15	0.35	V
Park Drive Leakage	Vout = 20V			50	uA
Regulating Voltage at Park Volts Input		1.275	1.30	1.325	V

Note 1: This specification not tested in production

Note 2: The high-side saturation performance of the UC3173A is referenced to the +Vin supply pin. The +Vc suppy pin can operate slightly below the +Vin supply input, about 400 mV, without affecting this performance.

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTION (CONTINUED)					
Amplifier A Auxiliary Input Bias Current		-750	-300		nA
Amplifier A Parking High-Side Saturation Voltage	Iout = -50mA, +Vin = 0V, +Vc = +Vl = 5V, Park Input Open, +Vc to Vout		0.8	0.95	V
Minimum Parking Supply	At +Vc and +Vl, +Vin = 0V, A Amplifier out - Vsat Parking Drive>0.5V Ipark = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At +Vl, +Vc = +Vin = 0V, Vsats < 0.5V, Iout Parking Drive = 50mA, Rl = 30ohms to 2V		1.1	1.4	V
	Iout Power OK = 5mA, Rl = 300ohms to 2V		1.2	1.6	V
+Vl Parking Supply Current	Park Input Open, +Vl = 5V, +Vc = 1.6V, +Vin = 0V Power OK Iout = 5mA, Parking Drive Iout = 50mA		1.6	3.0	mA
AUXILIARY FUNCTIONS					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		uA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	uA
Comp Adjust Pin Saturation Voltage	Range Input = 0V, Pin Current = +/-500uA Referenced to Aout		0.02	0.1	V
Comp Adjust Leakage Current	Range Input = 1.7V, Supplies = 12V Aout-V Comp Adj = +/-6V			5	uA
Total Supply Current when Inhibited	+Vin, +Vc, and +Vl currents		1.0	1.5	mA
Thermal Shutdown Temperature	Note 1		165		°C

Note 1: This specification not tested in production

PIN FUNCTIONAL DESCRIPTION

+Vin Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high-side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

+Vc +Vc supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A, or B amplifiers are to be activated. This pin can operate approximately 400mV below the +Vin supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

+Vl Logic portions of the UC3173A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PARKING DRIVE and POWER OK outputs. This pin is a low current supply that would normally be tied to the +Vc pin, or to a parking hold-up capacitor for extended parking operation with very low recovered back-emf.

GND Reference point for the internal reference, UV comparator, and other low-level circuitry.

PWR GND Current return for all high level circuitry, this pin should be connected to the same potential as **GND**.

A Out Output for the A power amplifier, providing one end of the differential drive to the load during normal operation, and during park. During a UVLO condition at the +Vin supply pin, this output is forced to a high, source only state.

B Out Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tri-stated.

A- In Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

B- In Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

Ref Input Reference for input control signals to the power amplifier, as well as, the non-inverting inputs to the A and B amplifiers, and the output level shift for the C/S amplifier.

C/S+ The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

Ref Input / 2 - 0.3V, in low range mode, and
2 • **Ref Input** - 0.9V, in high range mode.

C/S- The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

Range When this pin is open or at a logic **low** potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic **high**, the gain of the current sense amplifier will change into its **high** range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

Comp Adj The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

UV 1 & 2 Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the **Power OK** output to an active low state. If either of these inputs is not used it should be connected to a voltage greater than 1.3V.

Power OK Indicates with an active low condition that either of the **UV** inputs are low, or that the supply voltage at the **+VI** input to the UC3173A has dropped below the UVLO threshold. This output will remain active low until the **+VI** supply has dropped to below approximately 1.2V.

Park Volts The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3173A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-emf/velocity retract of the head. The park condition on the UC3173A is **always** activated by any one of the following four conditions, 1: a low condition on either of the **UV** inputs, 2: a high input level at the **Park** input, 3: a UVLO condition at the **+VI** supply pin, and 4: activation of the **TSD**, (thermal shutdown) protection circuit. During a UVLO condition at the **+VI** pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

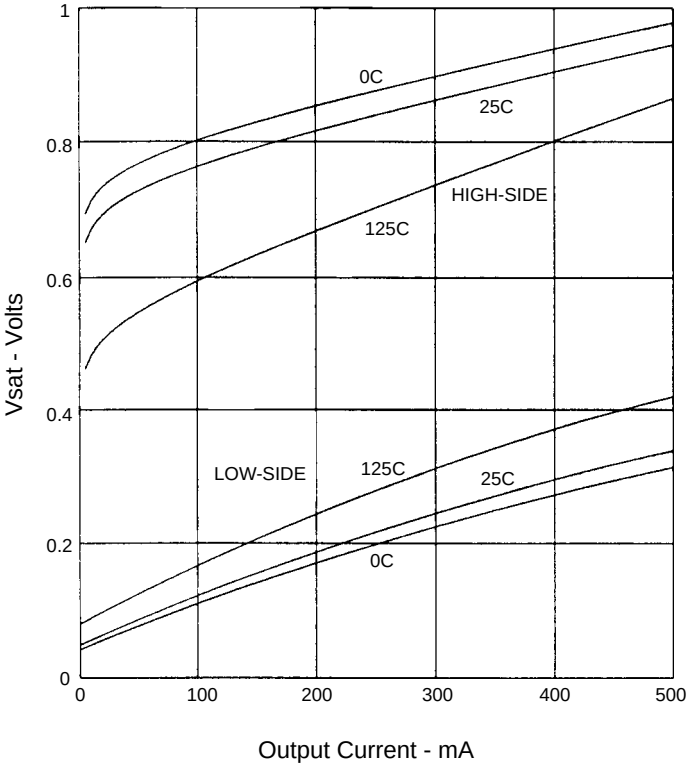
Park Logic input that forces the park condition on the UC3173A. This input has an internal pull-up that will force the park condition if the pin is left open.

Park Drive A 100mA drive output that is active low during a park operation. This pin is normally used to supply the low-side drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

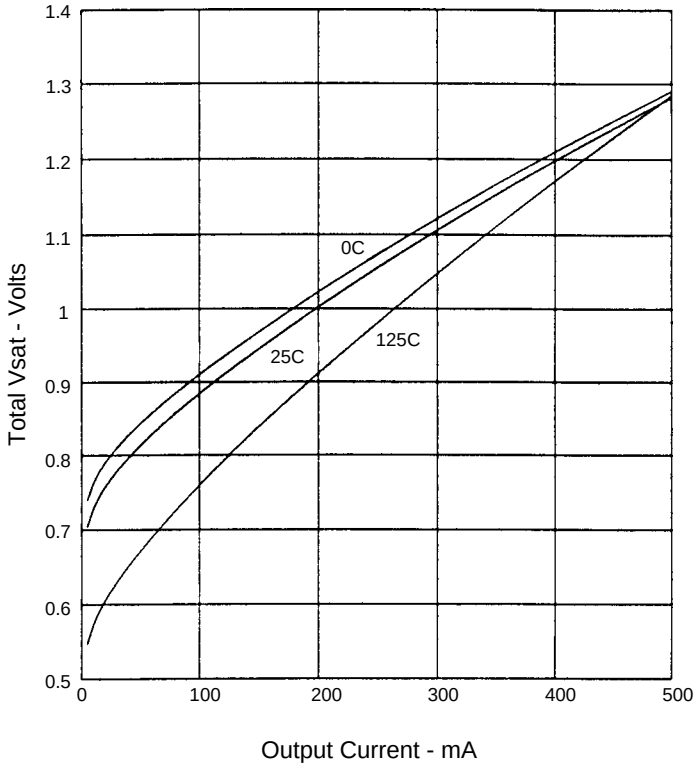
Inhibit A high impedence logic input that disables the A and B power amplifiers, as well as the Current Sense amplifier. The UV comparators and logic functions of the UC3173A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The **Inhibit** function is over-ridden by any condition that forces the park function to be activated.

CHARACTERISTIC CURVES

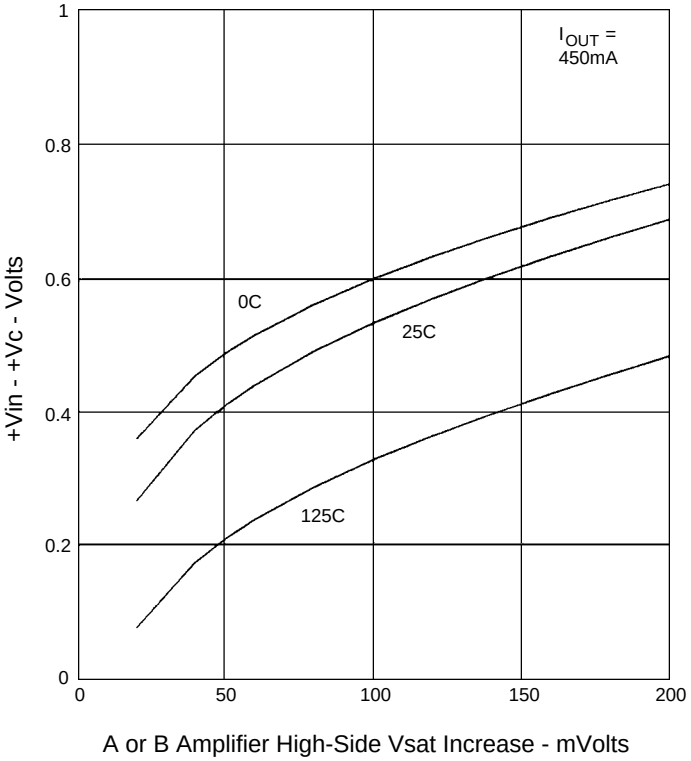
A AND B AMPLIFIER HIGH AND LOW VSATS



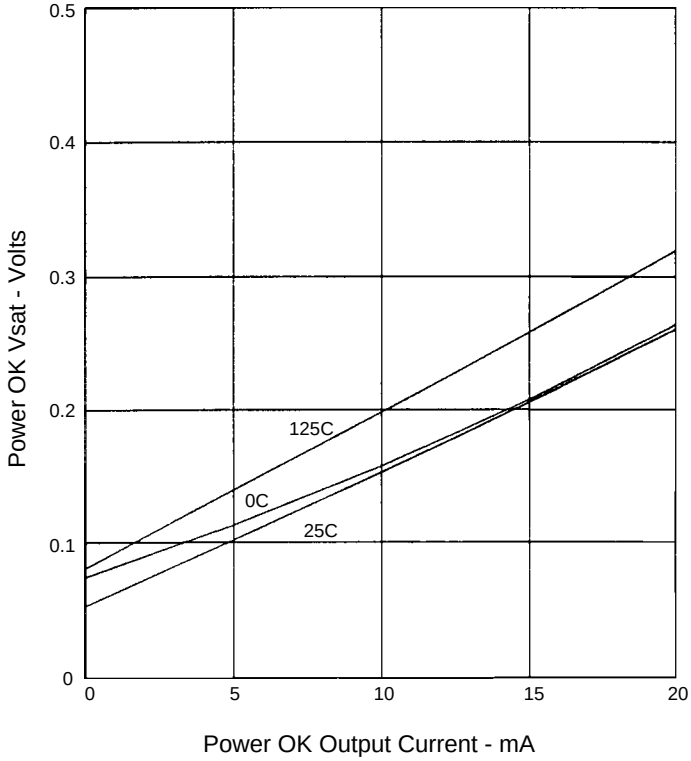
A AND B AMPLIFIER TOTAL VSAT



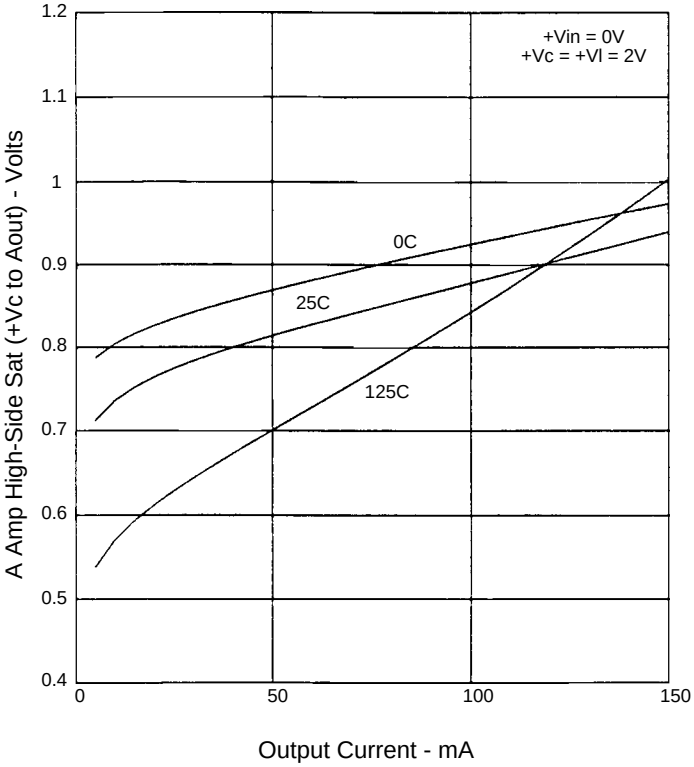
+Vin TO +Vc HEADROOM



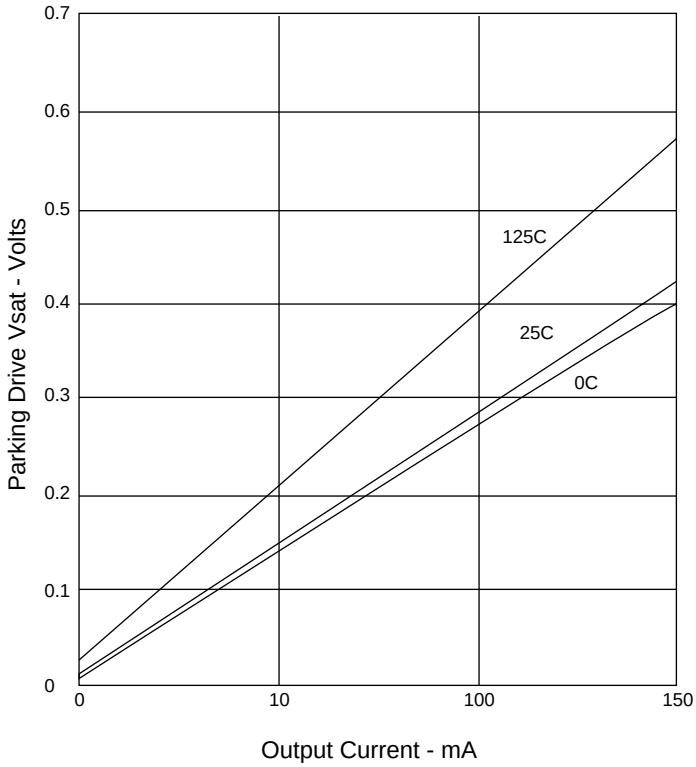
POWER OK SATURATION VOLTAGE



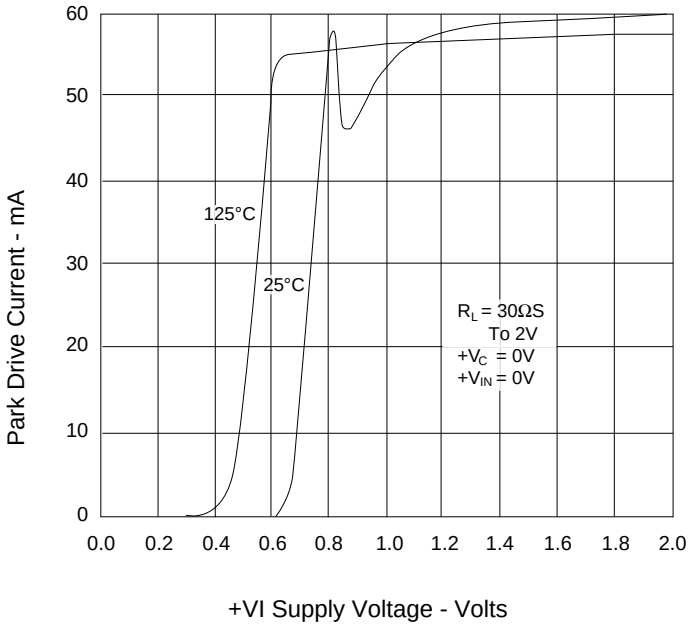
A AMPLIFIER HIGH-SIDE Vsat IN PARK MODE



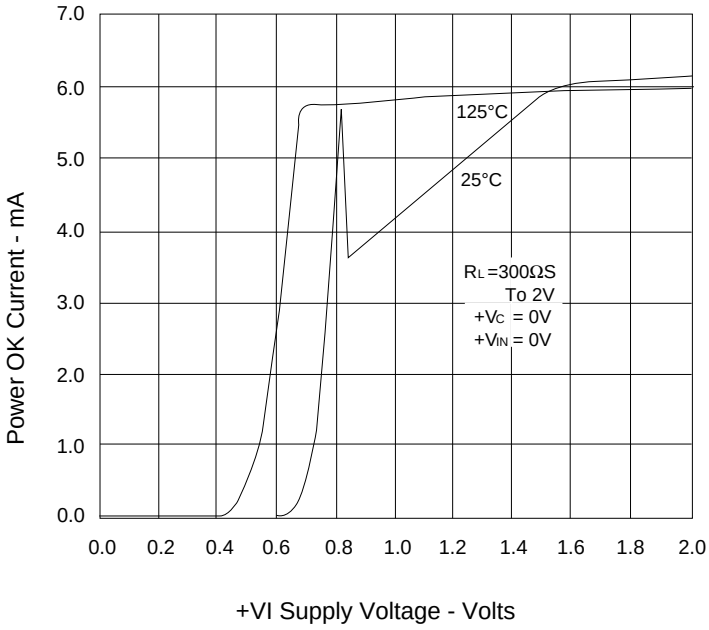
PARKING DRIVE SATURATION VOLTAGE



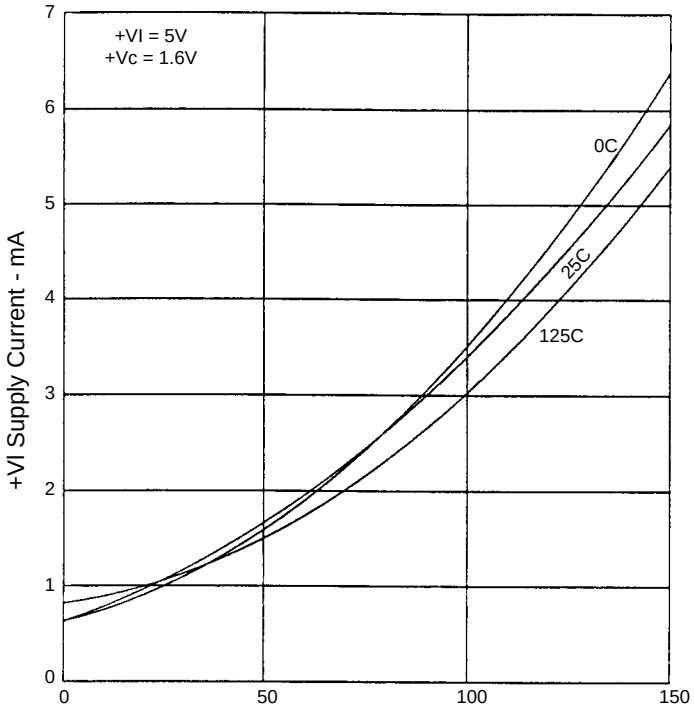
PARK DRIVE CURRENT vs. +VI SUPPLY



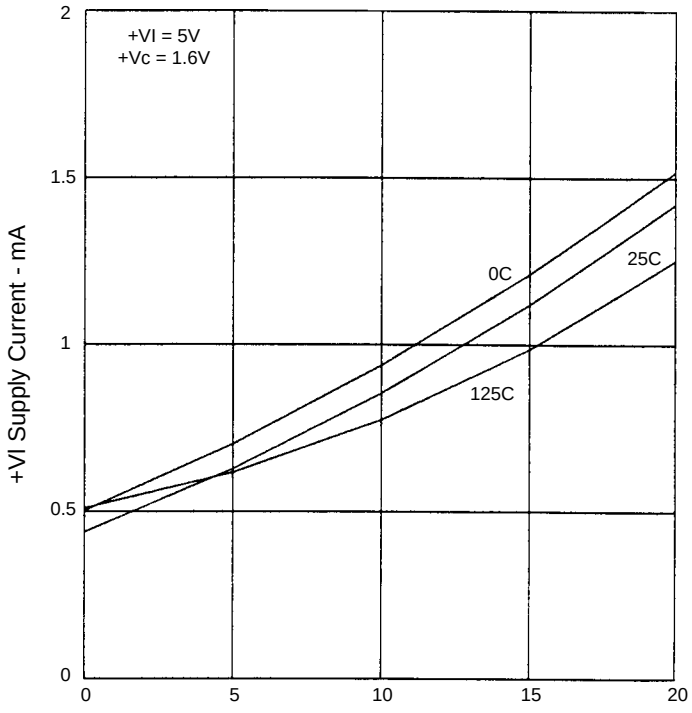
POWER OK CURRENT vs. +VI SUPPLY



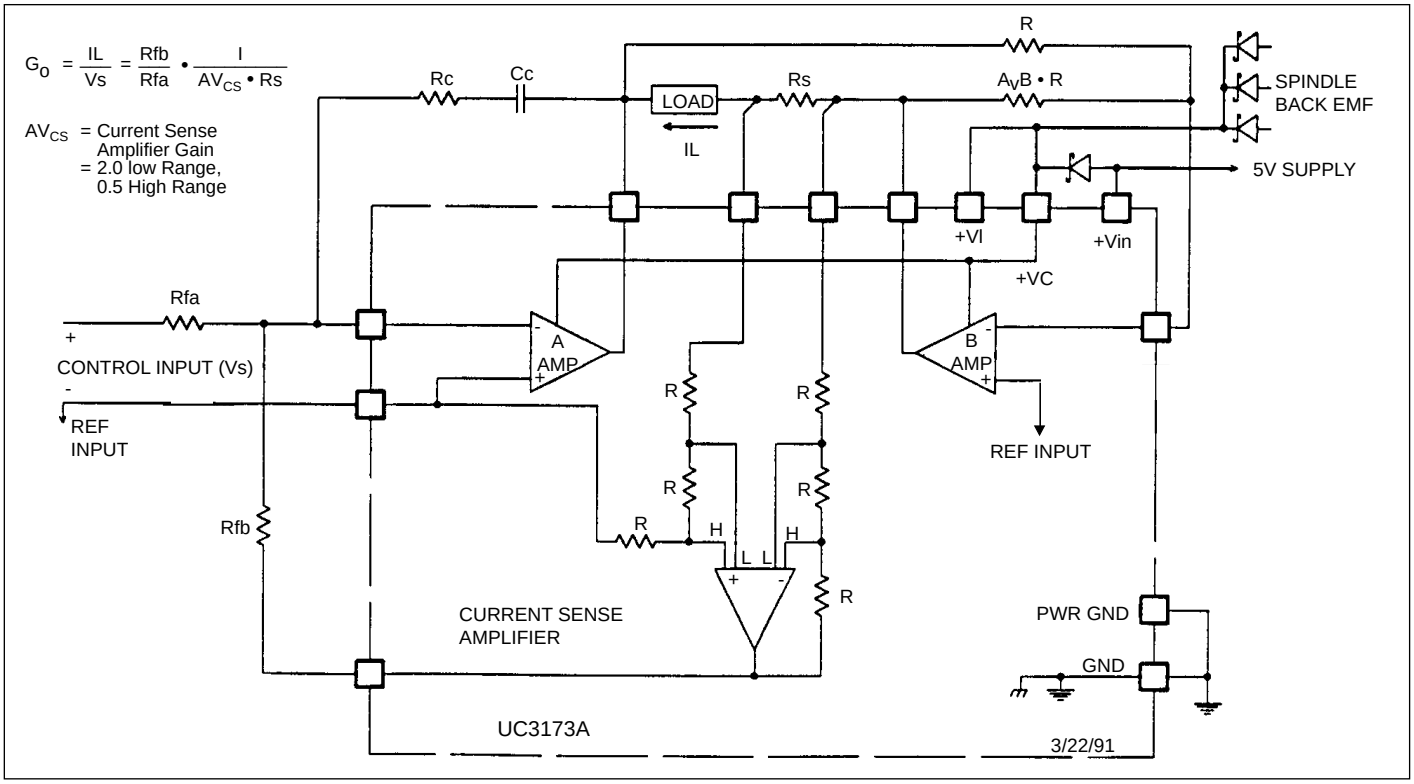
+VI CURRENT VERSUS PARK DR CURRENT



+VI CURRENT VERSUS PWR OK CURRENT



TYPICAL APPLICATION



Maximizing the Voltage to the Load

In order to assure that maximum voltage drive to the load is achievable there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the **Ref Input** and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the **Ref Input** voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (1).

$$(1)\ V_{ref}(\text{optimum}) = \frac{+Vin - Vhs_{sat} + Vls_{sat}}{2}$$

where: Vhs_{sat} = high-side V_{sat} at maximum load.
Vls_{sat} = low-side V_{sat} at maximum load.

Data for (1) can be taken off the characteristic curves showing Vsat performance versus output current. There will be a degree of temperature dependence to this solution since the low side Vsat of the power stages has a positive temperature dependence, and the high-side a negative. In some cases it might be worth interpolating between the 25°C and the 125°C curves to hit a typical junction temperature.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given **Ref Input** voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by,

$$(2)\ A_{VB} = \frac{+Vin - Vhs_{sat} - V_{ref}}{V_{ref} - Vls_{sat}}$$

or,

$$\frac{Vref - Vls_{sat}}{+Vin - Vhs_{sat} - V_{ref}}$$

whichever is greater than unity.

For a typical case, where Vref has been set at +Vin/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of (A_{VB}+1).

Setting and Maximizing the Loop Bandwidth
The normal configuration for compensation of the power amplifier is shown in the ***Typical Application*** drawing. A simple RC network. RcCc time constant is typically chosen to correspond to the electrical time constant of the load, given by RI/L. Where RI is the total load and sense resistanace between the bridge outputs, and L is the load inductance.

The 3dB frequency(f_{3dB}) of the closed loop amplifier is given by the following expression:

$$(3)\ f_{3dB} = \frac{(1 + A_VB) \bullet A_VCS \bullet Rs \bullet Rc}{2\pi L \bullet Rfb}$$

assuming $f_{3dB} >> (2\pi Rc \bullet Cc)^{-1}$

where: A_VB is the voltage gain of the B amplifier.
A_VCS is the CS amplifier voltage gain.

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in the typical application drawing, the noise gain is given by the impedance ratio of the Rc-Cc series network, to the parallel combination of Rfa and Rfb. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product(GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

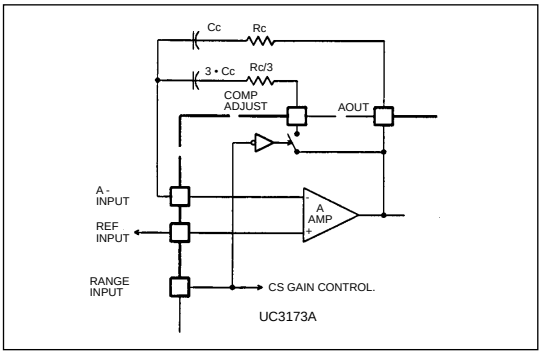
$$(4)\ f_{3dBmax} = \left(\frac{f_{gbw}A \bullet (1+A_VB) \bullet A_VCS \bullet Rs \bullet Rfa}{2\pi L \bullet (Rfa + Rfb)}\right)^{1/2}$$

where: $f_{gbw}A$ is the GBW of the A amplifier.

In the UC3173A, to accommodate wider power amplifier bandwidths, the GBW Product of the A amplifier has been extended to 2MHz. A loop compensated in this manner will have a second order closed response with the poles split around the 3dB frequency given in (3). The loop phase margin will be approximately 45°. The value of Rc required to set the above conditions is given by

$$(5)\ Rc_{max} = Rfb \bullet \left(\frac{f_{gbw}A \bullet 2\pi L \bullet Rfa}{(A_VB + 1) \bullet A_VCS \bullet Rs \bullet (Rfa + Rfb)}\right)^{1/2}$$

Range Change Bandwidth Control
When the range change feature of the UC3173A is used the closed loop bandwidth of the power amplifier will change according to (3). In other words, the bandwidth would be four times larger during the low range mode when AVCS is equal to 2, than during the high range mode when AVCS is equal to 0.5, unless the value of Rc is adjusted to compensate. The **Comp Adjust** pin on the UC3173A can be used to do this. The **Comp Adjust** pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.



The Comp Adjust pin switches in a parallel compensation network tostabilize the small signal bandwidth with range changes.

Head Parking
In the application figure, ***Controlled Velocity Head Parking,*** the UC3173A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by

$$(6)\ V_{park} = 1.3 \bullet \left(1 + \frac{R1}{R2}\right)$$

The B amplifier output is tri-stated during park, this side of the load is driven low by the **Park Drive** pin. A series resistor, Rp in the figure, can be inserted in series with the load to limit the peak current if required.

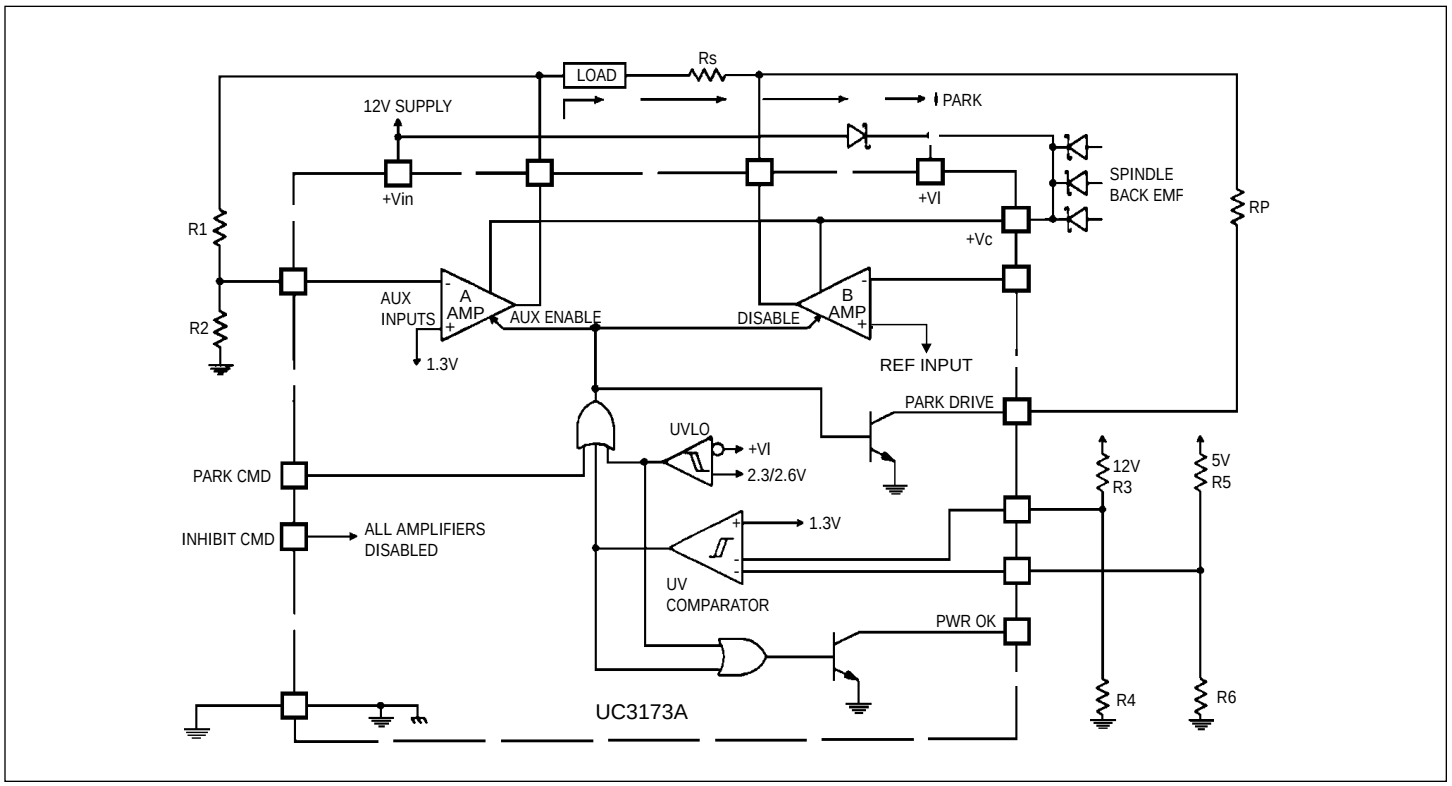
During park, supply to the load, and the UC3173A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the **+Vl** supply pin drops below the UVLO voltage,(2.3V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3173A will maintain drive to the load down to low supply levels. For example, with 1.5 Volts of recovered back EMF, the UC3173A can still deliver 50mA of drive to a 10 ohm load.

Parking With Very Low Back EMF
The UC3173 can also be configured to get parking drive to the load with very low recovered back EMF. The figure titled ***Head Parking with Low Back EMF*** illustrates how the **Power OK** pin can be used to drive an external PNP device to achieve very low parking drive Vsat losses. With this configuration, the UC3173A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

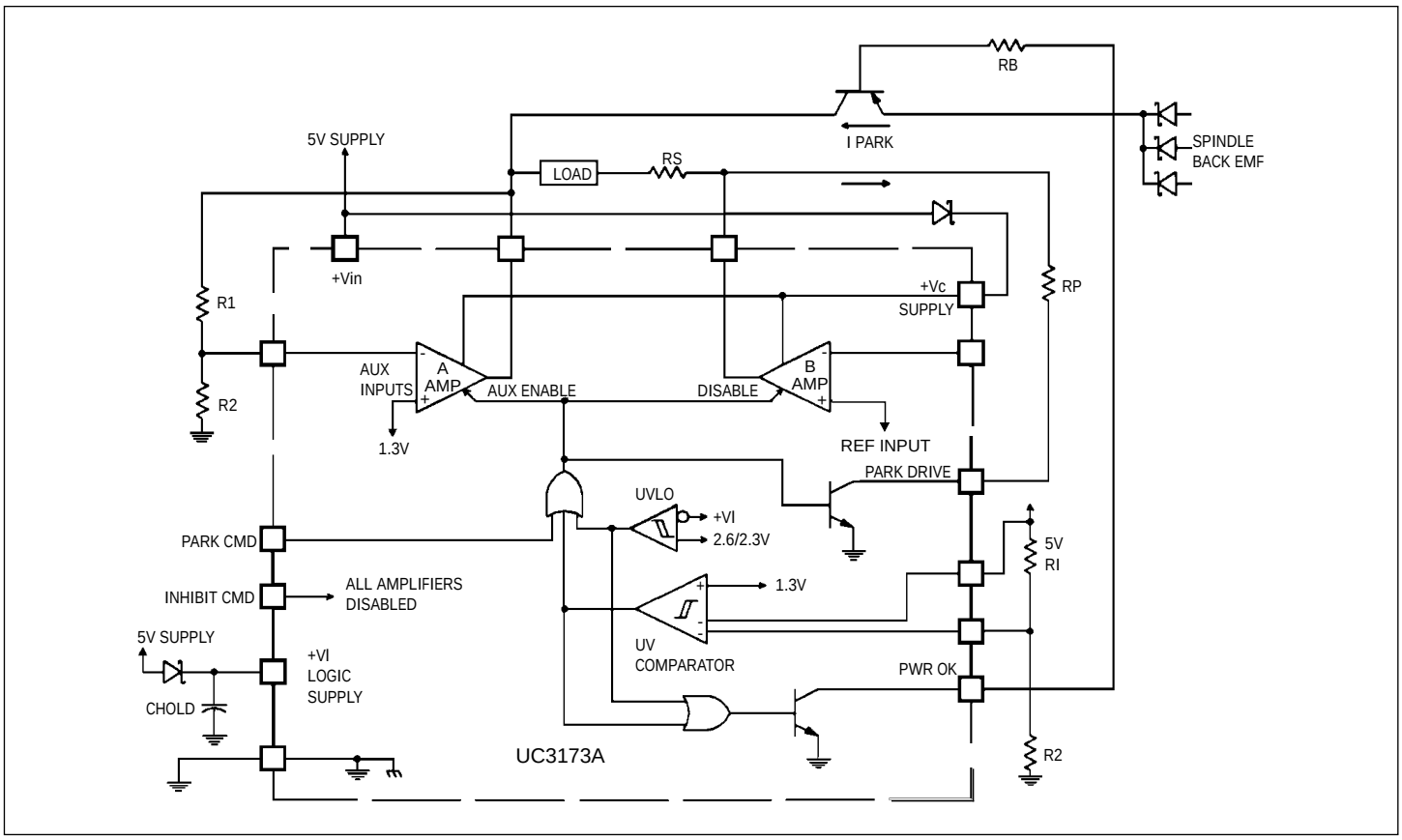
During system commanded parking with the supplies present, the **Park Volts** pin is still used to set the maximum voltage to the load. The logic function of the Power OK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the **Park Drive** and **Power OK** pins are provided by the **+Vl** supply pin. By using a hold up capacitor, CHOLD, the drive can be maintained to the load as the back EMF drops to below 1 volt. A variation on this approach is to add a connection between the +Vl pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V volt supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply drops below a certain level, is forcing a programmed voltage.

CONTROLLED VELOCITY HEAD PARKING



HEAD PARKING WITH LOW BACK EMF



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