UNITRODE

UC1633
UC2633
UC3633

Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

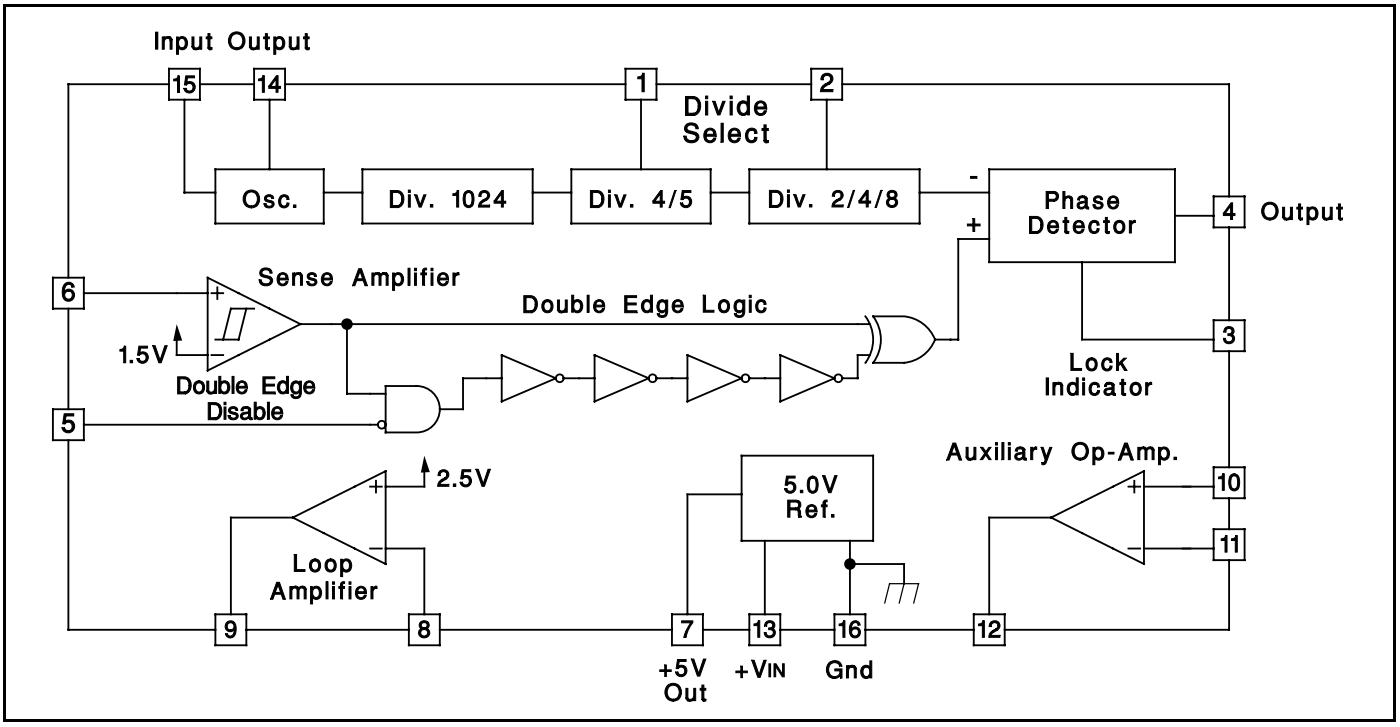
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output of other speed detection device. This signal is buffered by a sense ampilfier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of the op-amps will source or sink in excess of 16mA, so they can provide a low impedence control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM

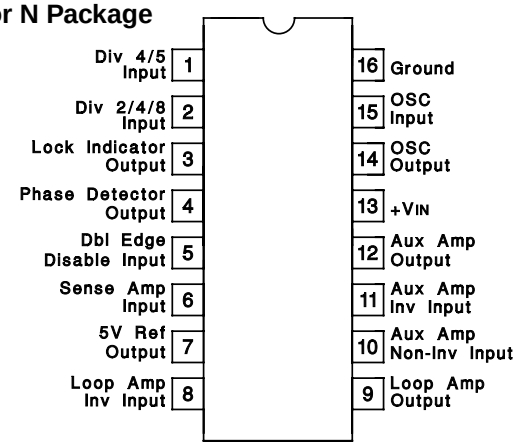


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ($+V_{IN}$) . . . . . +20V
Reference Output Current . . . . . -30mA
Op-Amp Output Currents . . . . . ±30mA
Op-Amp Input Voltages . . . . . -.3V to +20V
Phase Detector Output Current . . . . . ±10mA
Lock Indicator Output Current . . . . . +15mA
Lock Indicator Output Voltage . . . . . +20V
Divide Select Input Voltages . . . . . -.3V to +10V
Double Edge Disable Input Voltage . . . . . -.3V to +10V
Oscillator Input Voltage . . . . . -.3V to +5V
Sense Amplifier Input Voltage . . . . . .3V to +20V
Power Dissipation at T_A = 25°C (Note 2 . . . . . 1000mW
Power dissipation at T_C = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

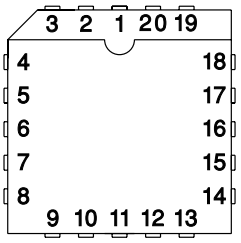
Note1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-16 (TOP VIEW)
J or N Package



CONNECTION DIAGRAMS

PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
Div 4/5 Input	2
Div 2/4/8 Input	3
Lock Indicator Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
$+V_{IN}$	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V; T_A=T_J.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$+V_{IN}$ = 15V		20	28	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0V to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8V to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (V_{IB})	Oscillator Input Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	V_{IN} = V_{IB} ±0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = $1V_{PP}$ at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA
Div. 4/5 Threshold		0.5	1.6	2.2	V

Note 3: These impedence levels will vary with T_J at about 1700ppm/°C

ELECTRICAL CHARACTERISTICS (cont.): (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V; T_A=T_J.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dividers (cont.)					
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	v
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
CMRR	V_{CM} = 0V to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedence levels will vary with T_J at about 1700ppm/°C

APPLICATION AND OPERATING INFORMATION

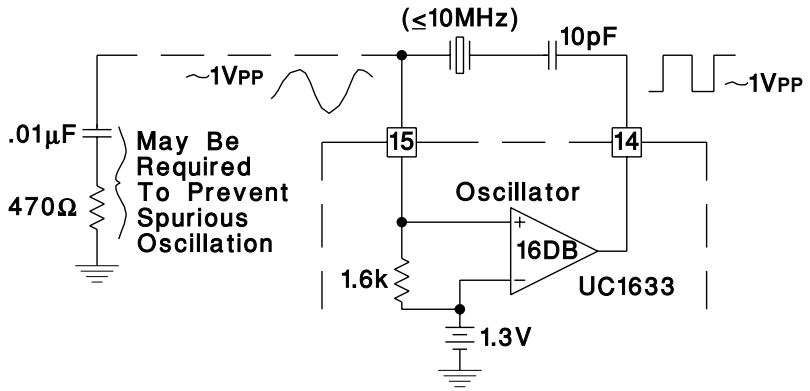
Determining the Oscillator Frequency

The frequency at the oscillator is determined by the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

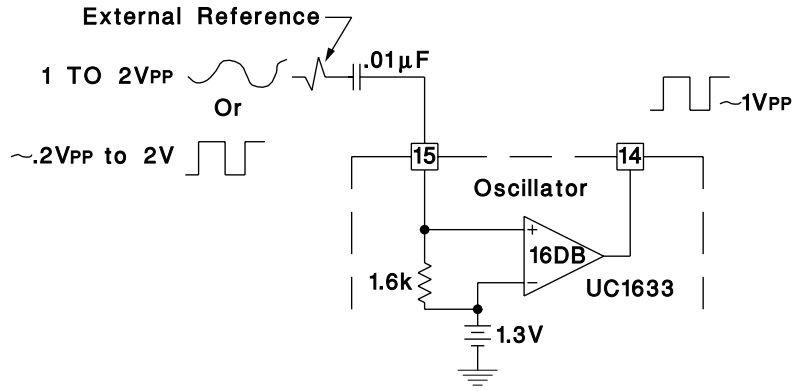
f_{OSC}(Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (x 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option, the loop reference frequency can be doubled for a given motor RPM.

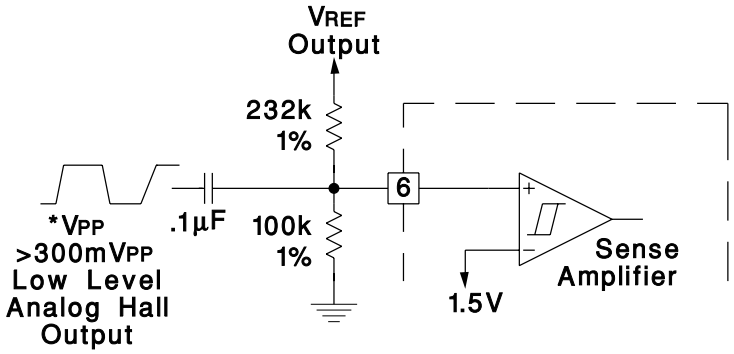
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method for Deriving Rotation Feedback Signal from Analog Hall Effect Device



**This signal may require filtering if chopped mode drive scheme is used.*

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

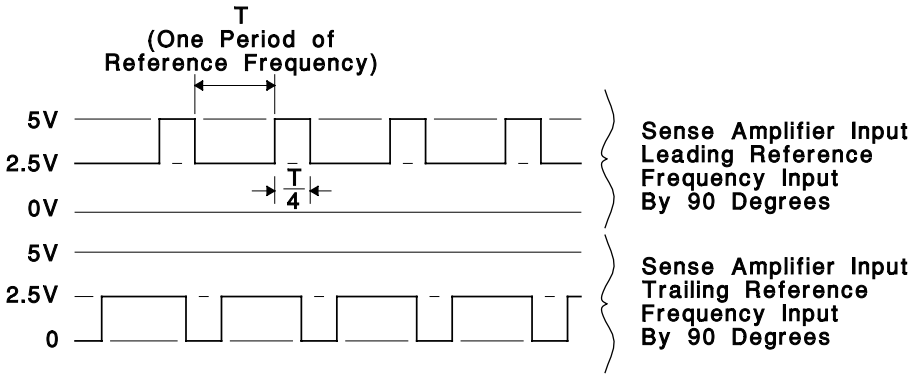
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low and the middle state output impedence is high, typically 6.0kΩ. When there is any static frequency difference between the inputs, the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal, the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level for the remainder of the period. If the phase relationship is reversed, then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector. kø, is 5V/4π radians or about 0.4V/radian. The dynamic range of the detector is ±2π radians.

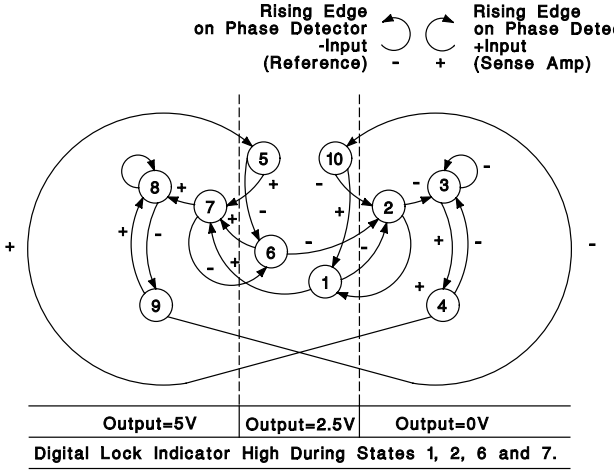
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic, and the connecting arrows represent the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge of the -input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from the frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

Typical Phase Detector Output Waveforms

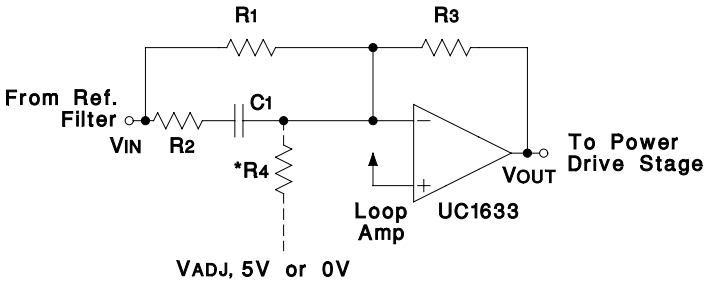


Phase Detector State Diagram



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{R_3}{R_1} \bullet \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{R_2 C_1}$$

$$\omega_z = \frac{1}{(R_1 + R_2)\, C_1}$$

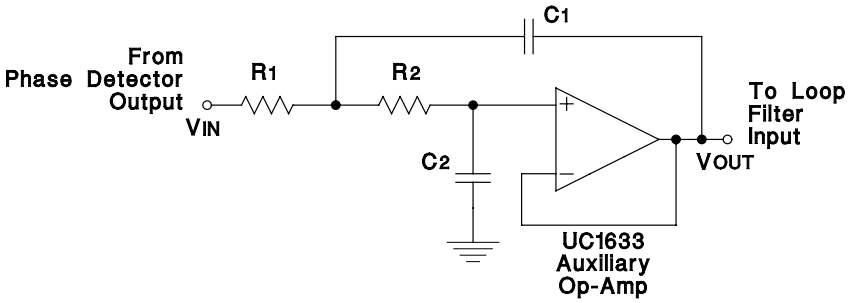
* The static phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R_4 = \frac{2.5V \bullet R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$, R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$, R4 Goes to 5.0V

Reference Filter Configuration



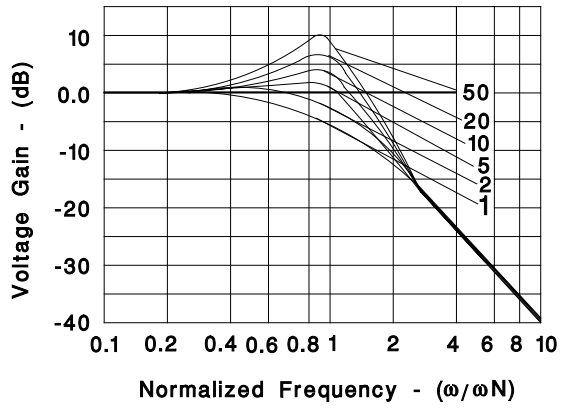
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s\,2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

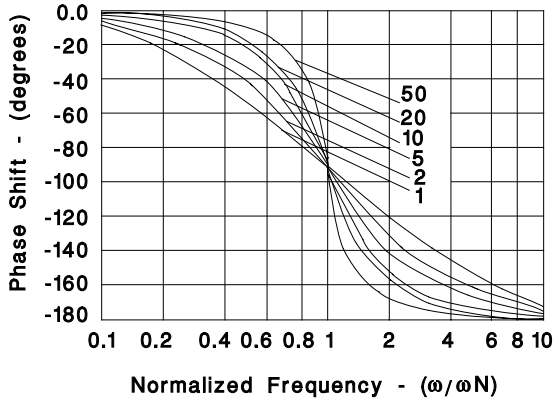
Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid - Gain Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

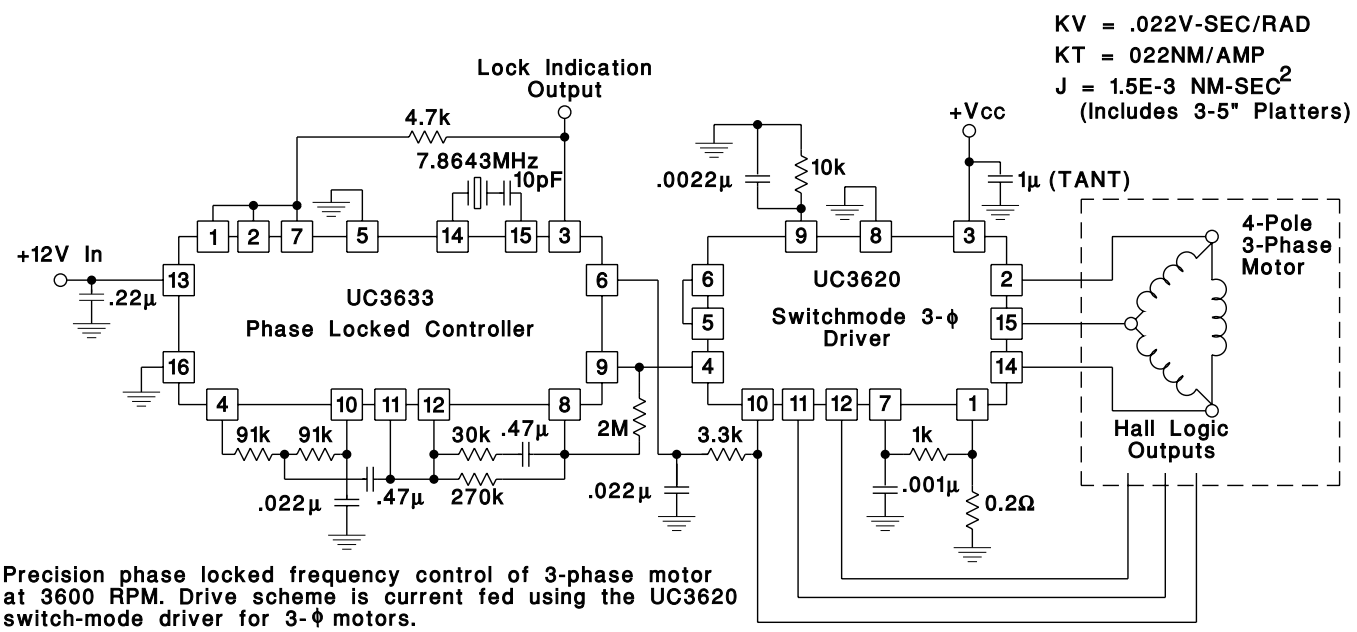
Reference Filter Design Aid - Phase Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

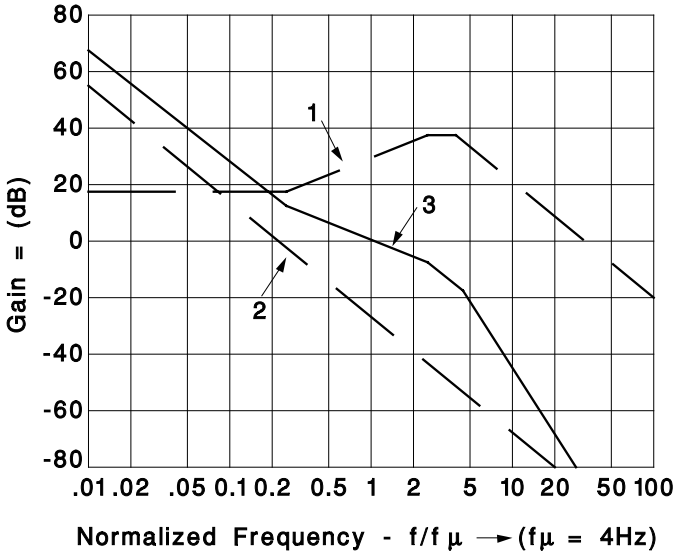
APPLICATION AND OPERATION INFORMATION

Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots - Design Example Open Loop Response



1.) $K_{LF}(s) \bullet K_{RF}(s)$

2.*) $\dfrac{N \bullet K\phi \bullet G_{PD} \bullet K_T}{s^2 \bullet J}$

3.) Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response
$K_{RF}(s)$ = Reference Filter Response
N = 4 (Using Double Edge Sensing With 4 Pole Motor)
$K\phi$ = Phase Detector Gain (.4V/RAD)
G_{PD} = Power Stage Transductance (1A/V)
K_T = Motor Torque Constant (.022NM/A)
J = Motor Moment of Inertia (.0015NM/A - SEC^2)
s = 2πjf

Note: For a current mode driver the electrical time constant, L_M / R_M, of the motor does not enter into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2 above, can be approximated by:*

$$\frac{N \bullet K\phi \bullet K_{PD} \bullet K_T}{s^2 \bullet J \bullet R_M} \quad \text{if: } R_M > K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T{}^2}{2\pi \bullet J \bullet R_M} < f < \frac{R_M}{2\pi \bullet L_M}$$

Here: K_{PD} = Voltage gain of Driver Stage
R_M = Motor Winding Resistance
L_M = Motor Winding Inductance

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