PRELIMINARY

Low Dropout 0.5A Negative Linear Regulator

FEATURES

- Precision Negative Series Pass Voltage Regulation
- 0.2V Drop Out at 0.5A
- Wide Input voltage Range -3.2V to -15V
- Low Quiescent Current Irrespective of Load
- Simple Logic Shutdown Interfacing
- -5V, -12V and Adjustable Output
- 3% Duty Cycle Short Circuit Protection
- Remote Load Sensing for Accurate Load Regulation
- 8-Pin DP Package

DESCRIPTION

The UCC384 family of negative linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input to output differential applications, the UCC384 will pass 0.5A while requiring only 0.2V of input voltage headroom. Drop out voltage decreases linearly with output current, so that drop out at 50mA is less than 20mV.

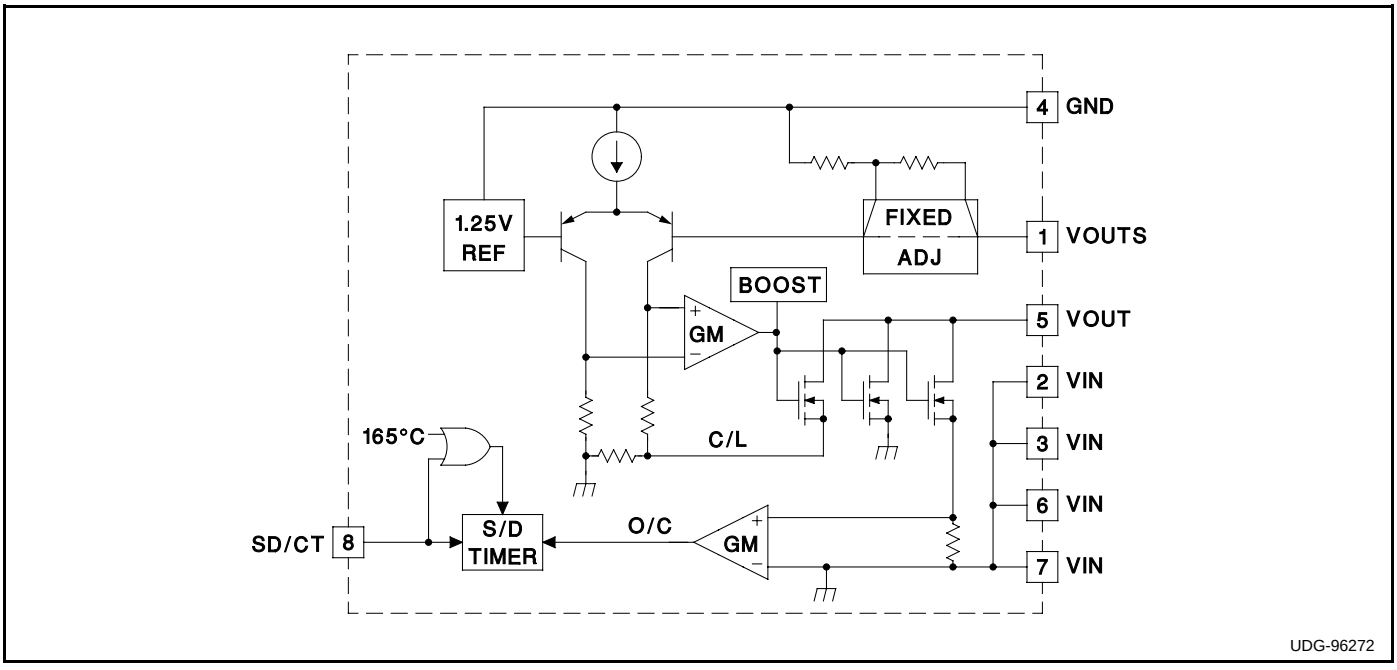
Quiescent current consumption for the device under normal (non-drop out) conditions is typically 200µA. An integrated charge pump is internally enabled only when the device is operating near drop out with low VIN. This guarantees that the device will meet the drop out specifications even for maximum load current and a VIN of –3.2V with only a modest increase in quiescent current. Quiescent current is always less than 350µA, with the charge pump enabled. Quiescent current of the UCC384 does not increase with load current.

Short circuit current is internally limited. The device responds to a sustained over current condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 32 times the T_{ON} delay. The device then begins pulsing on and off at the T_{ON}/T_{OFF} duty cycle of 3%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. An external capacitor sets the on time. The off time is always 32 times T_{ON}.

The UCC384 can be shutdown to 40µA (maximum) by pulling the SD/CT pin greater than –0.6V. To allow for simpler interfacing, the SD/CT pin may be pulled above the ground pin without turning on clamping diodes.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

BLOCK DIAGRAM



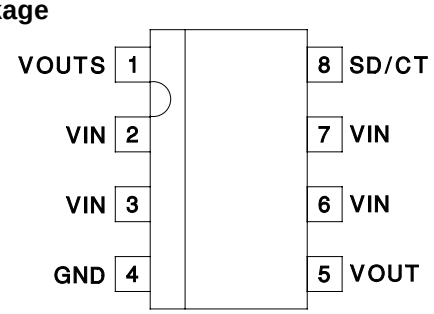
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VIN . . . . . –16VV
Shutdown Voltage . . . . . +6V to –5V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
UCC384-5 Fixed -5V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–5.075	–5	–4.925	V
	Overall Conditions	–5.125		–4.875	V
Line Regulation	VIN = –5.3V to –15V		0.004	0.011	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.1	0.25	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –4.85V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = –4.85V		20	50	mV
UCC384-5 Fixed -5V 0.5A Power Supply Section					
Input Voltage Range		–15		–5.2	V
Quiescent Current Charge Pump On	VIN = –4.85V (Note 1)		240	350	µA
Quiescent Current	VIN = –15V		200	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-5 Fixed -5V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Overcurrent Time Out, T_{ON}	VOUT = 0V	300	410	550	µs
UCC384-12 Fixed 12V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–12.18	–12	–11.82	V
	Overall Conditions	–12.30		–11.70	V
Line Regulation	VIN = –12.3V to –15V		0.010	0.027	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.24	0.60	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –11.85V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = –11.85V		20	50	mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284x, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
UCC384-12 Fixed -12V 0.5A Power Supply Section					
Input Voltage Range		–15		–12.2	V
Quiescent Current	VIN = –15V, SD/CT = 0		240	350	µA
Quiescent Current in Shutdown	VIN = –15V		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-12 Fixed -12V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Over Current Time Out, T_{ON}	VOUT = 0V	300	410	550	µs
UCC384-ADJ Adjustable 0.5A Regulation Section					
Reference Voltage	T_A = 25°C	–1.27	–1.25	–1.23	V
	Over Temperature	–1.28		–1.22	V
Line Regulation	VIN = –3.5V to –15V, VOUT = VOUTS		0.003	0.008	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.07	0.17	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –3.15V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = 3.15V		20	50	mV
Sense Pin Input Current			100	250	nA
UCC384-ADJ Adjustable 0.5A Power Supply Section					
Input Voltage Range		–15		–3.5	V
Undervoltage Lockout		–3.2		–2.8	V
Quiescent Current Charge Pump On	VIN = –3.15V (Note 1)		230	350	µA
Quiescent Current	VIN = –15V		190	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-ADJ Adjustable 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Over Current Time Out, T_{ON}	VOUT = 0V	300	410	550	µs

Note 1: Internal Charge Pump is enabled only for drop-out condition with low VIN. Only in this condition is the Charge Pump required to provide additional output FET gate drive to maintain drop-out specifications. For conditions where the Charge Pump is not required, it is disabled, which lowers overall device power consumption.

PIN DESCRIPTIONS

GND: This is the low noise ground reference input for regulation. All voltages are measured with respect to this pin.

SD/CT: For the UCC384-5/-12, this is the shutdown pin which, when pulled greater than –0.6V relative to GND, puts the device in a low current state. This pin is internally clamped to –1.5V via a 50kΩ source impedance. This input should not be externally driven more negative than –5V; otherwise device damage will result. For all versions, a capacitor is required between the SD/CT pin and GND to set the short circuit charging time, T_{ON} during overcurrent according to the following (typical) equation:

$$T_{ON} = 27{,}300 \bullet C_{CT}$$

Note: The SD/CT capacitor must be connected to ground, not VIN, to assure that SD/CT is not pulled significantly negative during power-up.

VIN: Negative input supply for the regulator. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance.

VOUT: This is the regulator output. A single 4.7µF output capacitor connected to GND will generally provide adequate loop compensation and load step transient response. Smaller output capacitors will degrade the load step performance of the regulator.

For a given compensation capacitor, regulator loop stability generally improves as the output load current increases. As well, there exists an inverse relationship between capacitance value and ESR. Namely, as the capacitor value decreases (tantalums and electrolytic), the ESR increases, which tends to keep the effective zero confined to a range of 1kHz to 100kHz. Thus, for load currents above 5mA, the device is stable for capacitor values below 1µF, as the increasing ESR keeps the zero frequency near the location of the on chip pole, which occurs at approximately 10kHz. Similarly, large capacitors also provide stability since their ESR's are falling.

The exact range of capacitor values and ESR's over which stability can be guaranteed is difficult to determine, because the load current becomes a variable in the equation. However, the device is stable for capacitor values ranging form 1µF and up, with ESR's up to 5Ω. Under some circumstances, even sub 1µF stability is possible for ESR's consistent with this size of capacitor.

VOUTS: Feedback for regulator sensing of the output voltage. For loads which are a considerable resistive distance form the VOUT pin, the VOUTS pin can be used to move the resistance into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path. For local regulation, merely connect this pin directly to VOUT. For the -ADJ (adjustable) device, the output voltage can be set by two external resistors according to the following relationship:

$$VOUT = -1.25 \bullet \left(1 + \frac{R1}{R2}\right)$$

where R1 is a resistor connected between VOUT and VOUTS and R2 is a resistor connected between VOUTS and GND. Because R1 and R2 will generally be quite large, a small lead cap should be placed across R1 to cancel the input pole created by R1 and the parasitic capacitance appearing on VOUTS. Values of approximately 20pF should be adequate.

APPLICATION INFORMATION

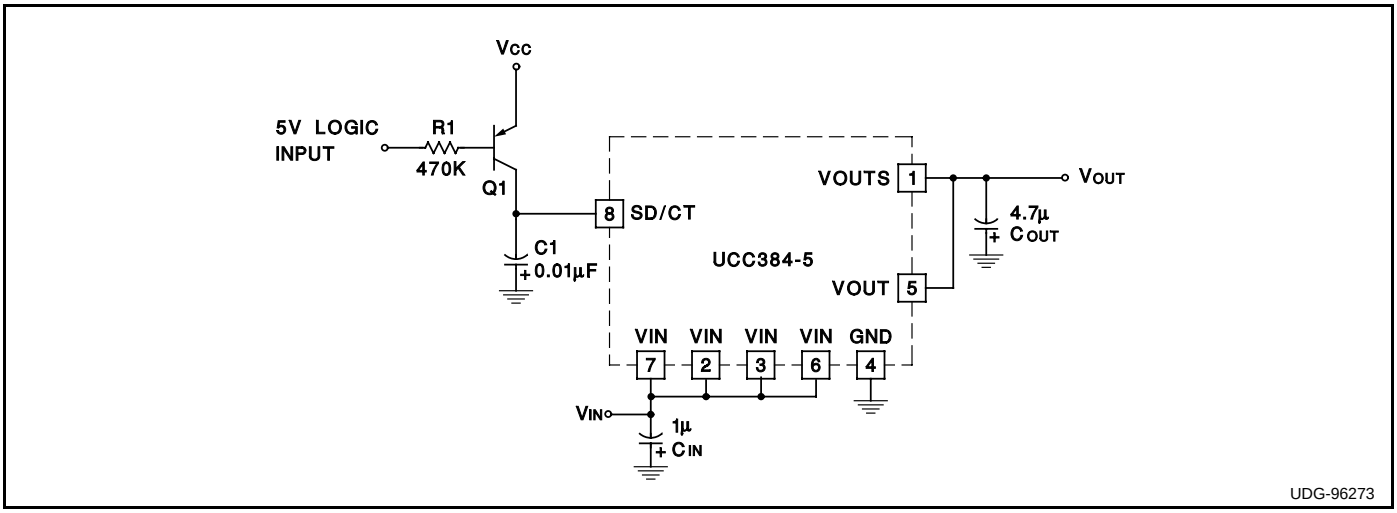


Figure 1. UCC384-5 Application Schematic

APPLICATION INFORMATION (cont.)

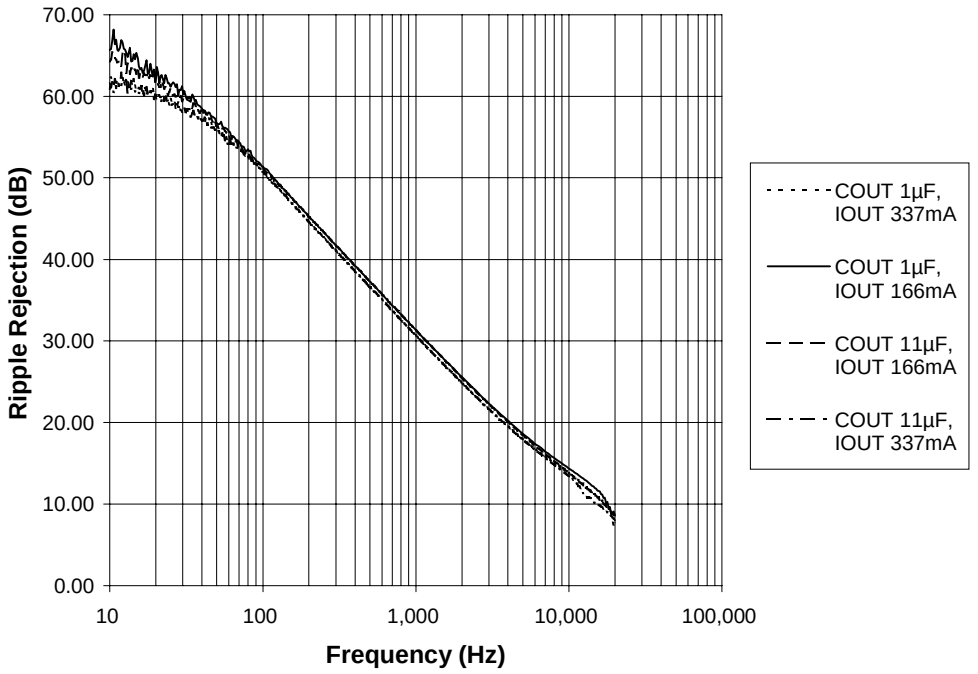


Figure 2. Ripple Rejection vs Frequency

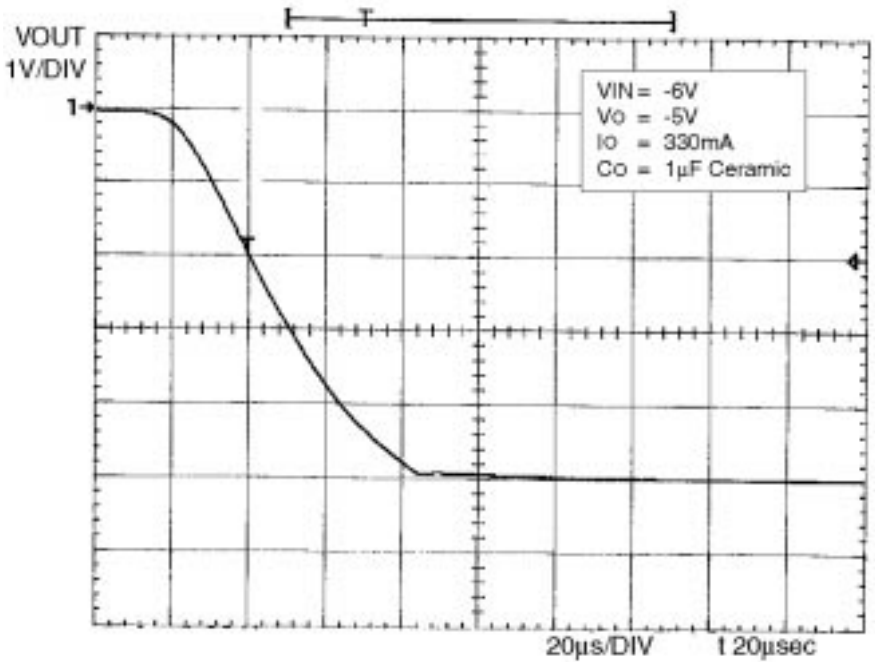


Figure 3. Typical Turn On Response

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