UNITRODE

UC1854A/B
UC2854A/B
UC3854A/B

Enhanced High Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Limits Line Current Distortion To <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed Frequency Average Current Mode Control
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Integrated Current and Voltage Amp Output Clamps
- Multiplier Improvements: Linearity, 500mV VAC Offset (eliminates external resistor), 0-5V Multout Common Mode Range
- V_{REF} "GOOD" Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Threshold Options (16/10V / 10.5/10V)
- 300µA Startup Supply Current

	UVLO Turn on	UVLO Turn off
UC1854A	16V	10V
UC1854B	10.5V	10V

DESCRIPTION

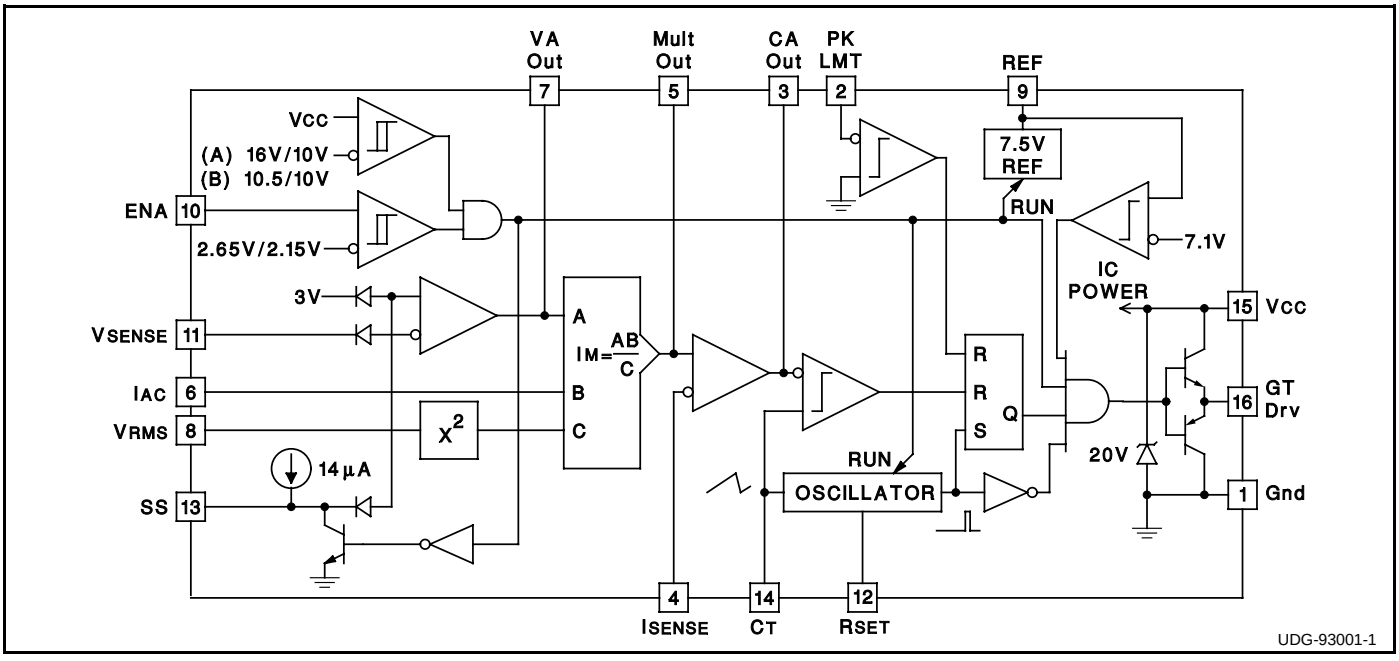
The UC1854A/B products are pin compatible enhanced versions of the UC1854. Like the UC1854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC1854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

The UC1854A/B products improve upon the UC1854 by offering a wide bandwidth, low offset Current Amplifier, a faster responding and improved accuracy enable comparator, a V_{REF} "good" comparator, UVLO threshold options (16/10V for offline, 10.5/10V for startup from an auxiliary 12V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the Multiplier output/Current Amp input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, R_{SET} controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 * I_{AC} at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

A 1% 7.5V reference, fixed frequency oscillator, PWM, Voltage Amplifier with softstart, line voltage feedforward (V_{RMS} squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16 pin N, DW, and J and 20 pin L and Q packages.

BLOCK DIAGRAM



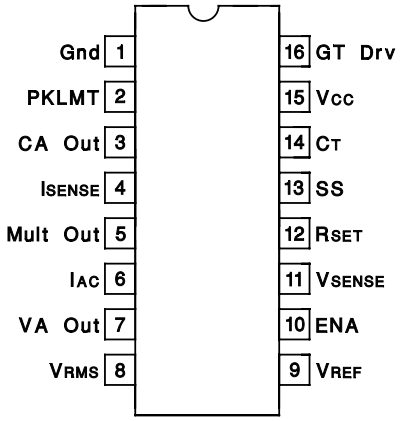
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 22V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, V_{SENSE}, V_{RMS} 11V
Input Voltage, I_{SENSE}, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, R_{SET}, I_{AC}, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

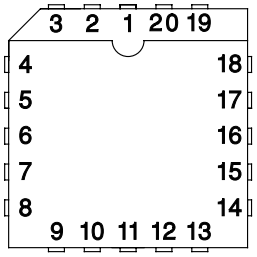
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA imput is internally clamped to approximately 10V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
I_{SENSE}	5
N/C	6
Mult Out	7
I_{AC}	8
VA Out	9
V_{RMS}	10
N/C	11
V_{REF}	12
ENA	13
V_{SENSE}	14
R_{SET}	15
N/C	16
SS	17
C_T	18
V_{CC}	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	CAO, VAO = 0V, V_{CC} = UVLO - 0.3V		250	400	µA
Supply Current, On			12	18	mA
V_{CC} Turn-On Threshold	UC1854A		16	17.5	V
	UC1854B		10.5	11.2	V
V_{CC} Turn-Off Threshold	UC1854A / B	9	10		V
V_{CC} Clamp	I(V_{CC}) = I_{CC}(on) + 5mA	18	20	22	V
VOLTAGE AMPLIFIER					
Input Voltage		2.9	3.0	3.1	V
V_{SENSE} Bias Current		–500	–25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	70	100		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3.5	mA
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		1		mHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER						
Input Offset Voltage	V_{CM} = 0V	T_A = +25°C	–4		0	mV
		OverTemp	–5.5		0	mV
Input Bias Current(sense)	V_{CM} = 0V		–500		500	nA
Open Loop Gain	V_{CM} = 0V, V_{OUT} = 2 to 6V		80	110		dB
V_{OUT} High	I_{LOAD} = –500µA			8		V
V_{OUT} Low	ILOAD = 500µA			0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V			1.5	3.5	mA
Common Mode Range			–0.3		5	V
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		3	5		mHz
REFERENCE						
Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.4	7.5	7.6	V
	I_{REF} = 0mA		7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA		0	8	20	mV
Line Regulation	V_{CC} = 12 to 18V		0	14	25	mV
Short Circuit Current	V_{REF} = 0V		25	35	60	mA
OSCILLATOR						
Initial Accuracy	T_A = 25°C		85	100	115	kHz
Voltage Stability	V_{CC} = 12 to 18V			1		%
Total Variation	Line, Temp		80		120	kHz
Ramp Amplitude (p-p)			4.9		5.9	V
Ramp Valley Voltage			0.8		1.3	V
ENABLE / SOFTSTART / CURRENT LIMIT						
Enable Threshold			2.5	2.65	2.8	V
Enable Hysteresis	V_{FAULT} = 2.5V			500	600	mV
Enable Input Bias Current	V_{ENABLE} = 0V			–2	–5	µA
Propagation Delay to Disable	Enable Overdrive = –100mV,(Note 1)			300		ns
SS Charge Current	$V_{SOFTSTART}$ = 2.5V		10	14	24	
PKLMT Offset Voltage			–15		15	mV
PKLMT Input Current	V_{PKLMT} = –0.1V		–200	–100		µA
PKLMT Propagation Delay	(Note 1)			150		ns
MULTIPLIER						
Output Current - I_{AC} Limited	I_{AC}=100µA, V_{RMS} = 1V, R_{SET} = 10k		–220	–200	–170	µA
Output Current - Zero	I_{AC}=0µA, R_{SET} = 10k		–2.0	–0.2	2.0	µA
Output Current - Power Limited	V_{RMS} = 1.5V, Va = 6V		–230	–200	–170	µA
Output Current	V_{RMS} = 1.5V, Va = 2V			–22		µA
	V_{RMS} = 1.5V, Va = 5V			–156		µA
	V_{RMS} = 5V, Va = 2V			–2		µA
	V_{RMS} = 5V, Va = 5V			–14		µA
Gain Constant	(Note 2) V_{RMS} = 1.5V, T_J = 25°C, Va = 6V		–1.1	–1.0	–0.9	A/A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \dfrac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^{\,2} \times I_{MO}}$

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER					
Output High Voltage	I_{OUT} = –200mA, V_{CC} = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V
Output Rise / Fall Time	C_{LOAD} = 1nF, (Note 1)		35		ns
Output Peak Current	C_{LOAD} = 10nF, (Note 1)		1.0		A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \frac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^2 \times I_{MO}}$

FUNCTIONAL DESCRIPTION

The UC1854A/B products were designed as pin compatible upgrades to the industry standard UC1854 active Power Factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC1854. In addition, linearity improvements to the Multiply, Square, and Divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to Unitrode application notes U-134 and DN-44.

MULTIPLY / SQUARE AND DIVIDE

The UC1854A/B Multiplier design maintains the same gain constant (K = –1), as the UC1854. The relationship between the inputs and output current is given as:

$$I_{MO} = I_{AC}(V_{AO} - 1.5V) / K \bullet V_{RMS}^2$$

This is nearly the same as the UC1854, but circuit differences have improved the performance and application.

The first difference is with the I_{AC} input. The UC1854A/B regulates this pin voltage to a nominal 500mV over the full operating temperature range, rather than the 6.0V used on the UC1854. This low offset voltage eliminates the need for a line zero crossing compensating resistor to V_{REF} from I_{AC} that UC1854 designs require. The maximum current at high line into I_{AC} should be limited to 250µA for best performance. Therefore, if V_{AC} (max) = 270V, then R_{AC} = 270(1.414) / 250µA = 1.53MΩ.

The V_{RMS} pin linear operating range is improved with the UC1854A/B as well. The input range for V_{RMS} extends from 0 to 5.5V. Since the UC1854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to V_{RMS} should produce 1.5V at low line (85VAC). This will put 4.77V on V_{RMS} at high line (27VAC) which is well within its operating range.

The Voltage Amplifier output forms the third input to the Multiplier and is internally clamped to 6.0V. This eliminates an external zenerclamp often used in UC1854 designs. The offset voltage at this input to the Multiplier has been raised on the UC1854A/B to 1.5V.

The Multiplier output pin, which is also common to the Current Amplifier non-inverting input, has a –0.3V to 5.0V output range,compared to the –0.3 to 2.5V range of the UC1854. This improvement allows the UC1854A/B to be used in applications where the current sense signal amplitude is very large.

VOLTAGE AMPLIFIER

The UC1854A/B Voltage Amplifier design is essentially similar to the UC1854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitor, which provides improved recovery from large signal events, such as line dropouts, or power interruption. It also minimizes the DC current flowing through the feedback. The output of the Voltage amplifier is also changed. In addition to a 6.0V temperature compensated clamp, the output short circuit current has been lowered to 2mA typical, and an active pull down has replaced the passive pulldown of the UC1854.

CURRENT AMPLIFIER

The Current Amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC1854A/B Current Amplifier has improved the input offset voltage from ±4mV to 0 to –3mV. The negative offset of the UC1854A/B guarantees that the PWM circuit will not drive the MOS-

FUNCTIONAL DESCRIPTION (cont.)

FET if the current command is zero (both Current amplifier inputs zero.).Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the Current Amplifier has been improved as well to 5mHz typical. While this is not generally an issue at 50 or 60Hz inputs, it is essential for 400Hz input avionics applications.

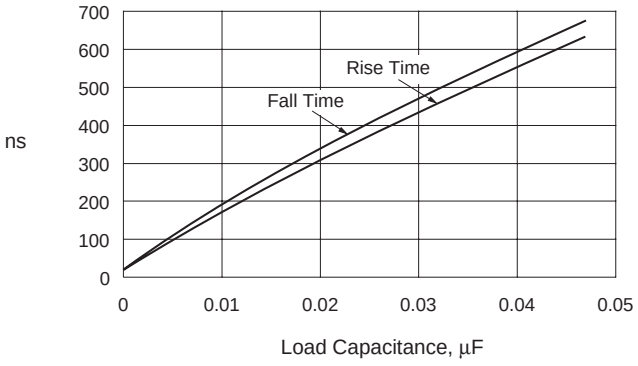
MISCELLANEOUS

Several other important enhancements have been implemented in the UC1854A/B. A V_{CC} supply voltage clamp at 20V allows the controller to be current fed if desired. The lower startup supply current (250µA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5/10V UVLO option (UC1854B) enables the controller to be powered off of an auxiliary 12V supply.

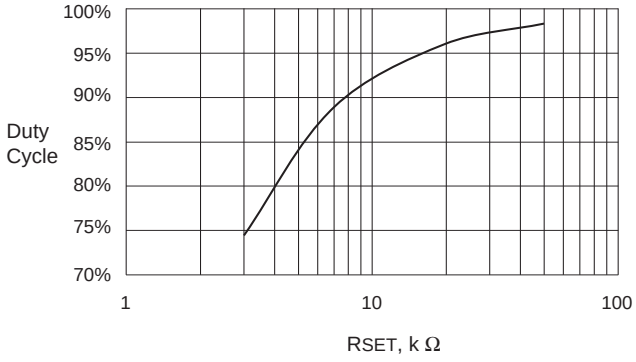
The V_{REF} "GOOD" comparator guarantees that the MOSFET driver output remains low if the supply or the 7.5V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKL and CA+ pins that some UC1854 designs require. The propagation delay of the disable feature has been improved to 300ns typical. This delay was proportional to the size of the V_{REF} capacitor on the UC1854, and is typically several orders of magnitude slower.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

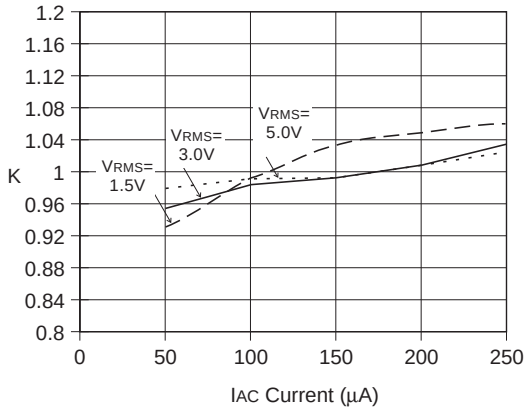
Gate Drive Rise and Fall Time



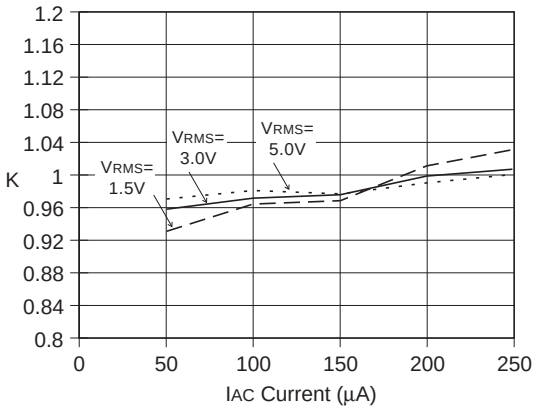
Gate Drive Maximum Duty Cycle



UC1854A/B Multiplier Linearity
V_{AOUT} = 3.5V

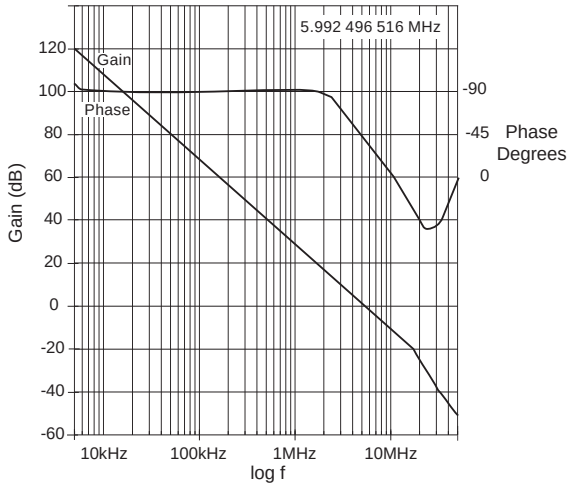


UC1854A/B Multiplier Linearity
V_{AOUT} = 5V

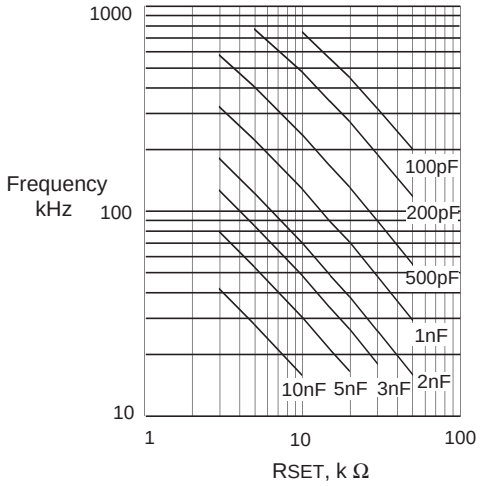


TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$ (cont.)

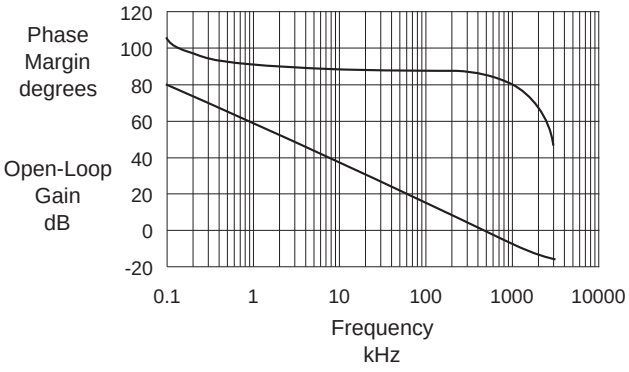
Current Amplifier Frequency Response



Oscillator Frequency vs R_{SET} and C_T



Voltage Amplifier Gain and Phase vs Frequency



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