The UCC3857 provides all of the control functions necessary for an Isolated Boost PFC Converter. These converters have the advantage of transformer isolation between primary and secondary, as well as an output bus voltage that is lower than the input voltage. By providing both power factor correction and down conversion in a single power processing stage, the UCC3857 is ideal for applications which require high efficiency, integration, and performance.

The UCC3857 brings together the control functions and drivers necessary to generate overlapping drive signals for external IGBT switches, and provides a separate output to drive an external power MOSFET which provides zero current switching (ZCS) for both the IGBTs. Full programmability is provided for the MOSFET driver delay time with an external RC network. ZCS for the IGBT switches alleviates the undesirable turn off losses typically associated with these devices. This allows for higher switching frequencies, smaller magnetic components and higher efficiency. The power factor correction (PFC) portion of the UCC3857 employs the familiar average current control scheme used in previous Unitrode controllers. Internal circuitry changes, however, have simplified the design of the PFC section and improved performance.

Controller improvements include an internal 6 bit A-D converter for RMS input line voltage detection, a zero load power circuit, and significantly lower quiescent operating current. The A-D converter eliminates an external 2 pole low pass filter for RMS detection.
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN, VD) ....................... 18V
General Analog/Logic Inputs
  (Maximum Forced Voltage) ..................... –0.3V to 5V
IAC (Maximum Forced Current) ....................... 200µA
Reference Output Current ...................... Internally Limited
Output Current (MOSDRV, IGDRV1, IGDRV2)
  Pulsed ........................................ 1A
  Continuous ................................ 200mA
Storage Temperature ...................... –65°C to +150°C
Junction Temperature ...................... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ............. +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

DESCRIPTION (cont.)

This simplifies the converter design, eliminates 2nd harmonic ripple from the feedforward component, and provides an approximate 6 times improvement in input line transient response. The zero load power comparator prevents energy transfer during open load conditions without compromising power factor at light loads. Low startup and operating currents which are achieved through the use of Unitrode’s BCDMOS process simplify the auxiliary bootstrap supply design.

Additional features include: under voltage lockout for reliable off-line startup, a programmable over current shutdown, an auxiliary shutdown port, a precision 7.5V reference, a high amplitude oscillator ramp for improved noise immunity, softstart, and a low offset analog square, multiple and divide circuit. Like previous Unitrode PFC controllers, worldwide operation without range switches is easily implemented.

CONNECTION DIAGRAMS

DIL-20, SOIC-20 (Top View)
N Package, DW Package

PLCC-20 (Top View)
Q and L Packages
## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for \( T_A = 0°C \) to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, \( V_{IN}, V_D = 12V, RT = 19.2K, CT = 680pF \).

### PARAMETER TEST CONDITIONS MIN TYP MAX UNITS

#### Input Supply
- **Supply Current, Active**
  - No Load on Outputs, \( V_D = V_{IN} \)
  - \( 3.5 \) \( 5 \) mA
- **Supply Current, Startup**
  - No Load on Outputs, \( V_D = V_{IN} \)
  - 60 TBD \( \mu \)A
- **VIN UVLO Threshold**
  - 13.75 15.5 V
- **UVLO Threshold Hysteresis**
  - 3 3.75 TBD V

#### Reference
- **Output Voltage (VREF)** \( T_J = 25°C, I_{REF} = 1mA \)
  - 7.387 7.5 7.613 V
- **Over Temperature, UCC3857**
  - 7.368 7.5 7.631 V
- **Over Temperature, UCC1857, UCC2857**
  - 7.313 7.5 7.687 V
- **Load Regulation** \( I_{REF} = 1mA \) to 10mA
  - 2 10 mV
- **Line Regulation** \( V_{IN} = V_D = 12V \) to 16V
  - 2 15 mV
- **Short Circuit Current** \( V_{REF} = 0V \)
  - –55 –30 mA

#### Current Amplifier
- **Input Offset Voltage (Note 1)**
  - –3 0 3 mV
- **Input Bias Current (Note 1)**
  - –50 nA
- **Input Offset Current (Note 1)**
  - 25 nA
- **CMRR** \( V_{CM} = 0V \) to 1.5V, \( V_{CAO} = 3V \)
  - 80 dB
- **AVOL** \( V_{CM} = 0V, V_{CAO} = 2V \) to 5V
  - 65 85 dB
- **VOH**
  - Load on \( C_AO = 50\mu A, V_{MOUT} = 0V, V_{CA–} = 1V \)
  - 6 7 V
- **VOL**
  - Load on \( C_AO = 50\mu A, V_{MOUT} = 0V, V_{CA–} = 1V \)
  - 0.2 V
- **Maximum Output Current** Source : \( V_{CA–} = 0V, V_{MOUT} = 1V, V_{CAO} = 3V \)
  - –150 \( \mu \)A
  - Sink : \( V_{CA–} = 1V, V_{MOUT} = 0V, V_{CAO} = 3V \)
  - 5 30 50 mA
- **Gain Bandwidth Product** \( F_{IN} = 100kHz, 10mV \) p – p
  - 3 5 MHz

#### Voltage Amplifier
- **Input Voltage** Measured on \( V_{SNS}, V_{COMP} = 3V \)
  - 2.9 3 3.1 V
- **Input Bias Current** Measured on \( V_{SNS}, V_{COMP} = 3V \)
  - –50 nA
- **AVOL** \( V_{COMP} = 1V \) to 5V
  - 75 dB
- **VOH**
  - Load on \( V_{COMP} = -50\mu A, V_{SNS} = 2.8V \)
  - 5.3 5.55 5.7 V
- **VOL**
  - Load on \( V_{COMP} = 50\mu A, V_{SNS} = 3.2V \)
  - 0.1 0.45 V
- **Maximum Output Current** Source : \( V_{SNS} = 2.8V, V_{COMP} = 3V \)
  - –20 –12 –5 mA
  - Sink : \( V_{SNS} = 3.2V, V_{COMP} = 3V \)
  - 5 20 30 mA

#### Oscillator
- **Initial Accuracy** \( T_J = 25°C \)
  - 42.5 50 57.5 kHz
- **Voltage Stability** \( V_{IN} = 12V \) to 18V
  - 40 50 60 kHz
- **CT Ramp Peak-Valley Amplitude**
  - 4 4.5 5 V
- **CT Ramp Valley Voltage**
  - 1.5 V

#### Output Drivers
- **VOH** \( I_L = -100mA \)
  - 9 10 V
- **VOL** \( I_L = 100mA \)
  - 0.1 0.5 V
- **Rise Time** \( C_{LOAD} = 1nF \)
  - 25 TBD ns
- **Fall Time** \( C_{LOAD} = 1nF \)
  - 10 TBD ns
**PIN DESCRIPTIONS**

**AGND:** Reference point of the internal reference and all thresholds, as well as the return for the remainder of the device except for the output drivers.

**CA–:** Inverting input of the inner current loop error amplifier.

**CAO:** Output of the inner current loop error amplifier. This output can swing between approximately 0.2V and 6V. It is one of the inputs to the PWM comparator.

**COMP:** This is the output of the voltage loop error amplifier. It is internally clamped to approximately 5.6V by the UCC3857 and can swing as low as approximately 0.1V. Voltages below 0.5V on COMP will disable the MOSDRV output and force the IGDRV1 and IGDRV2 outputs to a zero overlap condition.

**CRMS:** A capacitor is connected between CRMS and ground to average the AC line voltage over a half cycle. CRMS is internally connected to the RMS detection circuitry.

**CT:** A capacitor (low ESR, ESL) is tied between CT and ground to set the ramp generator switching frequency in conjunction with RT. The ramp generator frequency is approximately equal to:

\[
\frac{0.67}{RT \cdot CT}
\]

**DELAY:** A resistor to VREF and a capacitor to AGND are connected to DELAY to set the overlap delay time for the MOSDRV output stage. The overlap delay function can be disabled by removing the capacitor to AGND.

**IAC:** A resistor is connected to the rectified AC input line voltage from IAC. This provides the internal multiplier and the RMS detector with instantaneous line voltage information.

**IGDRV1:** Driver output for one of the two external IGBT power switches.

**IGDRV2:** Driver output for one of the two external IGBT power switches.

**MOSDRV:** Driver output for the external power MOSFET switch.

**MOUT:** Output of the analog multiply and divide circuit. The output current from MOUT is fed into a resistor to the return leg of the input bridge. The resultant waveform forms the sine reference for the current error amplifier.

**PKLMT:** Inverting input of the peak current limit comparator. The threshold for this comparator is nominally set to 0V. The peak limit comparator terminates the MOSDRV output and forces the IGDRV1 and IGDRV2 outputs to zero overlap when tripped.

**PGND:** Return for all high level currents, internally tied to the output driver stages of the UCC3857.
RT: A resistor is tied between RT and ground to set the charging current for the internal ramp generator. The UCC3857 provides a temperature compensated 3.0V at RT. The oscillator charging current is therefore: 3.0V/RT. Current out of RT should be limited to 250µA for best performance.

SNS: This is the feedback input for the outer voltage control loop. An external opto isolator circuit provides the output voltage regulation information to SNS across the isolation barrier.

SS: A capacitor is connected between SS and GND to provide the UCC3857 soft start feature. The voltage on COMP, is clamped to approximately the same voltage as SS. An internal 10µA (nominal) current source is provided by the UCC3857 to charge the soft start capacitor.

VD: Positive supply rail for the three output driver stages. The voltage applied to VD must be limited to less than 18VDC. VD should be bypassed to PGND with a 0.1µF to 1.0µF low ESR, ESL capacitor for best results. VD and VIN can be isolated from each other with an RC lowpass filter for better supply noise rejection.

VIN: Input voltage supply to the UCC3857. This voltage must be limited to less than 18VDC. The UCC3857 is enabled when the voltage on VIN exceeds 13.75V (nominal).

VREF: Output of the precision 7.5V reference. A 0.01µF to 0.1µF low ESR, ESL bypass capacitor is recommended between VREF and AGND for best performance.

APPLICATION INFORMATION

UCC3857 is designed to provide a solution for single stage power factor correction and step-down function using an isolated boost converter. Figure 2 shows the implementation of a typical isolated boost converter using IGBTs as main switches in push-pull configuration and using a MOSFET as an auxiliary switch to accomplish soft-switching of IGBTs. Many variations of this implementation are possible including bridge-type circuits.

The circuit shown in Fig. 2 provides several advantages over a more conventional approach of deriving a DC bus voltage from AC line with power factor correction. The conventional approach uses two power conversion stages and has higher cost and complexity. With the use of UCC3857, the dual functionality of power factor correction and voltage step-down is combined into a single stage.

The power stage comprises a current-fed push-pull converter where the ON times of the push-pull switches (Q1 and Q2) are overlapped to provide effective duty cycle of a conventional PWM boost converter. When only one switch is on, the power is transferred to the output through the transformer and the output rectifier. It can be seen that the operation on the primary side of the circuit is that of a boost converter and UCC3857 provides input
current programming using average current mode control to achieve unity power factor. The transformer turns ratio can be used to get the required level of output voltage (higher or lower than the peak line voltage). The transformer also provides galvanic isolation for the output voltage.

Power stage optimization involves design and selection of components to meet the performance and cost objectives. These include the power switches, transformer and inductor design.

The choice of IGBTs is based on their advantage over MOSFETs at higher voltages. For universal line operation, the voltage stress on the push-pull switches can approach 1000V. However, the slow turn-off of IGBTs can contribute high switching losses and the use of MOSFET (QA) helps turn the IGBTs off under zero voltage (lossless) conditions. This is accomplished by keeping QA on beyond the turn-off of Q1 or Q2 (see Figure 1 for waveforms) to allow the inductor current to divert from IGBT to MOSFET while the IGBT is turning off and still maintain zero volts. The MOSFET delay time (TD1) effectively adds to the boost inductor charge period. The voltage stress of the MOSFET is half the stress of the IGBTs under normal operating conditions. However, QA can see much higher voltage stress under start-up and short circuit conditions as the converter operates in a flyback mode then. For different operating requirements or constraints (e.g. single North American line operation), the choice of switching components may be different (e.g. MOSFETs for Q1 and Q2 and no QA) as the voltage stress is different. In that case, UCC3857 can still be used without using the MOSDRV output.

Transformer design is very critical in this topology. The push-pull transformer has to have minimal leakage inductance between the primary and secondary windings. Similarly, the leakage between the two primary windings has to be minimized. In practice, it is hard to achieve both the targets without using sophisticated construction techniques such as interleaving, use of foils etc. In many cases, it may be beneficial to have planar transformers to achieve these objectives. The effects of higher leakage inductance include higher voltage stresses, ringing, power losses and loss of available duty cycle. The high voltage

![Figure 2. Typical Application Circuit](UDG-96136)
levels make it difficult to design effective snubber circuits for these leakage induced ringings.

The design of the boost inductor is very similar to conventional boost converter. However, as shown in Fig. 2, an additional winding connected to the output through a diode is required on the boost inductor. This winding has to have the same turns ratio as the transformer and meet the isolation requirements. This winding is required to provide a discharge path for the inductor energy when the push-pull switches are both off. During start-up, when the output voltage is zero, the converter can see very high inrush currents. The overcurrent protection circuit of UCC3857 will shut down all the outputs when the set threshold is crossed. At that instance, the boost inductor auxiliary winding directs the energy to the output. This is a preferred manner of bringing the output voltage up to prevent the main switches from handling the high levels of inrush current. However, when the auxiliary winding is transferring the power to the output, the voltage stress across QA becomes input voltage plus the reflected output voltage—higher than its steady state value of reflected output voltage.

Chip Bias Supply and Start-up

UCC3857 is implemented using Unitrode’s BCDMOS process which allows minimization of the start-up (60µA typical) and operating (3.5mA typical) supply currents. It results in significantly lower power consumption in the trickle charge resistor used to start-up the IC.

Oscillator Set-up

The oscillator of UCC3857 is designed to have a wide ramp amplitude (4.5V p–p) for higher noise immunity. The CT pin has the sawtooth waveshape and during the discharge time of CT, a clock pulse is generated. During the discharge period, the effective internal impedance to GND is 600Ω. Based on this, the discharge time is given by 831•CT. As shown in the waveforms of Fig. 1, the internal clock pulse width is equal to the discharge time and that sets the minimum dead time between IGDRV1 and IGDRV2. The clock frequency is given by

$$f_{SW} = \frac{1}{(1.5 \cdot RT + 831) \cdot CT} = \frac{1}{(1.5 \cdot RT \cdot CT)} \tag{1}$$

The IGDRV1 and IGDRV2 outputs are switched at half the clock frequency while MOSDRV is switched at the clock frequency.

Reference Signal (IMULT) generation

Like the UC3854 series, the UCC3857 has an analog computation unit (ACU) which generates a reference current signal for the current error amplifier. The inputs to the ACU are signals proportional to instantaneous line voltage, input voltage RMS information and the voltage error amplifier output. Unlike prior techniques of RMS voltage sensing, UCC3857 employs a patent pending technique to simplify the RMS voltage generation and eliminate performance degradation caused by the prior techniques. With the novel technique (shown in Figure 3), need for external 2-pole filter for VRMS generation is eliminated. Instead, the IAC current is mirrored and used to charge an external capacitor (CCRMS) during a half cycle. The voltage on CRMS takes the integrated sinusoidal shape and is given by equation 2. At the end of the half-cycle, CRMS voltage is held and converted into a 6-bit digital word for further processing in the ACU. CCRMS is discharged and readied for integration during next half cycle.

The advantage of this method is that the second harmonic ripple on the VRMS signal is virtually eliminated. Such second harmonic ripple is unavoidable with the limited roll-off of a conventional 2-pole filter and results in 3rd harmonic distortion in the input current signal. The dynamic response to the input line variations is also improved as a new VRMS signal is generated every cycle.

$$V_{CRMS} = \frac{I_{AC}(pk)}{2 \cdot \omega \cdot CRMS} \cdot (1 - \cos \omega t) \tag{2}$$

For proper operation, $I_{AC}(pk)$ should be selected to be 100µA at peak line voltage. For universal input voltage with peak value of 265 VAC, this means $RAC=3.6M$. The noise sensitivity of the IC requires a small bypass capacitor for high frequency noise filtering. The value of this capacitor should be limited to 220pF maximum. The VCRMS value should be approximately 1V at the peak of low line (80 VAC) to minimize any digitization errors. The peak value of VCRMS at high line then becomes 3.5V. The desired VCRMS can be calculated from equation 2 to be 75nF for 60Hz line.

The multiplier output current is given by equation (3) with $K=0.33$.

$$IMULT = \frac{(V_{COMP} - 0.5) \cdot I_{AC} \cdot K}{V_{CRMS}^2} \tag{3}$$

The multiplier peak current is limited to 200µA and the selected values for IAC and VCRMS should ensure that the current is within this range. Another limitation of the multiplier is that IMULT can not exceed two times the IAC current, limiting the minimum voltage on VCRMS.

The discrete nature of the RMS voltage feedforward means that there are regions of operation where the input voltage changes, but the VRMS value fed into the multiplier does not change. The voltage error amplifier compensates for this by changing its output to maintain
the required multiplier output current. When the output of the ADC changes, there is a jump in the output of the error amplifier. This has minimal impact on the overall converter operation.

Another key consideration with the RMS voltage scheme is that it relies on the zero-crossing of the Iac signal to be effective. At very light loads and high line conditions, the rectified AC does not quite reach zero if a large capacitor is being used for filtering on the rectified side of the bridge. In such instances, the feedforward effect does not take place and the controller functionality is compromised. For UCC3857, the Iac current should go below 10 µA for the zero crossing detection to take place. It is recommended that the capacitor value be kept low enough for the light load operation or that the alternative scheme shown in Figure 4 be used for Iac sense.

**Gate Drive Considerations**

The gate drive circuits in UCC3857 are designed for high speed driving of the power switches. Each drive circuit consists of low impedance pull-up and pull-down DMOS output stages. The UCC3857 provides separate supply and ground pins (VD and PGND) for the driver stages. These pins allow better local bypassing of the driver circuits. VD can also be used to ensure that the SOA limits of the output stages are not violated when driving high peak current levels. For this, VD can be kept as low as possible (e.g. 10V) while VIN can go higher to handle the UVLO requirements.

**Current Amplifier Set-up**

Once the multiplier is set-up by choosing the VRMS range, the current amplifier components can be designed. The maximum multiplier output is at low line, full load conditions. The inductor peak current also occurs at the same point. The multiplier terminating resistor can be determined using equation 4.

\[
R_{MULT} = \frac{I_{L_{PK}} \cdot R_{SENSE}}{I_{MULT_{PK}}}
\]

(4)

The current amplifier can be compensated using a previously presented techniques (U-134) summarized here. A
simplified high frequency model for inductor current to
duty cycle transfer function is given by
\[ G_{ID}(s) = \frac{\hat{i}_L}{d} = \frac{V_o}{sL} \] (5)
The gain of the current feedback path at the frequency of
interest (crossover) is given by
\[ \frac{d}{\hat{i}_L} = R_{SENSE} \cdot R_Z \cdot \frac{1}{R_i \cdot \text{VSE}} \] (6)

Where VSE is the ramp amplitude (p-p) which is 4.5V for
UCC3857. Combining equations 5 and 6 yields the loop
gain of the current loop and equating it to 1 at the de-
sired crossover frequency can result in a design value for
Rz. The current loop crossover frequency should be lim-
lited to about 1/3 of the switching frequency of the con-
verter to ensure stability. See Unitrode Application Note
U-140 for further information.

Trailing Edge Delay

As shown in the waveforms of Fig. 1, the modified iso-
lated boost converter requires drive signals for the two
main (IGBT) switches and the auxiliary (MOSFET) switch
with certain timing relationships. The delay between
turn-off of an IGBT and turn-off of the MOSFET can be
programmed for the UCC1857. In a PFC application, the
input line varies from zero to the AC peak level, resulting
in a wide range of required duty ratios. A fixed delay time
will induce line current distortion at the peaks of the AC
line under high line and/or light load conditions. This is
cased by the minimum controllable duty ratio imposed
on the modulator by the fixed delay. If the minimum con-
trollable duty ratio is fixed, the inner current loop can ex-
hibit a limit cycle oscillation at the line peaks, inducing
line current distortion.

The UCC1857 has an adaptive MOSFET delay gen-
erator, which is directly modulated by load power demand.
Referring to Fig. 5, this circuit directly varies the delay
time based on the output level of the voltage error ampli-
ifier, which in an average current mode PFC converter
with line feedforward is indicative of load power. The de-
lay time is programmed with external components, R0
and C0. The sequence of events starts when the internal
CLK signal resets latch U2, causing PWMDEL to go high
and the Q output to go low. C0 was discharged via M1
and is held low until the internal PWM signal goes low
(indicating turn-off of either of the IGBT drives). At this
point M1 turns off and C0 charges towards the 7.5V ref-
ence through R0. A comparator U1 compares this volt-
age to the voltage error amplifier output (VCOMP). When
the voltage on C0 is greater than VCOMP, the latch U2 is
set causing PWMDEL to go low. PWMDEL is logically
ANEd with CLKNOT to produce the signal, which com-
mands the MOSFET driver output (MOSDRV). The delay
time, TD1, is given by
\[ TD1 = -RD \cdot CD \cdot \frac{\ln \left( \frac{7.5 - V_{COMP}}{7.5} \right)}{R_D} \] (7)

This technique reduces the overlap delay at light loads or
high lines, but maintains a longer delay when the line
voltage is low or the load is heavy. This by definition re-
duces the minimum controllable duty ratio to an accept-
able level, and is programmable by the user. Reducing
the delay time under light current conditions is accept-
able since the IGBT current is directly proportional to
load current. By providing programming flexibility with R0
and C0, the delay times can be optimized for current and
future classes of IGBT switches. The delay can also be
set to zero by removing C0 from the circuit.