

Resonant Lamp Ballast Controller

FEATURES

- Controls Different Types of Lamps: Cold Cathode Fluorescent, Neon, and Gas Discharge
- Zero Voltage Switching (ZVS) of Push-Pull Drivers
- Accurate Control of Lamp Current
- Variable Lamp Intensity Control
- 1 μ A Disable Current
- 4.5V to 24V Operation
- Open Lamp Detection Circuitry

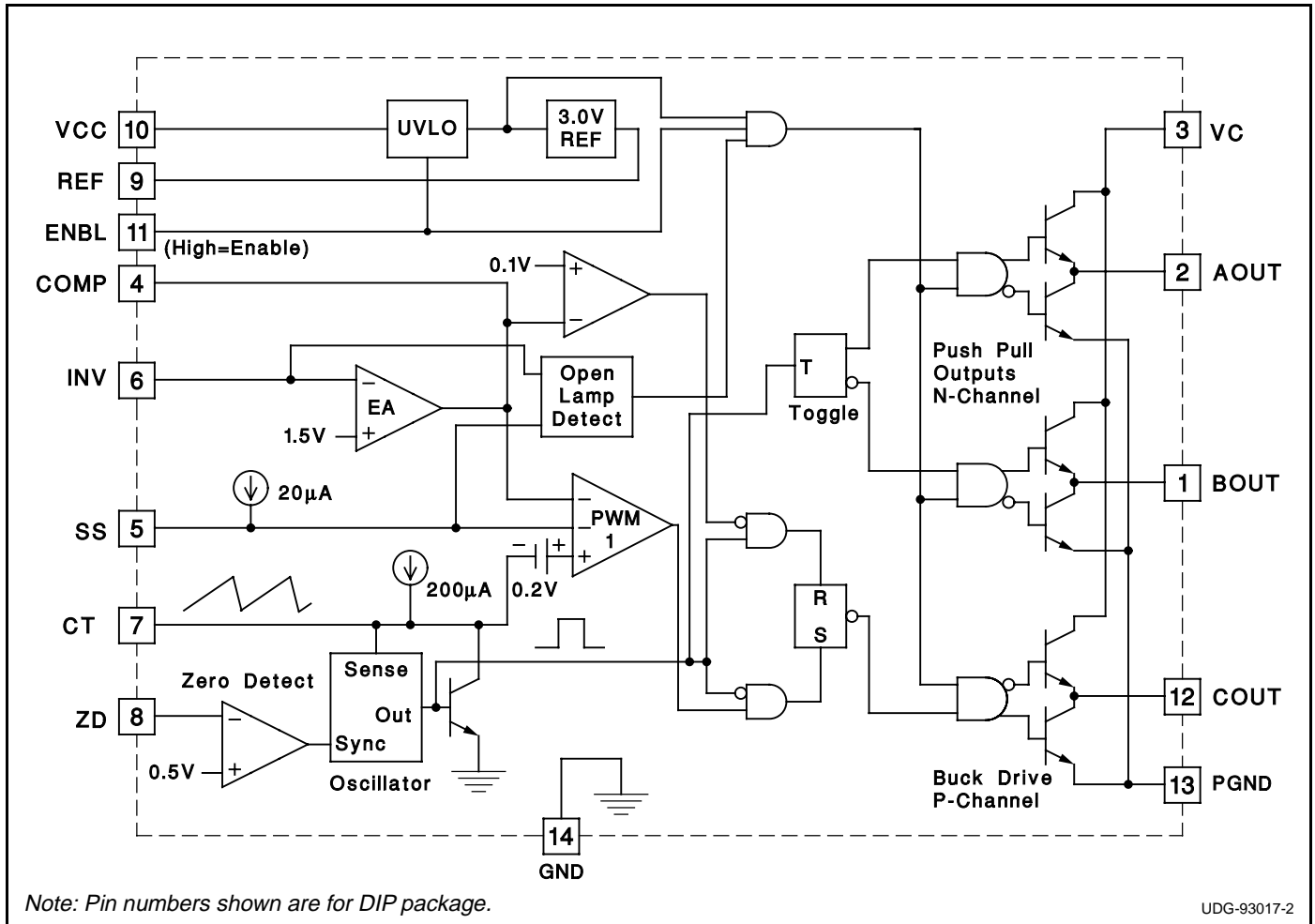
DESCRIPTION

The UC3872 is a resonant lamp ballast controller optimized for driving cold cathode fluorescent, neon, and other gas discharge lamps. The resonant power stage develops a sinusoidal lamp drive voltage, and minimizes switching loss and EMI generation. Lamp intensity adjustment is accomplished with a buck regulator, which is synchronized to the external power stage's resonant frequency. Suitable for automotive and battery powered applications, the UC3872 draws only 1 μ A when disabled.

Soft start and open lamp detect circuitry have been incorporated to minimize component stresses. Open lamp detection is enabled at the completion of a soft start cycle. The chip is optimized for smooth duty cycle control to 100%.

Other features include a precision 1.2% reference, undervoltage lockout, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

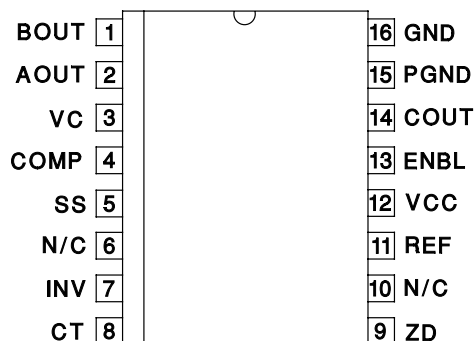
Analog Inputs	−0.3 to +10V
VCC, VC Voltage	+24V
ZD Input Current	
High Impedance Source	+10mA
ZD Input Voltage	
Low Impedance Source	+24V
Power Dissipation at TA = 25°C	1W
Storage Temperature	−65°C to +150°C
Lead Temperature	300°C

Note 1: Currents are positive into, negative out of the specified terminal.

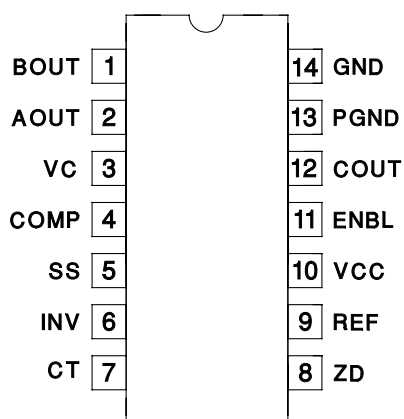
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

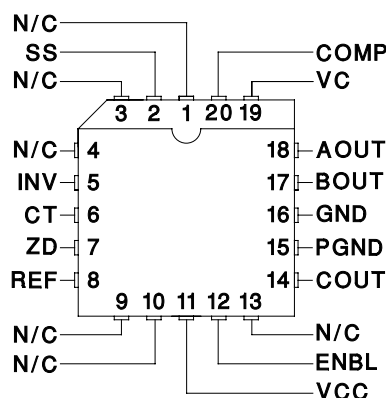
SOIC-16, SSOP-16 (TOP VIEW) DW, M Package



DIL-14 (TOP VIEW) N Package



PLCC-20 (Top View) Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for TJ = −55°C to +125°C for the UC1872, −40°C to +85°C for the UC2872, −0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, VENBL = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ = 25°C	2.963	3.000	3.037	V
	Over Temperature	2.940	3.000	3.060	V
Line Regulation	VCC = 4.75V to 18V			10	mV
Load Regulation	Io = 0 to −5mA			10	mV
Oscillator Section					
Free Running Frequency	TJ = 25°C	57	68	78	kHz
Maximum Synchronization Frequency	TJ = 25°C	160	200	240	kHz
Charge Current	VCT = 1.5V	180	200	220	μA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp Section					
Input Voltage	Vo = 2V	1.445	1.475	1.505	V
Input Bias Current			−0.4	−2	μA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	VINV = 1.3V	3.1	3.5	3.9	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these parameters apply for $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1872, -40°C to $+85^\circ\text{C}$ for the UC2872, -0°C to $+70^\circ\text{C}$ for the UC3872; $V_{CC} = 5\text{V}$, $V_C = 15\text{V}$, $V_{ENBL} = 5\text{V}$, $C_T = 1\text{nF}$, $Z_D = 1\text{V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Section (cont.)					
Output Low	$V_{INV} = 1.7\text{V}$		0.1	0.2	V
Output Source Current	$V_{INV} = 1.3\text{V}$, $V_o = 2\text{V}$	-350	-500		μA
Output Sink Current	$V_{INV} = 1.7\text{V}$, $V_o = 2\text{V}$	10	20		mA
Common Mode Range		0		$V_{IN}-1\text{V}$	V
Unity Gain Bandwidth	$T_J = 25^\circ\text{C}$ (Note 4)		1		MHz
Open Lamp Detect Section					
Soft Start Threshold	$V_{INV} = 0\text{V}$	2.9	3.4	3.8	V
Open Lamp Detect Threshold	$V_{SS} = 4.2\text{V}$	0.6	1.0	1.4	V
Soft Start Current	$V_{SS} = 2\text{V}$	10	20	40	μA
Output Section					
Output Low Level	$I_{OUT} = 0$, Outputs A and B		0.05	0.2	V
	$I_{OUT} = 10\text{mA}$		0.1	0.4	V
	$I_{OUT} = 100\text{mA}$		1.5	2.2	V
Output High Level	$I_{OUT} = 0$, Output C	13.9	14.9		V
	$I_{OUT} = -10\text{mA}$	13.5	14.3		V
	$I_{OUT} = -100\text{mA}$	12.5	13.5		V
Rise Time	$T_J = 25^\circ\text{C}$, $C_I = 1\text{nF}$ (Note 4)		30	80	ns
Fall Time	$T_J = 25^\circ\text{C}$, $C_I = 1\text{nF}$ (Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	$V_{INV} = 1\text{V}$	100			%
Out C Min Duty Cycle	$V_{INV} = 2\text{V}$			0	%
Under Voltage Lockout Section					
Startup Threshold Voltage		3.7	4.2	4.5	V
Hysteresis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	$V_{ENBL} = 5\text{V}$		150	400	μA
Supply Current Section					
VCC Supply Current	$V_{CC} = 24\text{V}$		6	14	mA
VC Supply Current	$V_C = 24\text{V}$		5	12	mA
ICC Disabled	$V_{CC} = 24\text{V}$, $V_{ENBL} = 0\text{V}$		1	10	μA

Note 3: Unless otherwise specified, all voltages are with respect to ground.

Currents are positive into, and negative out of the specified terminal.

Note 4: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AOUT, BOUT: These outputs provide complementary drive signals for the push-pull N-channel MOSFETs. Each one is high for 50% of the time, switching states each time a zero-detect is sensed.

COMP: COMP is the output terminal of the error amplifier. Compensation components are normally connected

between COMP and INV. Connecting a capacitor from this pin to ground limits turn on current and blanks the open lamp detect signal allowing the lamp to start.

COU: This output directly drives the bulk regulator P-channel MOSFET. COU turn-on is synchronized to each zero-detect, and therefore switches at twice the fre-

PIN DESCRIPTIONS

CT: A capacitor connected between this pin and GND sets the synchronization frequency range. The modulator controlling COUT is designed to provide smooth control up to 100% duty cycle.

VC: A capacitor connected between this pin and GND sets the synchronization frequency range. The capacitor is charged with approximately 200 μ A, creating a linear ramp which is used by COUT's (buck regulator driver) PWM comparator.

ENBL: When ENBL is driven high the device is enabled. When ENBL is pulled low, the IC is shut down and typically draws 1 μ A.

GND: This pin is the ground reference point for the internal reference and all thresholds.

INV: This pin is the inverting input to the error amplifier and the input for the open lamp detect circuitry. If the voltage at INV is below the 1V open lamp detect threshold, the outputs are disabled.

PGND: This pin is the high current ground connection for the three output drivers.

REF: This pin is connected to the 3V reference voltage which is used for the internal logic. Bypass REF to ground with a 0.01 μ F ceramic capacitor for proper operation.

VC: VC is the power supply voltage connection for the output drivers. Bypass it to ground with a 0.1 μ F ceramic capacitor for proper operation.

VCC: VCC is the positive supply voltage for the chip. Its operating range is from 4.2V to 24V. Bypass VCC to ground with a 0.1 μ F ceramic capacitor for proper operation.

ZD: The zero-detect input senses when the transformer's primary center tap voltage falls to zero to synchronize the sawtooth voltage waveform on CT. The threshold is approximately 0.5V, providing a small amount of offset such that with propagation delay, zero-volt switching occurs. A resistor (typically 10k) should be connected between ZD and the primary center tap to limit input current at turn off.

TYPICAL APPLICATION

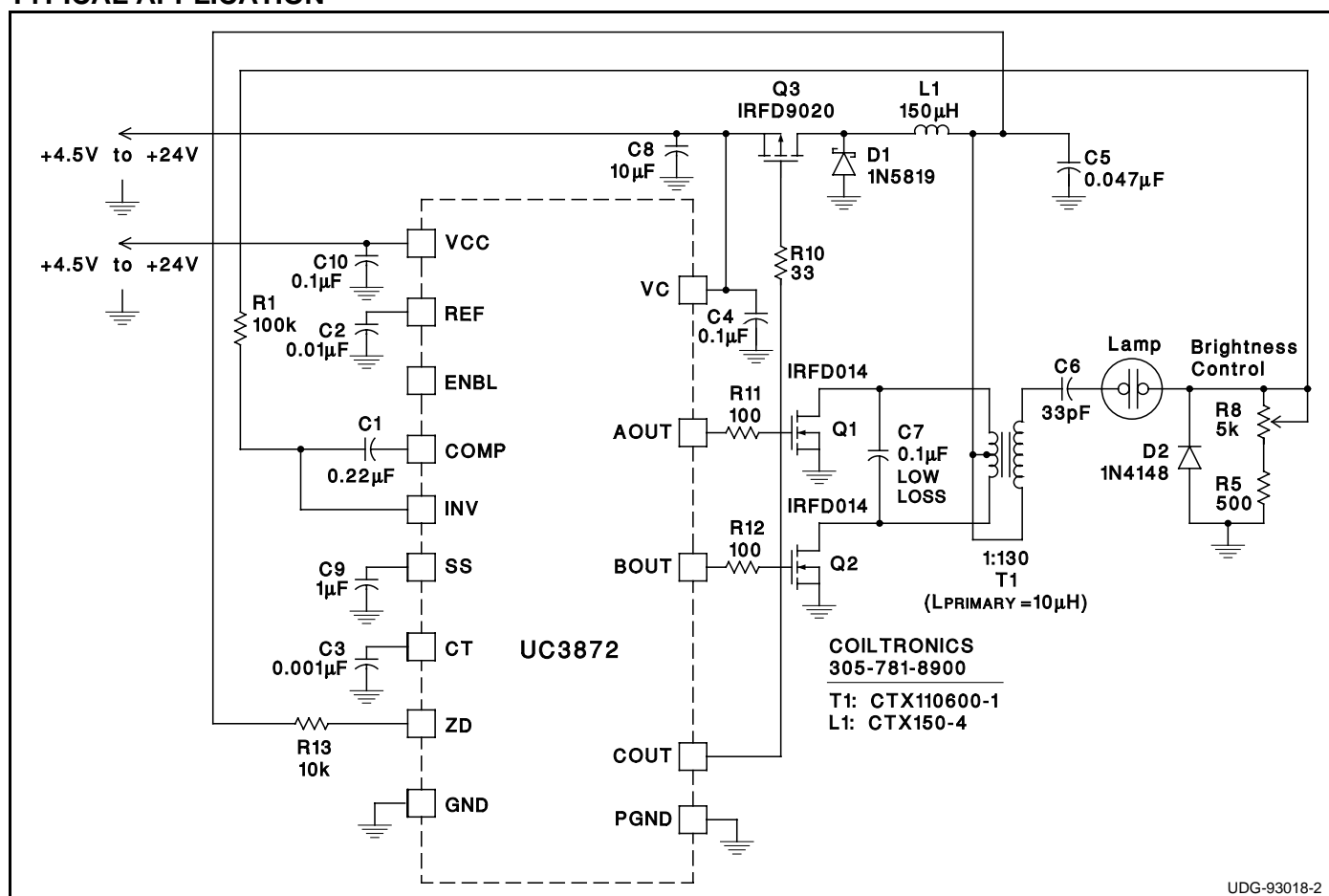


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3872 Resonant Lamp Ballast Controller. The IC provides all drive, control and housekeeping functions. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signals.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant wave-

form falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time required for the 4mA current sink to discharge the timing capacitor to 0.1 volts. This pulse width limits the minimum linear control range of the buck regulator. The 200 μ A current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

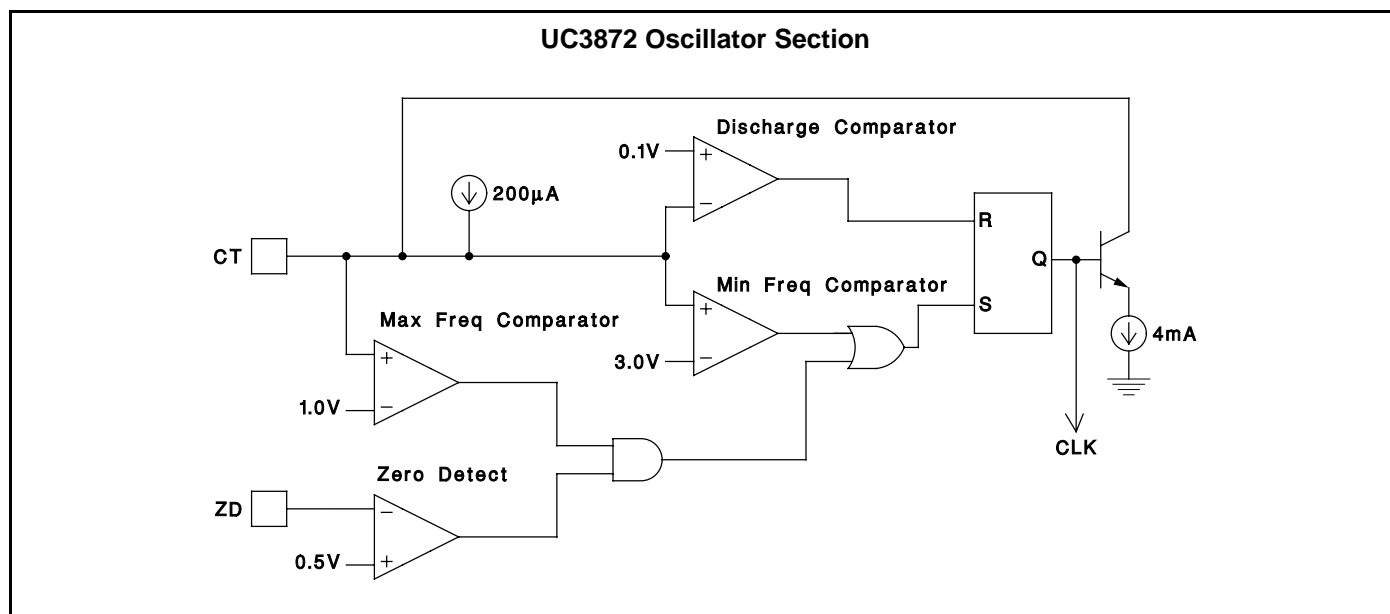


Figure 2

A unique protection feature incorporated in the UC3872 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifier's input, and shuts down the outputs if insufficient signal is present. Soft start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to a battery. During shutdown, the IC typically draws less than 1 μ A. The UC3872, operating from 4.5V to 24V, is compatible with almost all battery voltages used in portable computers and automotive applications. Undervoltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation.

APPLICATION INFORMATION (cont.)

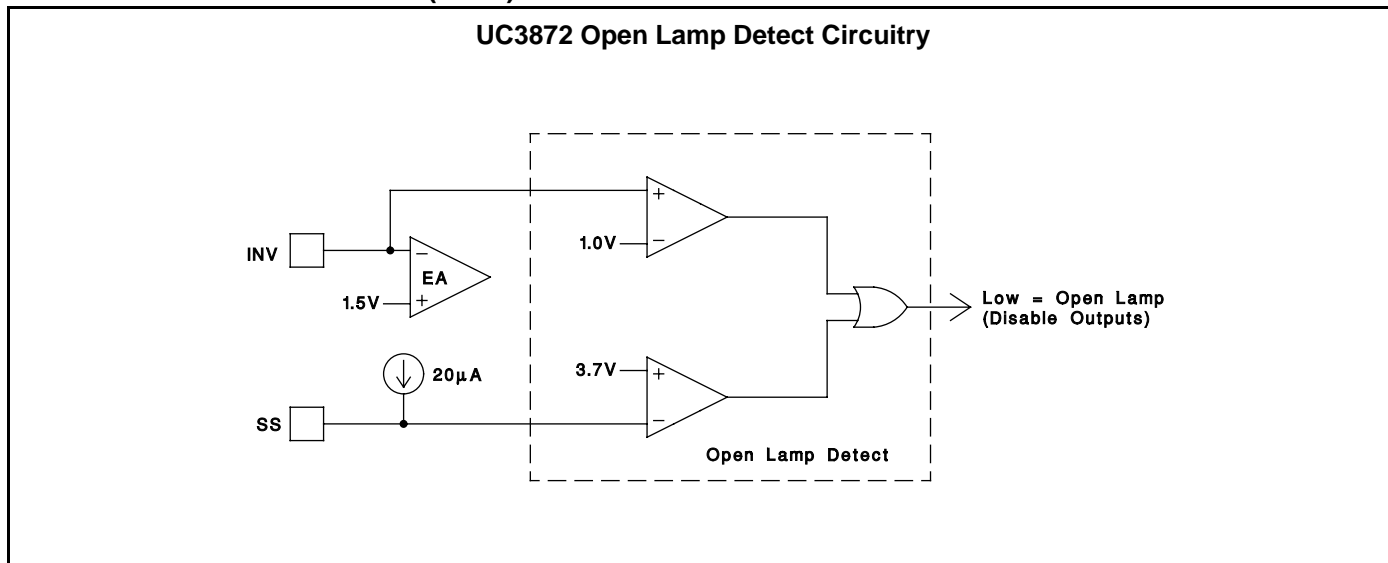


Figure 3