

Microprocessor Supervisor with Watchdog Timer

FEATURES

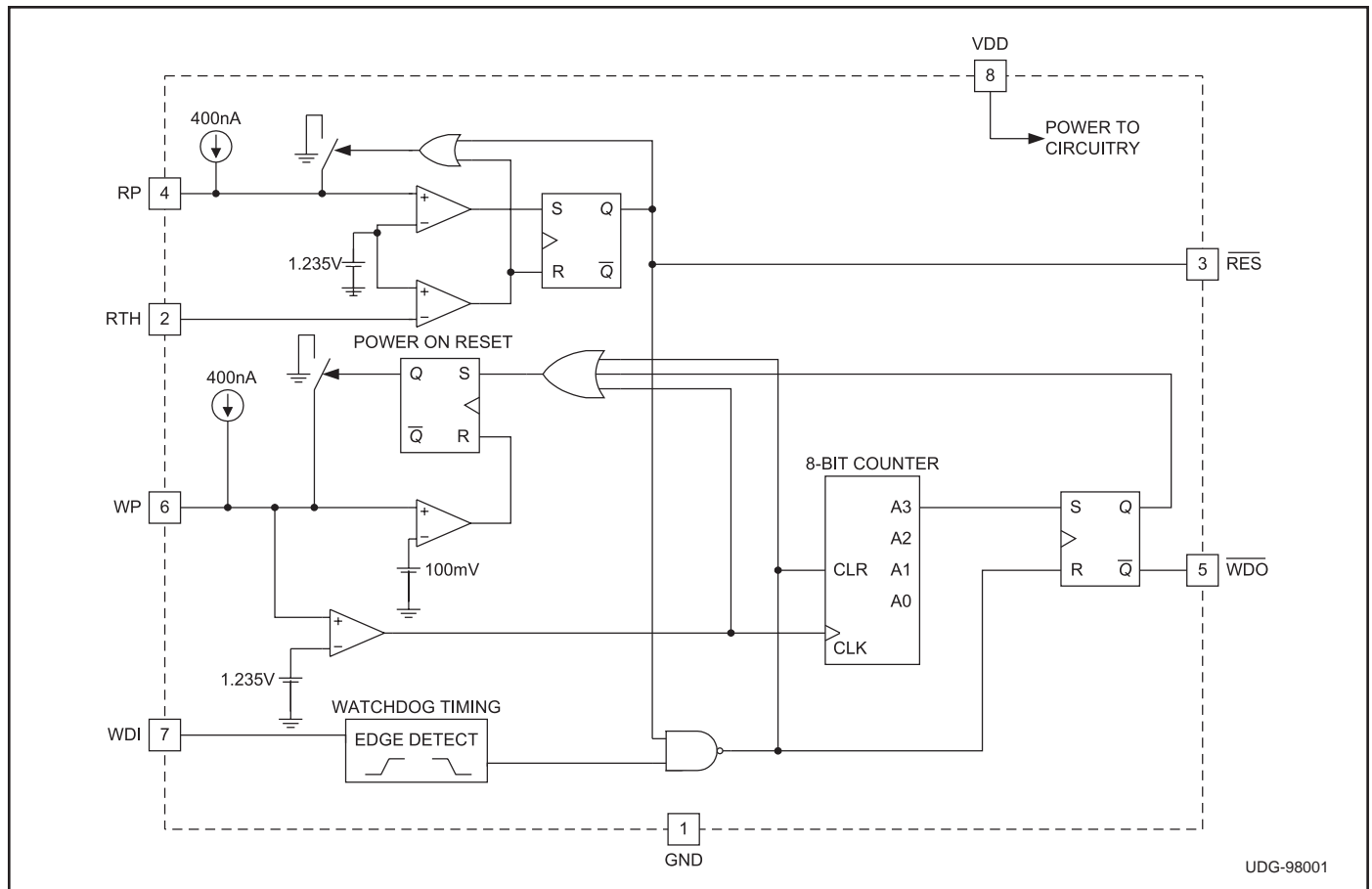
- Fully Programmable Reset Threshold
- Fully Programmable Reset Period
- Fully Programmable Watchdog Period
- 2% Accurate Reset Threshold
- VDD Can Go as Low as 2V
- 15µA Maximum IDD
- Reset Valid Down to 1V

DESCRIPTION

The UCC3946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the IC asserts a reset signal \overline{RES} with VDD as low as 1V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user. The IC is also resistant to glitches on the VDD line. Once \overline{RES} has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, WDO will be asserted. The watchdog function will be disabled during reset conditions.

The UCC3946 is available in 8-pin SOIC(D), 8-pin DIP (N or J) and 8-pin TSSOP(PW) packages to optimize board space.

BLOCK DIAGRAM



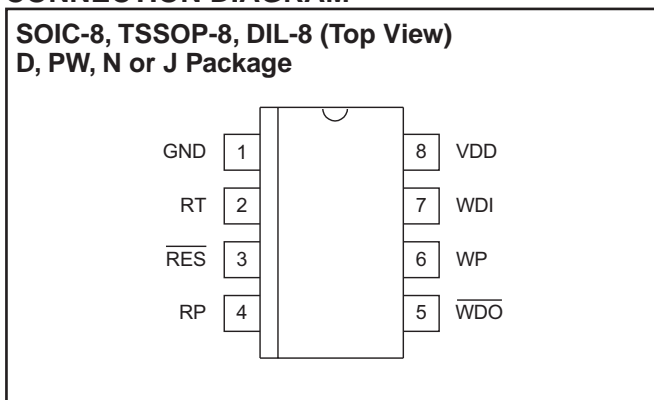
Note: Pinout represents the 8-pin TSSOP package.

ABSOLUTE MAXIMUM RATINGS

V_{IN} 10V
 Storage Temperature -65°C to +150°C
 Junction Temperature -55°C to +150°C
 Lead Temperature (Soldering, 10 sec.) +300°C

Currents are positive into, negative out of the specified terminal.
 Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 2V to 5.5V for UCC1946, UCC2946 and UCC3946; T_A = 0°C to 70°C for UCC3946, -40°C to 85°C for UCC2946, and -55°C to 125°C for UCC1946. T_A = T_J

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
		UCC3946			UCC1946 & UCC2946			
Operating Voltage		2		5.5	2.2		5.5	V
Supply Current			10	15		12	18	μA
Minimum VDD	(Note 1)			1			1	V
Reset Section								
Reset Threshold	VDD Rising	1.21	1.235	1.26	1.15	1.235	1.26	V
Threshold Hysteresis			15			15		mV
Input Leakage				5			5	nA
Output High Voltage	I _{SOURCE} = 2mA	V _{DD} - 0.3			V _{DD} - 0.3			V
Output Low Voltage	I _{SINK} = 2mA			0.1			0.1	V
	V _{DD} = 1V, I _{SINK} = 20μA			0.3			0.6	V
VDD to Output Delay	V _{DD} = -1mV/μs (Note 2)		120			120		μs
Reset Period	C _{RES} = 64nF	160	200	240	140	200	260	ms
Watchdog Section								
WDI Input High		0.7·V _{DD}			0.7·V _{DD}			V
WDI Input Low				0.3·V _{DD}			0.3·V _{DD}	V
Watchdog Period	C _{WD} = 64nF	1.12	1.60	2.08	0.96	1.60	2.24	s
Watchdog Pulse Width		20			20			ns
Output High Voltage	I _{SOURCE} = 2mA	V _{DD} - 0.3			V _{DD} - 0.3			V
Output Low Voltage	I _{SINK} = 2mA			0.1			0.1	V
	V _{DD} = 1V, I _{SINK} = 20mA		0.3			0.6		V

Note 1: This is the minimum supply voltage where RES is considered valid.

Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Ground reference for the IC.

RES: This pin is high only if the voltage on the RTH has risen above 1.235V. Once RTH rises above the threshold, this pin remains low for the reset period. This pin will also go low and remain low if the RTH voltage dips below 1.235V for an amount of time determined by Figure 1.

RTH: This input compares its voltage to an internal 1.25V reference. By using external resistors, a user can program any reset threshold he wishes to achieve.

RP: This pin allows the user to program the reset period

by adjusting an external capacitor.

VDD: Supply voltage for the IC.

WDI: This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, \overline{WDO} is asserted.

WDO: This pin is the watchdog output. This pin will be asserted low if the WDI pin is not strobed or toggled within the watchdog period.

WP: This pin allows the user to program the watchdog period by adjusting an external capacitor.

APPLICATION INFORMATION

The UCC3946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage “glitches” whose voltage amplitude and time duration are less than the values specified in Figure 1 are ignored.

The watchdog circuit monitors the microprocessor’s activity, if the microprocessor does not toggle WDI during the programmable watchdog period \overline{WDO} will go low, alerting the microprocessor’s interrupt of a fault. The \overline{WDO} pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

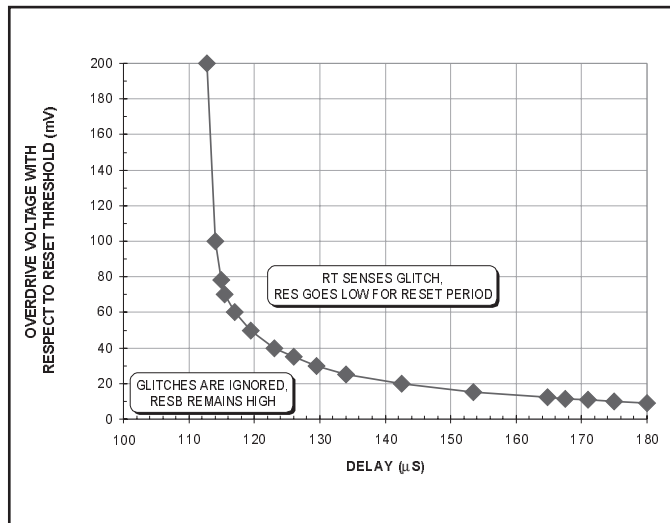


Figure 1.

Overdrive Voltage vs. Delay to Output Low on RESB

Slew rate: $-1V/mS$; Monitored Voltage = V_{DD}

Programming the Reset Voltage and Reset Period

The UCC3946 allows the reset trip voltage to be programmed with two external resistors. In most applications V_{DD} is monitored by the reset circuit, however, the design allows voltages other than V_{DD} to be monitored. Referring to Figure 2, the voltage below which reset will be asserted is determined by:

$$V_{RESET} = 1.235 \cdot \frac{R1 + R2}{R2}$$

In order to keep quiescent currents low, resistor values in the megaohm range can be used for $R1$ and $R2$. A manual reset can be easily implemented by connecting a momentary push switch in parallel with $R2$. \overline{RES} is guaranteed to be low with V_{DD} voltages as low as 1V.

Once V_{DD} rises above the programmed threshold, \overline{RES} remains low for the reset period defined by:

$$TRP = 3.125 \cdot CRP$$

where TRP is time in milliseconds and CRP is capacitance in nanofarads. CRP is charged with a precision current source of 400nA, a high quality, low leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Figure 3 illustrates the voltage levels and timings associated with the reset circuit.

Programming the Watchdog Period

The watchdog period is programmed with CWP as follows:

$$TWP = 25 \cdot CWP$$

where TWP is in milliseconds and CWP is in nanofarads. A high quality, low leakage capacitor should be used for CWP . The watchdog input WDI must be toggled with a high/low or low/high transition within the watchdog period to prevent \overline{WDO} from assuming a logic level low. \overline{WDO} will maintain the low logic level until WDI is toggled or \overline{RES} is asserted. If at any time \overline{RES} is asserted, \overline{WDO}

will assume a high logic state and the watchdog period will be reinitiated. Figure 4 illustrates the timings associated with the watchdog circuit.

Connecting \overline{WDO} to \overline{RES}

In order to provide design flexibility, the reset and watchdog circuits in the UCC3946 have separate outputs. Each output will independently drive high or low, depending on circuit conditions explained previously.

In some applications, it may be desirable for either the \overline{RES} or \overline{WDO} to reset the microprocessor. This can be done by connecting \overline{WDO} to \overline{RES} . If the pins try to drive to different output levels, the low output level will dominate. Additional current will flow from VDD to GND during these states. If the application cannot support additional current (during fault conditions), \overline{RES} and \overline{WDO} can be connected to the inputs of an OR gate whose output is

connected to the microprocessor's reset pin.

Layout Considerations

A 0.1 μ F capacitor connected from VDD to GND is recommended to decouple the UCC3946 from switching transients on the VDD supply rail.

Since RP and WP are precision current sources, capacitors CRP and CWP should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RTH pin.

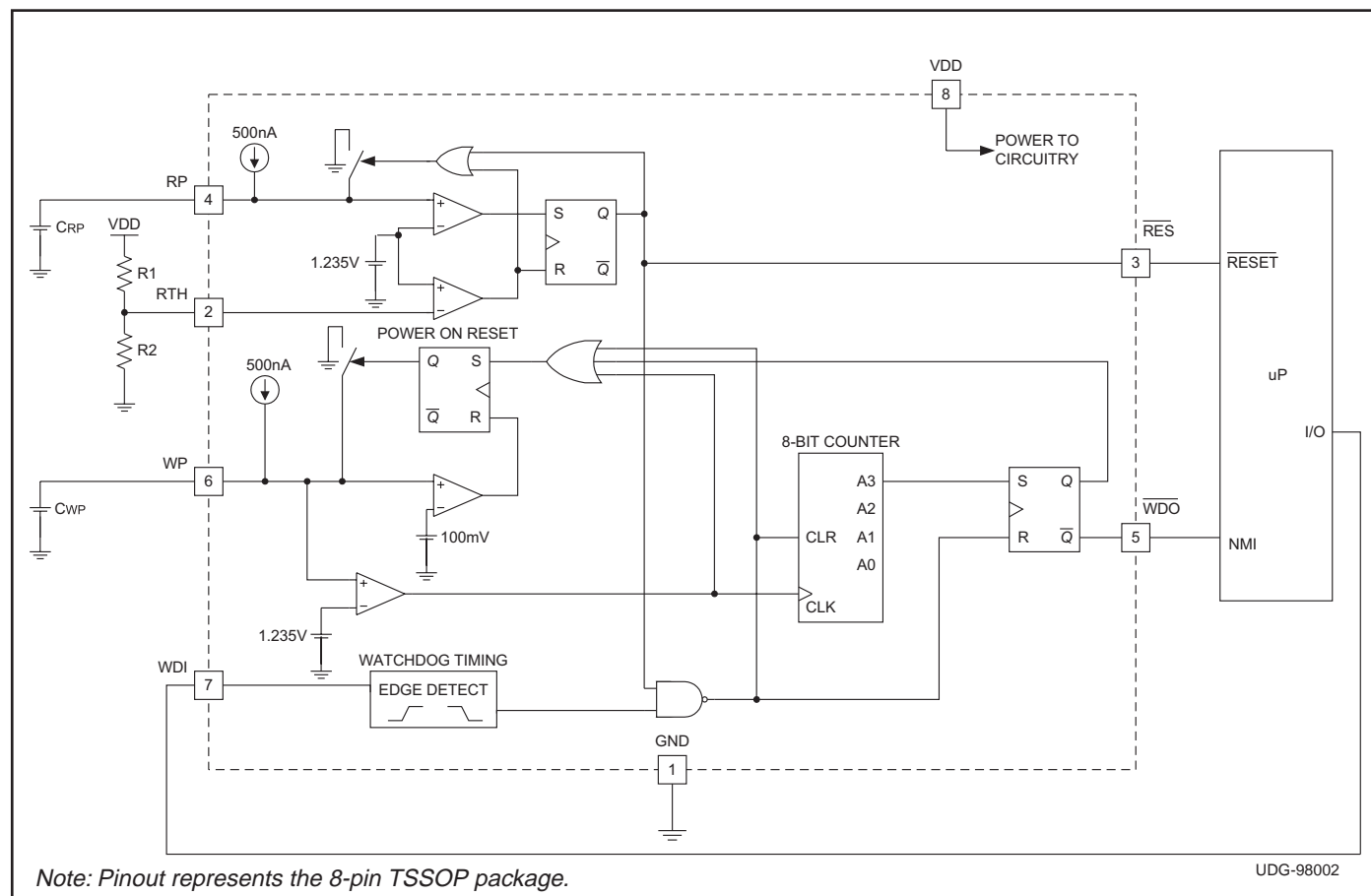


Figure 2. Typical Application Diagram

APPLICATION INFORMATION (cont.)

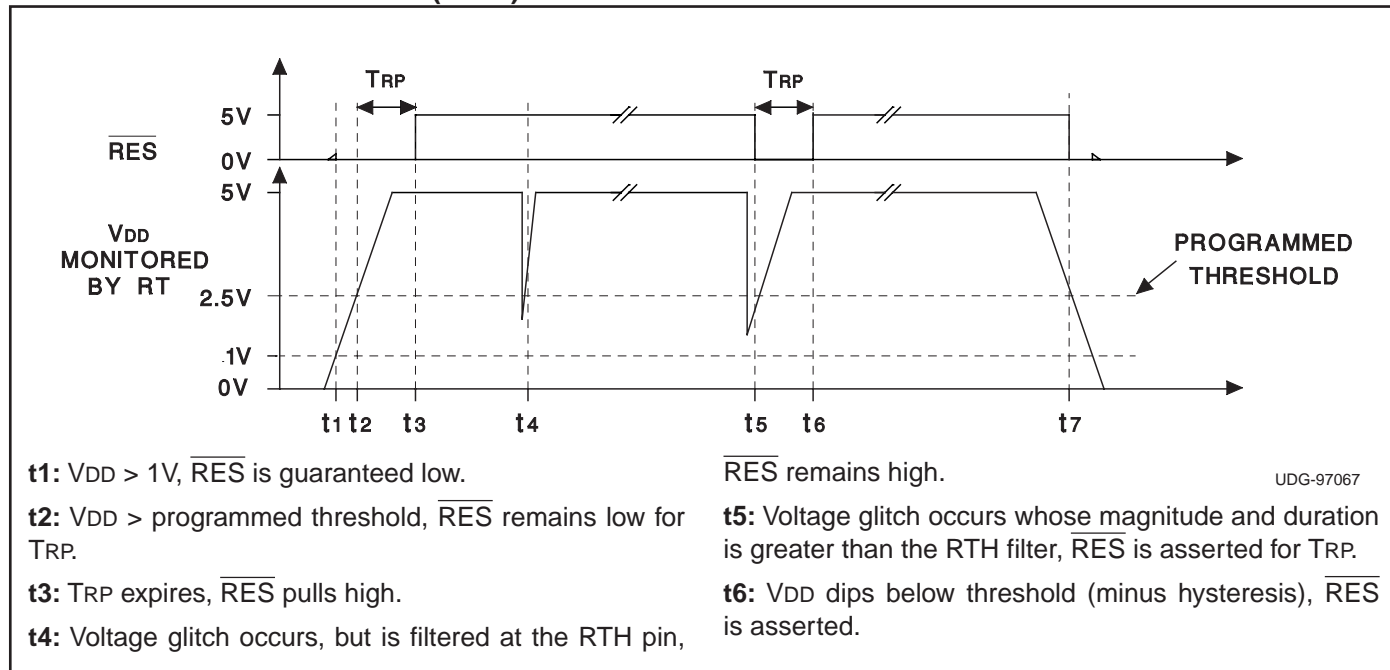


Figure 3. Reset Circuit Timings

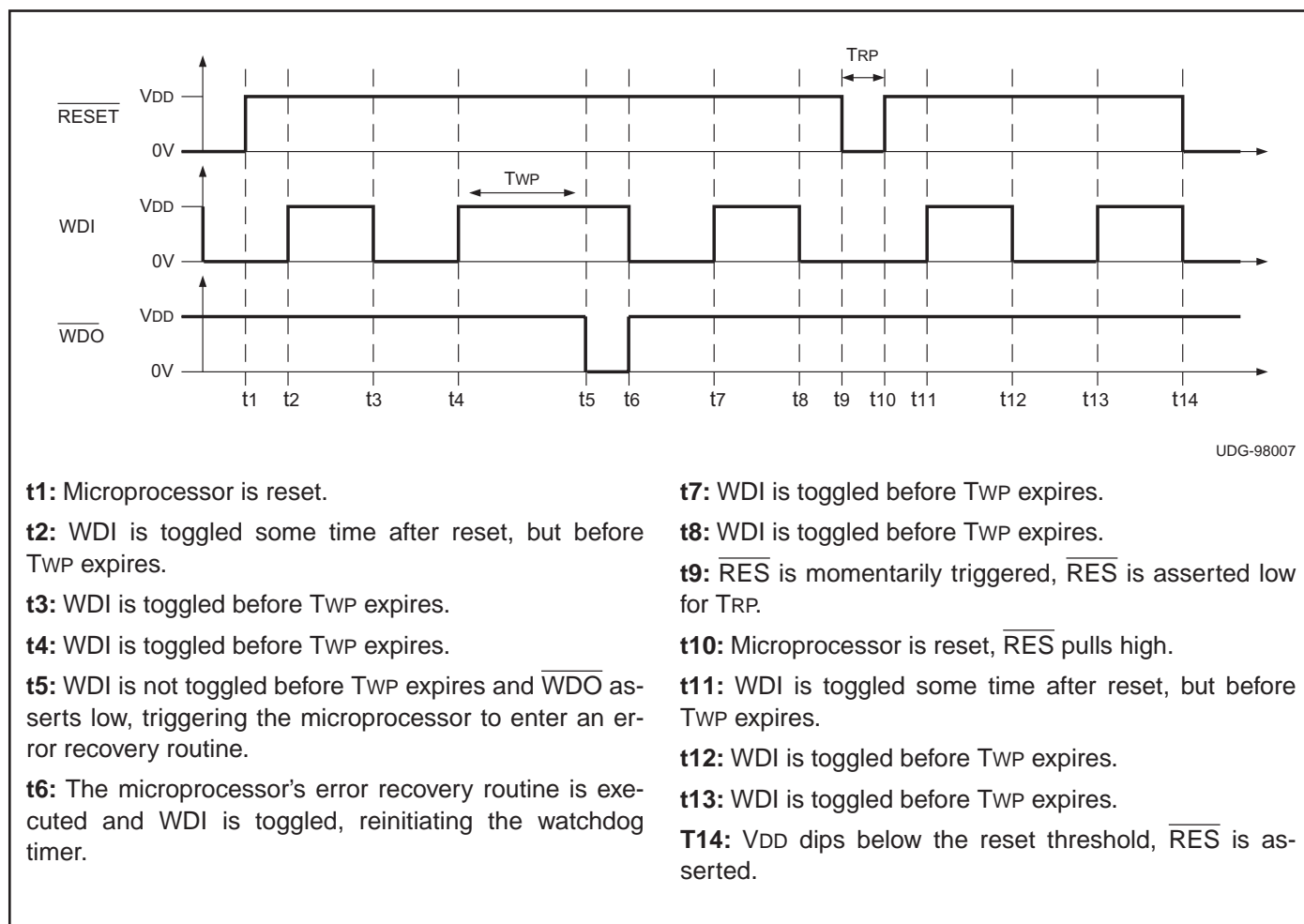


Figure 4. Watchdog Circuit Timings