IrDA 115.2kbps Receiver

FEATURES

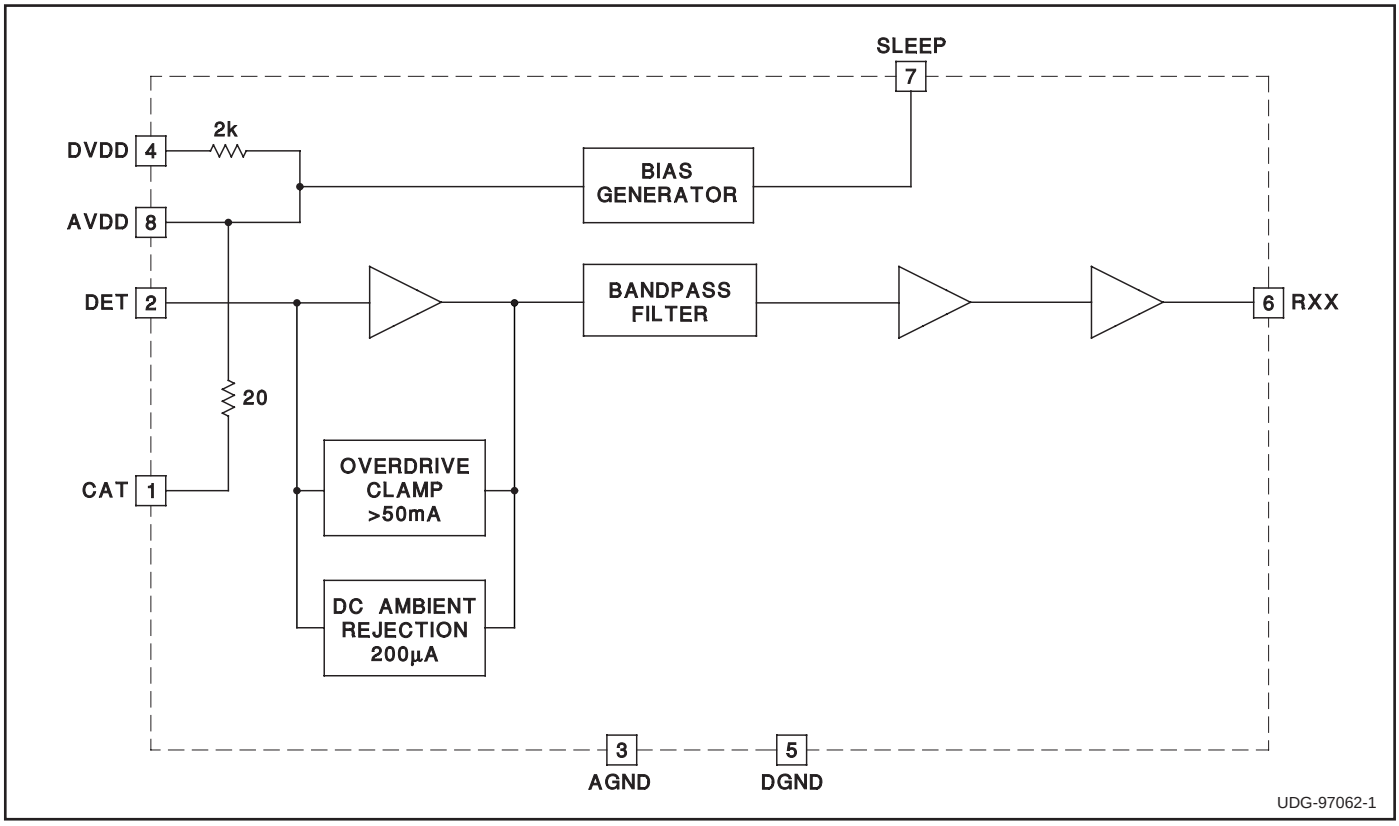
- Supports IrDA standard to 115.2kbps Data Rates
- 3V to 5V Operation
- Wide Dynamic Receiver Range from 200nA to 50mA Typical
- IrDA Compliant I/O
- Very Low Quiescent Current In Active Mode (250µA Typical)
- Ultra Low Quiescent Current In Sleep Mode (0.5µA Typical)
- Compatible with IrDA Detector Diodes

DESCRIPTION

The UCC5341 IrDA (Infrared Data Association) Receiver supports the analog section of the IrDA standard. It has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses to a UART. The amplifier is capable of input currents ranging from 200nA to greater than 50mA. The UCC5341 is bandpass limited to reduce interference from other IR sources. The UCC5341 also has very low current consumption in the active mode (250µA typically), making it excellent for power sensitive applications.

The output of the receiver is designed to drive CMOS and TTL levels, for direct interfacing to IrDA compliant UARTs and Super I/O devices. Internal resistors are provided for decoupling the detector diode supply, thus minimizing the number of external components required.

BLOCK DIAGRAM



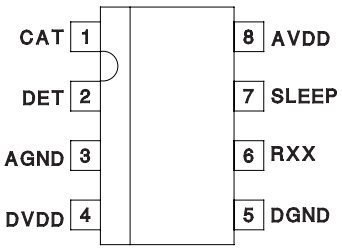
ABSOLUTE MAXIMUM RATINGS

AVDD, CAT, DVDD . . . . . –0.3V to 7V
CAT, DET, DVDD, SLEEP, ... –0.3V to AVDD + 0.3V
I_{RXX} . . . . . –10mA to 10 mA
I_{DET} 250mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are with respect to respect to AGND. DGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

ABSOLUTE MAXIMUM RATINGS

SOIC-8, DIL-8 (Top View)
D, N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3.0V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40pF, C_{DET} < 56pF. All currents are positive into a specified pin. $T_A = T_J$

PARAMETER	TEST CONDITION	MI N	TYP	MAX	UNITS
Supply Current Section					
I_{DD}	No Output Load, SLEEP ≤ 0.5V		250	350	µA
I_{DD}	SLEEP ≥ AVDD – 0.5V		0.5	3	µA
R_{DVDD}	AVDD to DVDD	1.0	2	3.0	kΩ
R_{CAT}	AVDD to CAT	10	20	32	Ω
Receiver Section					
Input Refered Noise	(Note 1)		10		$\frac{pA}{\sqrt{Hz}}$
Detection Threshold	1.6µs Input Pulse, 1µs ≤ R_{XX} ≤ 8µs		200	400	nA
Signal to Noise Ratio	I_{DET} = 200nA, (Note 1)		11.8		nA
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	I_{DET} = 400nApk to 20mApk, 0 to 200µADC, 1.6µs Input Pulse	1.0		8.0	µs
RXX Output (V_{OL})	I_{RXX} = 800µA		200	400	mV
RXX Output (V_{OH})	I_{RXX} = –100µA, DV_{DD} – R_{XX}		200	400	mV
RXX Rise Time	From 10% to 90% of DVDD		150	200	ns
RXX Fall Time	From 90% to 10% of DVDD		100	150	ns

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for analog circuits. Connect to circuit board ground plane.

AVDD: Supply pin for analog circuits. Bypass to AGND with a 100nF or 1µF ceramic capacitor.

CAT: Filtered Supply for PIN diode cathode. Internally connected to AVDD through a 20Ω resistor. Bypass to AGND with a 4.7µF capacitor plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with AVDD and/or AGND from all other signals, especially RXX.

DGND: Ground pin for digital circuits. Connect to circuit board ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD through a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

RXX: Output of the detect amplifier and buffer. Connect to UART. Avoid coupling the RXX signed to DET.

SLEEP: Sleep mode select pin. A logic high on SLEEP puts the chip into sleep mode, reducing IDD to 0.5µA typical.

APPLICATION INFORMATION

Ground Plane

There are 2 ground connections shown on the application drawing, representing the sensitive analog ground and the 'dirty' digital ground. These 2 points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provision to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

DET Considerations

DET is flanked by AGND and CAT. This should be used to good advantage by fully enclosing the DET circuit board trace with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 100nF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

Analog Power Supply Decoupling

The UCC3541 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass capacitor handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2k resistor will allow, an external resistor can shunt it. This should always be accompanied by increasing the value of the decoupling capacitor on DVDD and AVDD.

Economy Application

The diagram of the economy application shows only one bypass capacitor. This application is suitable where maxi-

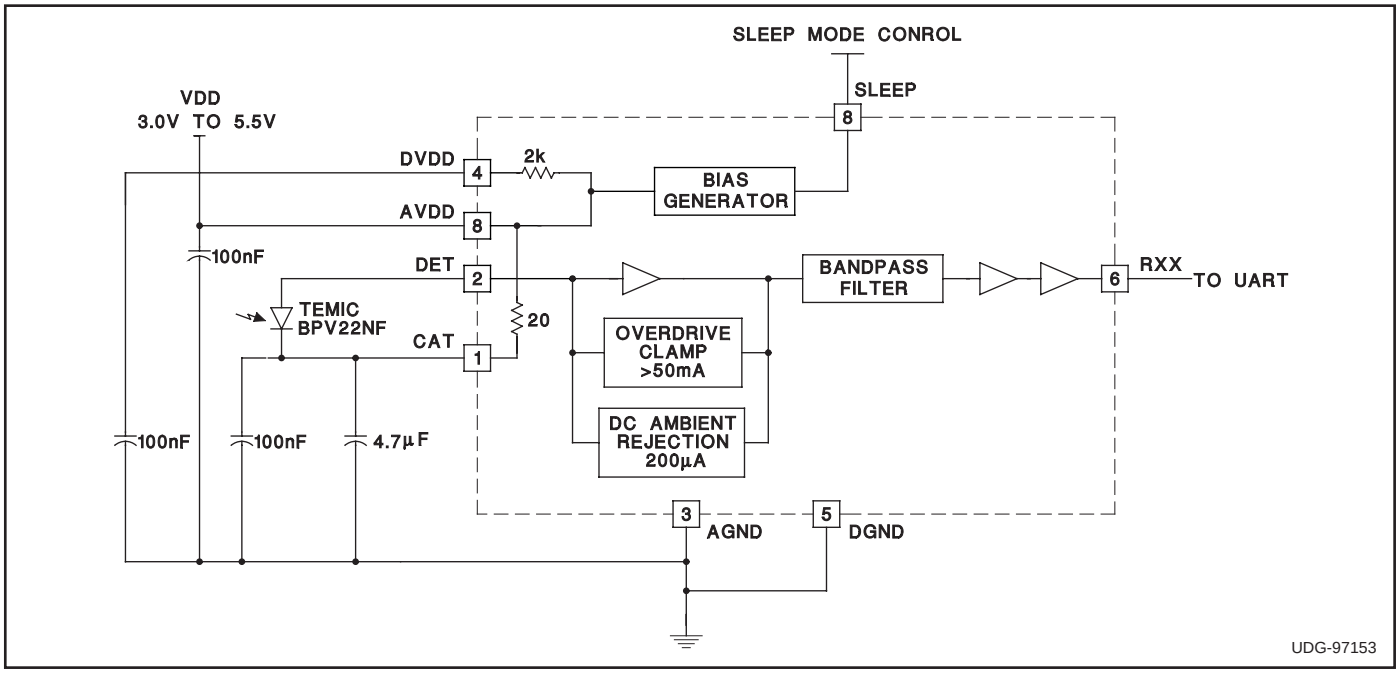


Figure 1. Typical Application of the UCC5341

APPLICATION INFORMATION (cont.)

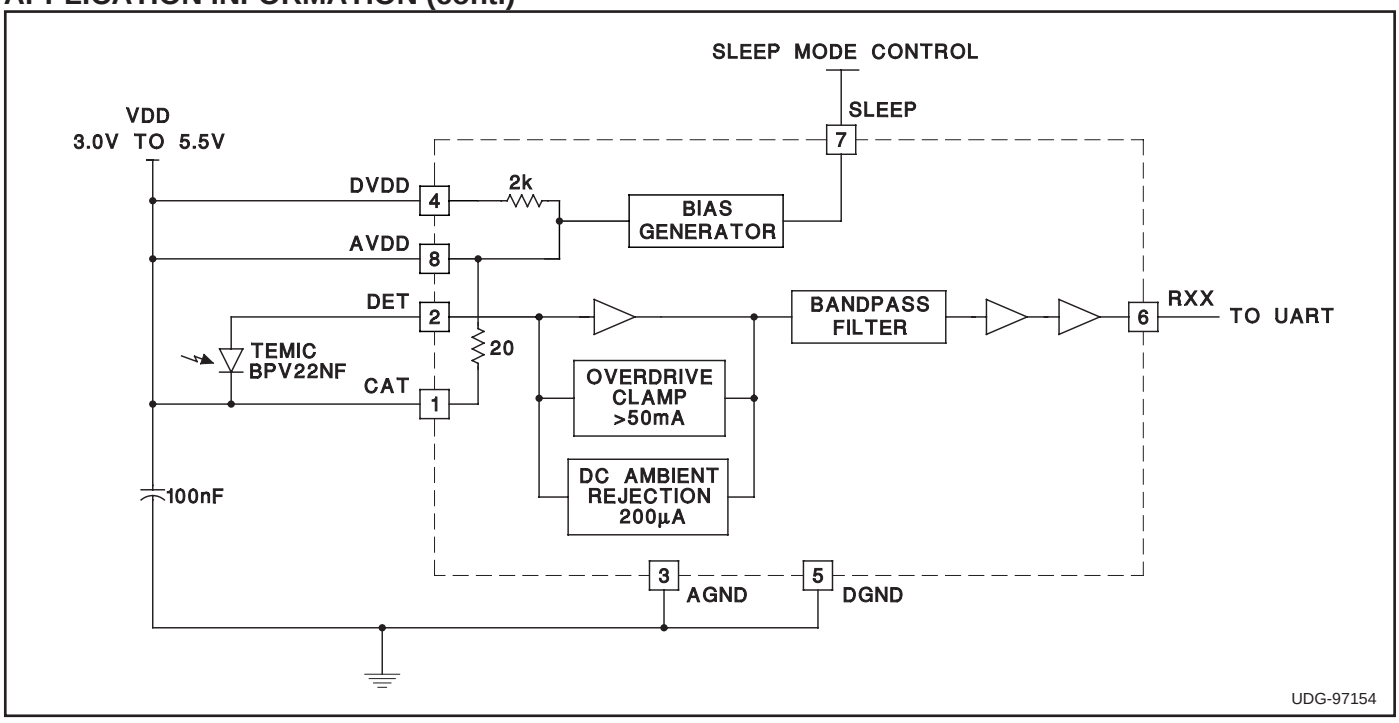


Figure 2. Economy Application of the UCC5341

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