

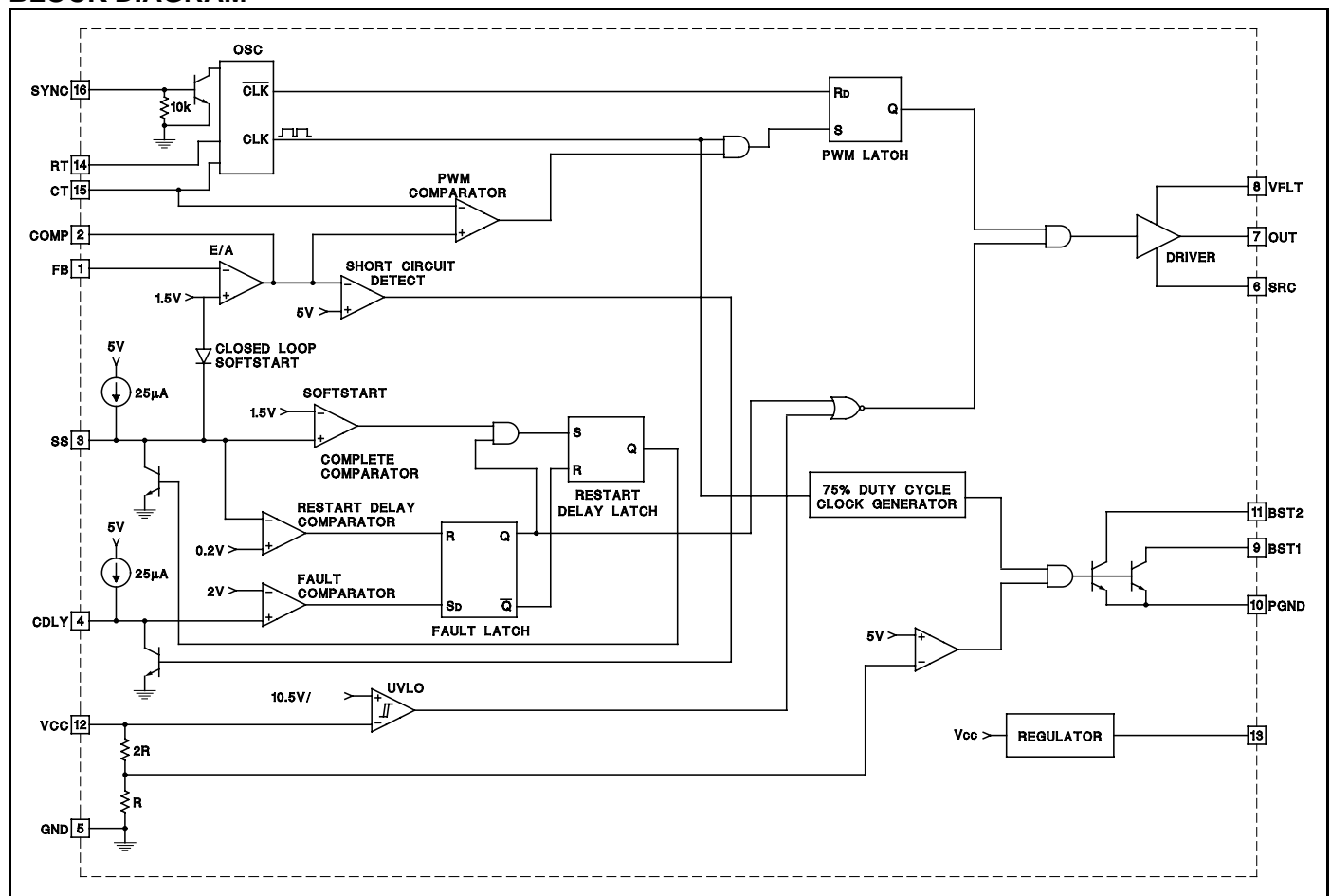
# Secondary Side Synchronous Post Regulator

## FEATURES

- Practical Operation at Switching Frequencies up to 1MHz
- Wide Band Error Amplifier
- Undervoltage Lockout with Hysteresis
- Output Active Low During UVLO
- Soft Start/Maximum Duty Cycle Control
- Trimmed Bandgap Reference
- Internally Regulated 15V Boost Supply
- Short Circuit Protection with Programmable Delay

## DESCRIPTION

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

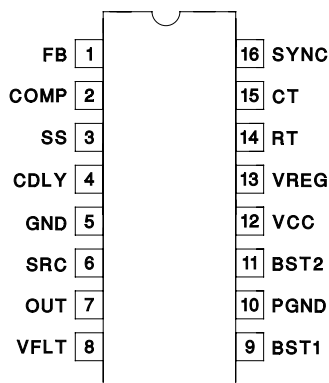
Supply Voltage	20V
VFLT Voltage	50V, 30V at 2A
Supply Current	50mA
Analog Inputs	–0.3 to 20V
SYNC Maximum Sink Current	600μA
PWM Driver, IOUT	±300mA
PWM Driver, IOUT (Peak)	±1.5A
Maximum Operating Frequency	1MHz

Power Dissipation at TA = 60°C	1W
Storage Temperature	–65°C to 150°C
Junction Temperature	–55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

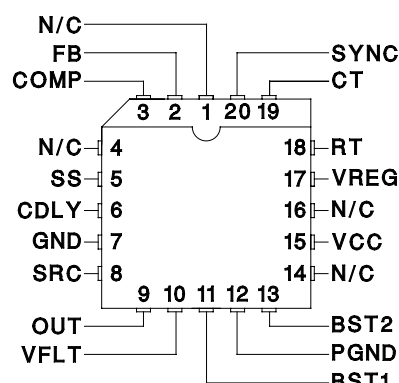
*Currents are positive into, negative out of specified terminal.  
Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

## CONNECTION DIAGRAM

**DIL-16, SOIC-16 (Top View)**  
**J, N or DW Packages**



**PLCC-20 (Top View)**  
**Q Package**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified, TA = 0°C to 70°C for the UC3584, –40°C to 85°C for the UC2584, and –55°C to 125°C for the UC1584, VCC = 15V. TA = TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
<b>Error Amplifier</b>					
FB	COMP = FB	1.468	1.5	1.532	V
IFB	VCOMP = VFB	150	300	450	nA
COMP VOL	FB = 1.6V, ICOMP = 200μA		50	400	mV
COMP VOH	FB = 1.4V, ICOMP = –200μA	5.1	5.5	7	V
AVOL		60	80		dB
PSRR (COMP)	COMP = FB, VCC = 14V to 16V	60			dB
GBW Product	F = 100kHz	5	10		MHz
<b>Oscillator</b>					
Frequency	RT = 3.75k, CT = 400pF, No Synchronization		500		kHz
Ramp Low	RT = 3.75k, CT = 400pF, No Synchronization		1.75		V
Ramp High	RT = 3.75k, CT = 400pF, No Synchronization		3.5		V
Ramp Amplitude	RT = 3.75k, CT = 400pF, No Synchronization		1.75		V
<b>PWM</b>					
Maximum Duty Cycle	COMP = 4.5V	90			%
Minimum Duty Cycle	COMP = 0V			0	%
<b>PWM DRIVER</b>					
VSAT High	VFLT – VOUT, IOUT = –100mA		2.5	3	V
VSAT Low	VOUT – VSRC, IOUT = 50mA		0.8	2.2	V
TRISE	Load = 1nF, SRC = 0V, Measure VOUT 1V to 9V		75	100	ns
TFALL	Load = 1nF, SRC = 0V, Measure VOUT 9V to 1V		25	100	ns
<b>Soft Start</b>					
Charge Current			30		μA
Discharge Current			1		mA
SS Delay	Css = 500nF		50		ms

**ELECTRICAL CHARACTERISTICS (cont.):** Unless otherwise specified,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  for the UC3584,  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  for the UC2584, and  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for the UC1584,  $V_{CC} = 15\text{V}$ .  $T_A = T_J$ .

PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
<b>Fault Latch</b>					
Charge Current			30		$\mu\text{A}$
Discharge Current			5		mA
Fault Latch Delay	CDLY = 500nF		50		ms
<b>UVLO</b>					
VCC On			10.5		V
Hysteresis			1.7		V
<b>Regulated Voltage</b>					
VREG	I <sub>REG</sub> = 0mA to 1mA	4.8		5.2	V
<b>VCC Regulator</b>					
VCC	Boost inductor connected to 5V	14	15	16	V
I <sub>CC</sub>	No Load, Boost Circuitry Inactive		12	40	mA
	No Load, Boost Circuitry Active (Note 1)		55		mA

Note 1: Guaranteed by design. Not 100% tested in production.

## PIN DESCRIPTIONS

**BST1:** Collector of the boost switch. This is the connection point of the external boost inductor and boost diode. The boost converter generates the bias supply for the UC3584 from the regulated 5V output.

**BST2:** See BST1. BST2 must be connected externally to BST1 pin.

**CDLY:** Delay Set. External CDLY capacitor sets the delay from the time Short Circuit condition is detected and Fault Condition is asserted.

**COMP:** Output of the Voltage Error Amplifier.

**CT:** Connect the Timing Capacitor between CT and GND.

**FB:** Inverting Input of the Voltage Error Amplifier.

**GND:** Analog System Ground.

**OUT:** Output of the floating driver for an external, N-channel MOSFET.

**PGND:** Power Ground. This is the reference node for the boost bias supply regulator. PGND and GND must be connected externally.

**RT:** A Timing Resistor connected between RT and GND sets the discharge current of the timing capacitor.

**SRC:** Source connection of the floating driver to the external switch.

**SS:** Soft Start. An external capacitor is connected between SS and GND to set the duration of the Soft Start cycle.

**SYNC:** Synchronization Pin. The UC3584 is synchronized from the falling edge of the transformer's secondary winding. Voltage must exceed 1V at minimum input line.

**VCC:** Bias supply of the chip, approximately 15V. This is also the output of the boost regulator. The VCC pin must be decoupled to PGND.

**VFLT:** Positive rail of the floating driver's bias supply. Decouple to SRC using a high frequency (ceramic) capacitor.

**VREG:** Output of the internal 5V regulated supply. Must be decoupled to GND.

## APPLICATION INFORMATION

### Biasing the UC3584

Bias supply for the UC3584 is generated from the main output of the power supply by a boost regulator. The inductor, diode and capacitor of the boost converter are external components, while the boost switch is internal to the chip. The boost converter operates in a burst mode with a built-in hysteresis of approximately 1V centered at 15V. This is a bang-bang controller and when enabled has a fixed duty cycle of 75%.

### Undervoltage Detection

The UVLO circuit of the UC3584 monitors the voltage on VCC. During power up and power down, the pulse width modulator and the output driver are disabled and OUT is held active low. Operation is enabled when VCC reaches 10.5V. The UVLO circuitry has a built-in hysteresis of 1.7V (10.5V to 8.8V) thus VCC must drop below 8.8V in order to assert UVLO again.

## APPLICATION INFORMATION (cont.)

### Precision Reference

An internal precision bandgap reference provides accurate voltages to the error amplifier and other control sections of the IC. A buffered 5V regulated voltage is also available for external circuitry on the VREG pin. This pin must be decoupled to the signal GND connection by a good quality high frequency capacitor.

### Oscillator and Trailing Edge Synchronization

The UC3584 is outfitted with a synchronizable oscillator which also generates a ramp signal across the CT capacitor for the PWM comparator. For easy implementation of the leading edge pulse width modulation technique, the oscillator has an inverted ramp waveform as shown in Figure 1. The free running oscillator frequency is determined by the timing components, RT and CT, according to the following equations:

$$R_T = \frac{1.5 \cdot D_{MAX}}{0.0065 \cdot (1 - D_{MAX})}$$

$$C_T = \frac{0.6 \cdot D_{MAX}}{R_T \cdot f_{OSC}}$$

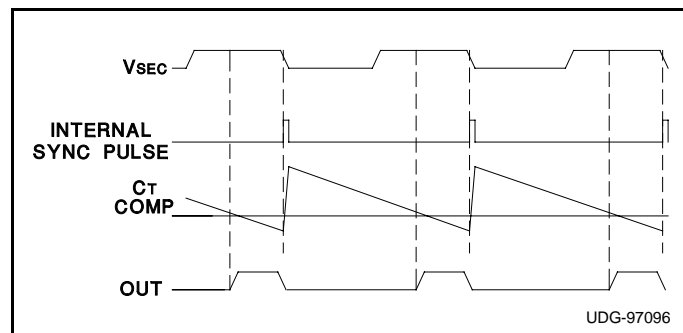
where

RT is the timing resistor, its value should be between 1kΩ and 100kΩ,

CT is the timing capacitor,

DMAX is the desired maximum duty cycle, and

fOSC is the free running oscillator frequency.



**Figure 1. Trailing Edge Synchronization, Leading**

During normal operation the oscillator must be synchronized to the falling edge of the transformer secondary waveform. Synchronization is achieved by connecting SYNC to the secondary winding via a resistor divider. The resistor divider must be chosen to provide a SYNC pin voltage in excess of 1V at the lowest operating voltage on the transformer secondary winding. The UC3584 will generate a narrow internal synchronization pulse which will synchronize the oscillator to the switching frequency of the main converter.

### PWM and Output Driver

The UC3584 employs leading edge modulation technique to set the required on time of its output. Leading edge modulation is preferred for secondary side regulation in multiple output converters to prevent ambiguity in the primary current waveform. In fact, this is the only feasible technique to preserve compatibility with primary side peak current mode control.

As Figure 1 depicts the UC3584 utilizes voltage mode control to regulate output voltage. The output pulse width (the on-time of the MOSFET switch) is determined on a cycle-by-cycle basis by comparing the output of the voltage error amplifier and the ramp waveforms across the timing capacitor. OUT is asserted when the voltage on COMP exceeds the voltage on CT. There are three more conditions which must be satisfied to obtain an active high on the OUT pin. These conditions are:

1. VCC within normal range (UVLO is inactive),
2. No fault condition is detected,
3. CT is discharging.

During the fast charging time of the CT capacitor is held low.

Ultimately, the output of the PWM circuitry controls the conduction interval of an external N-channel MOSFET switch in the power supply. The UC3584 employs an on-board, floating gate driver circuit to interface to the external switch. An external capacitor connected between VFLT and SRC acts as a floating power supply for the driver during the on-time of the switch. Charge is being replenished to the bootstrap capacitor during the off-time of the switch through the bootstrap diode connected between VCC and VFLT as shown in the typical application diagram.

### Soft Start

The UC3584 Soft Start circuitry is designed to implement closed loop startup of the power supply output. During Soft Start, the reference to the noninverting input of the error amplifier is controlled by the voltage across the soft start capacitor on SS. As this voltage rises, it provides an increasing reference to the error amplifier. Once the soft start capacitor charges above the 1.5V precision reference of the error amplifier, SS gets disconnected from the noninverting input of the error amplifier. This technique allows the error amplifier to stay in its linear mode and to regulate the output voltage of the power supply according to the gradually increasing reference voltage on its noninverting input. Further advantage of the closed loop start up scheme is the absence of output voltage overshoot during power up of the power supply output.

