

# High Speed PWM Controller

## FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V  $\pm$ 1%)

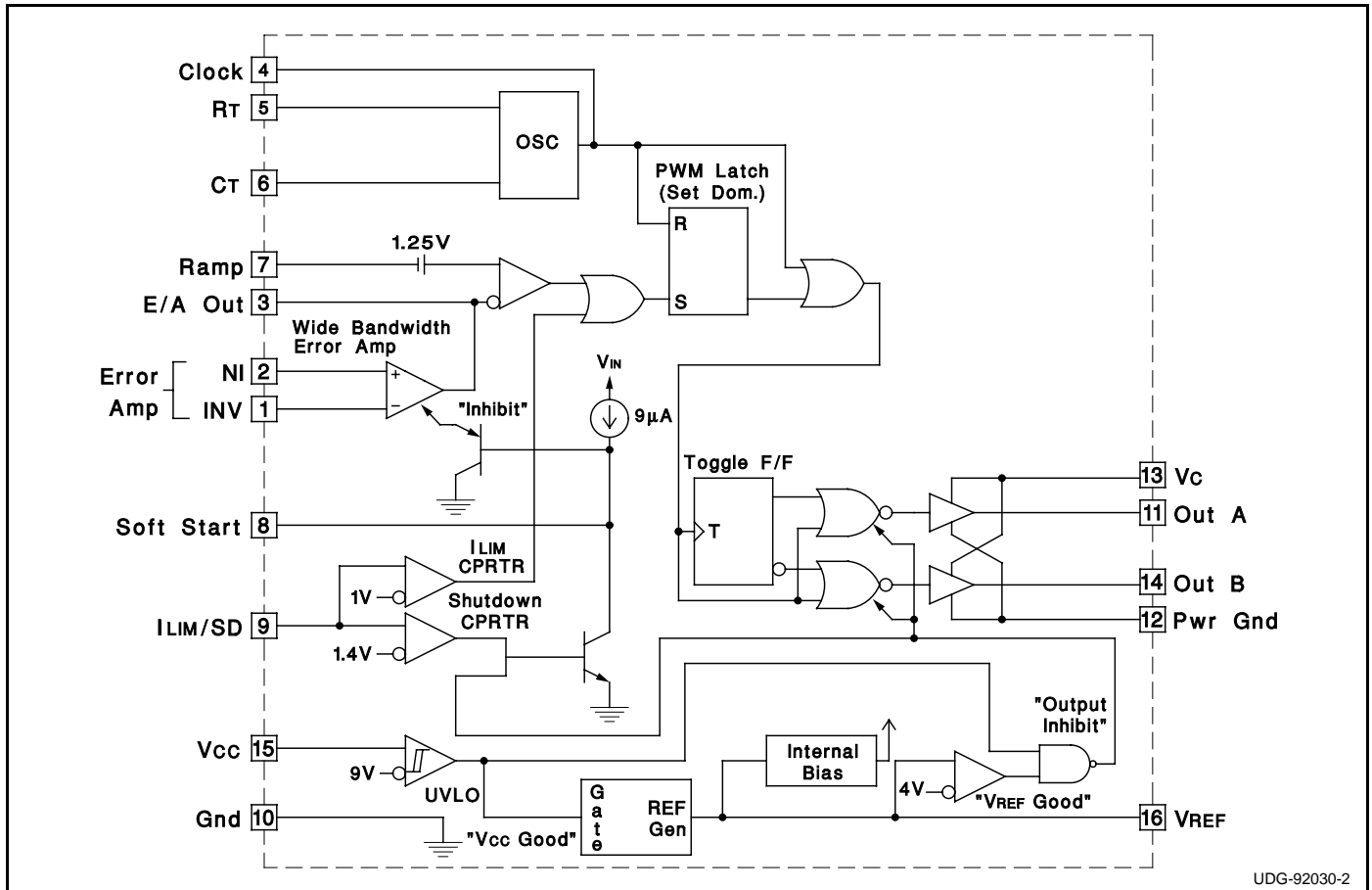
## DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

## BLOCK DIAGRAM



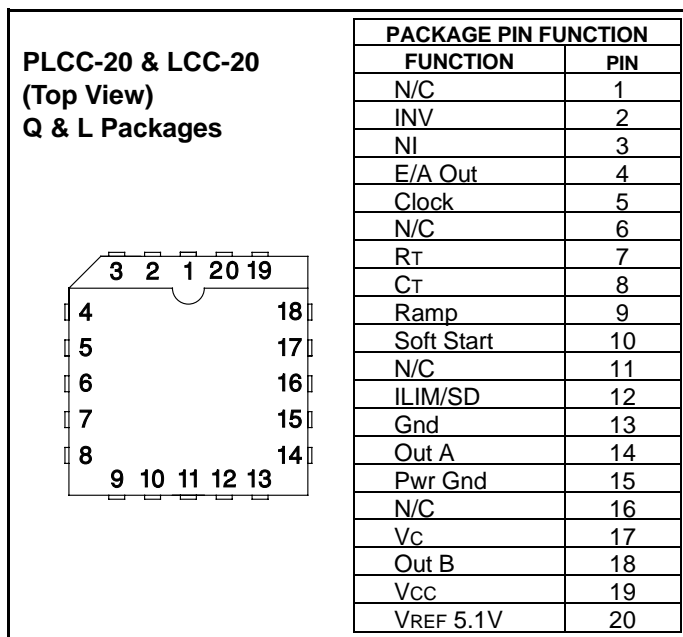
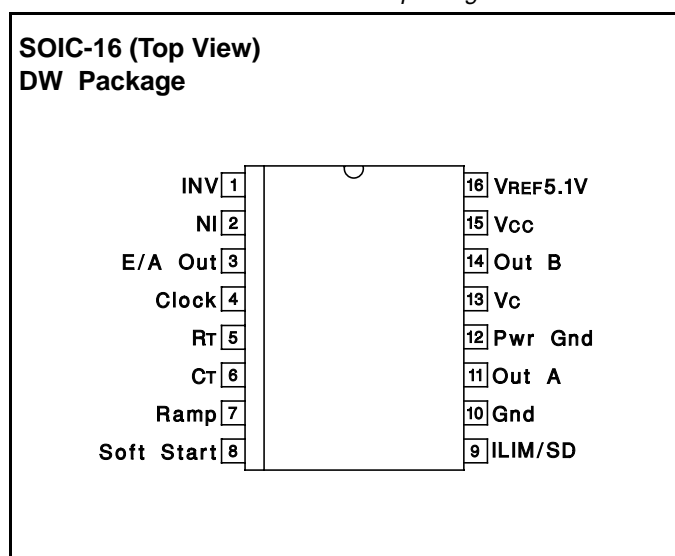
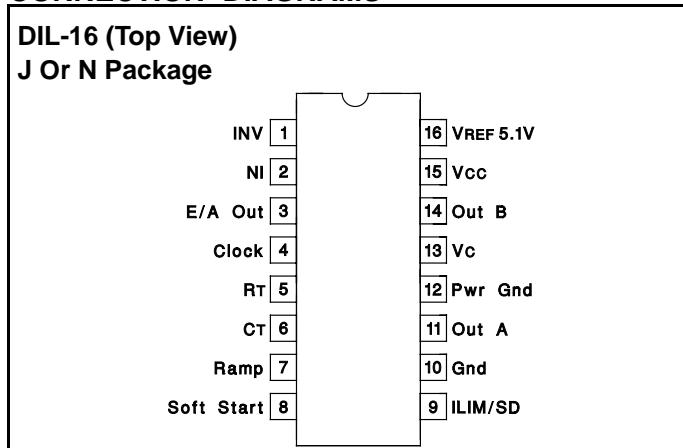
### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15)	30V
Output Current, Source or Sink (Pins 11, 14)	
DC	0.5A
Pulse (0.5 $\mu$ s)	2.0A
Analog Inputs	
(Pins 1, 2, 7)	-0.3V to 7V
(Pin 8, 9)	-0.3V to 6V
Clock Output Current (Pin 4)	-5mA
Error Amplifier Output Current (Pin 3)	5mA
Soft Start Sink Current (Pin 8)	20mA
Oscillator Charging Current (Pin 5)	-5mA
Power Dissipation	1W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

### CONNECTION DIAGRAMS



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for ,  $R_T = 3.65k$ ,  $C_T = 1nF$ ,  $V_{cc} = 15V$ ,  $-55^\circ C < T_A < 125^\circ C$  for the UC1825,  $-40^\circ C < T_A < 85^\circ C$  for the UC2825, and  $0^\circ C < T_A < 70^\circ C$  for the UC3825,  $T_A = T_J$ .

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	$T_J = 25^\circ C$ , $I_o = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$10V < V_{cc} < 30V$		2	20		2	20	mV
Load Regulation	$1mA < I_o < 10mA$		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	$10Hz < f < 10kHz$		50			50		$\mu V$
Long Term Stability*	$T_J = 125^\circ C$ , 1000hrs.		5	25		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	-15	-50	-100	-15	-50	-100	mA
<b>Oscillator Section</b>								
Initial Accuracy*	$T_J = 25^\circ C$	360	400	440	360	400	440	kHz
Voltage Stability*	$10V < V_{cc} < 30V$		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

**ELECTRICAL CHARACTERISTICS  
(cont.)**

Unless otherwise stated, these specifications apply for ,  $R_T = 3.65k$ ,  $C_T = 1nF$ ,  $V_{CC} = 15V$ ,  $-55^{\circ}C < T_A < 125^{\circ}C$  for the UC1825,  $-40^{\circ}C < T_A < 85^{\circ}C$  for the UC2825, and  $0^{\circ}C < T_A < 70^{\circ}C$  for the UC3825,  $T_A = T_J$ .

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Oscillator Section (cont.)</b>								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
<b>Error Amplifier Section</b>								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	$\mu A$
Input Offset Current			0.1	1		0.1	1	$\mu A$
Open Loop Gain	$1V < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5V < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10V < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN 3} = 1V$	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN 3} = 4V$	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN 3} = -0.5mA$	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN 3} = 1mA$	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/ $\mu s$
<b>PWM Comparator Section</b>								
Pin 7 Bias Current	$V_{PIN 7} = 0V$		-1	-5		-1	-5	$\mu A$
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN 7} = 0V$	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
<b>Soft-Start Section</b>								
Charge Current	$V_{PIN 8} = 0.5V$	3	9	20	3	9	20	$\mu A$
Discharge Current	$V_{PIN 8} = 1V$	1			1			mA
<b>Current Limit / Shutdown Section</b>								
Pin 9 Bias Current	$0 < V_{PIN 9} < 4V$			15			10	$\mu A$
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
<b>Output Section</b>								
Output Low Level	$I_{OUT} = 20mA$		0.25	0.40		0.25	0.40	V
	$I_{OUT} = 200mA$		1.2	2.2		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	13.0	13.5		13.0	13.5		V
	$I_{OUT} = -200mA$	12.0	13.0		12.0	13.0		V
Collector Leakage	$V_C = 30V$		100	500		10	500	$\mu A$
Rise/Fall Time*	$CL = 1nF$		30	60		30	60	ns
<b>Under-Voltage Lockout Section</b>								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
<b>Supply Current Section</b>								
Start Up Current	$V_{CC} = 8V$		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN 1}, V_{PIN 7}, V_{PIN 9} = 0V; V_{PIN 2} = 1V$		22	33		22	33	mA

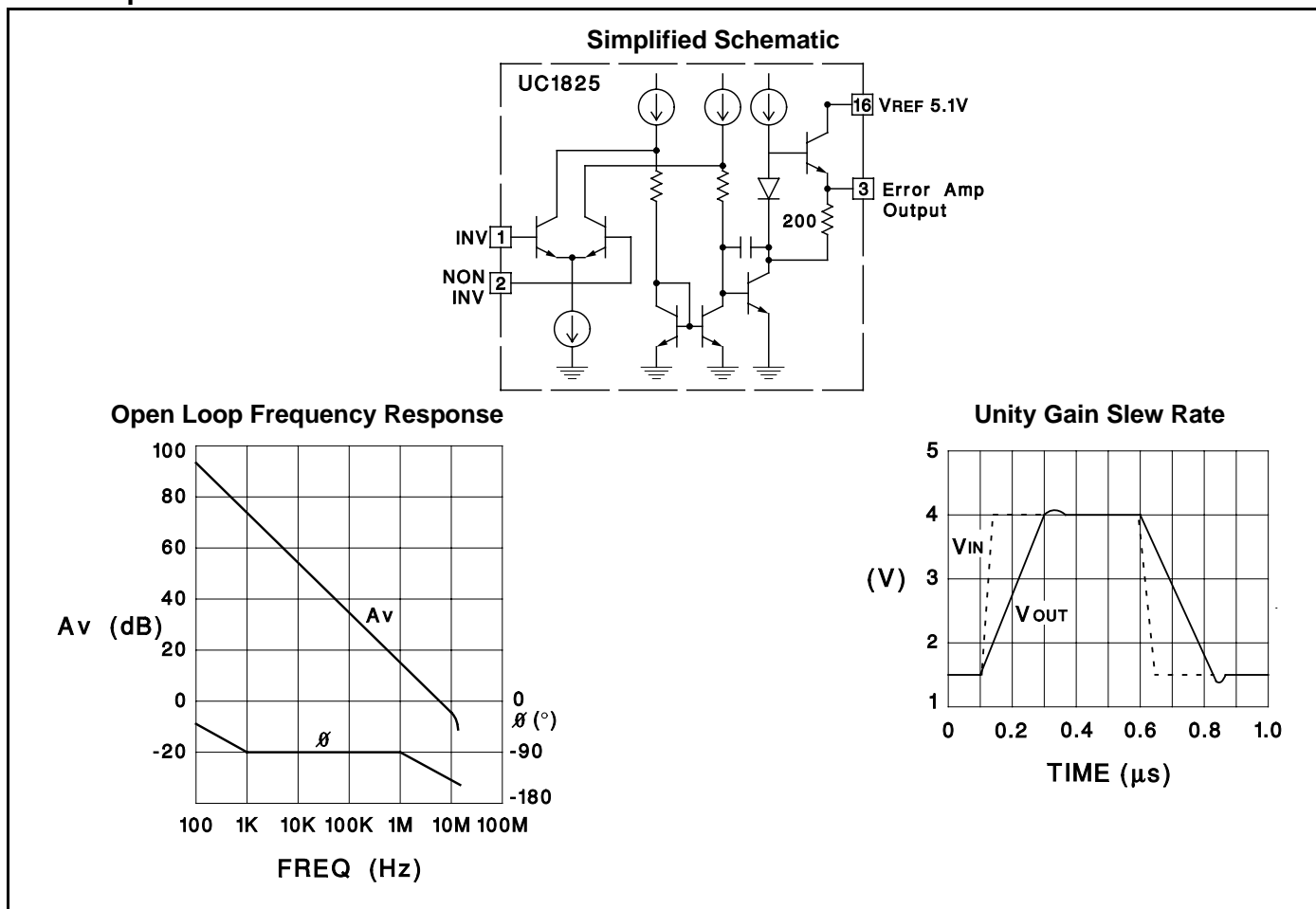
\* This parameter not 100% tested in production but guaranteed by design.

### Printed Circuit Board Layout Considerations

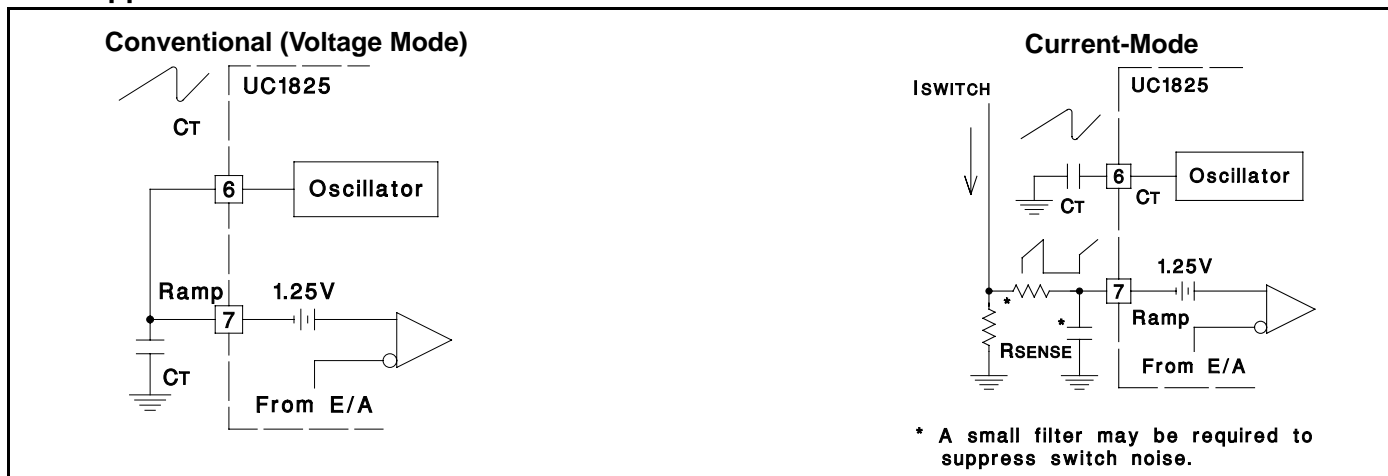
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp

Schottky diode at the output pin will serve this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1 $\mu$ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

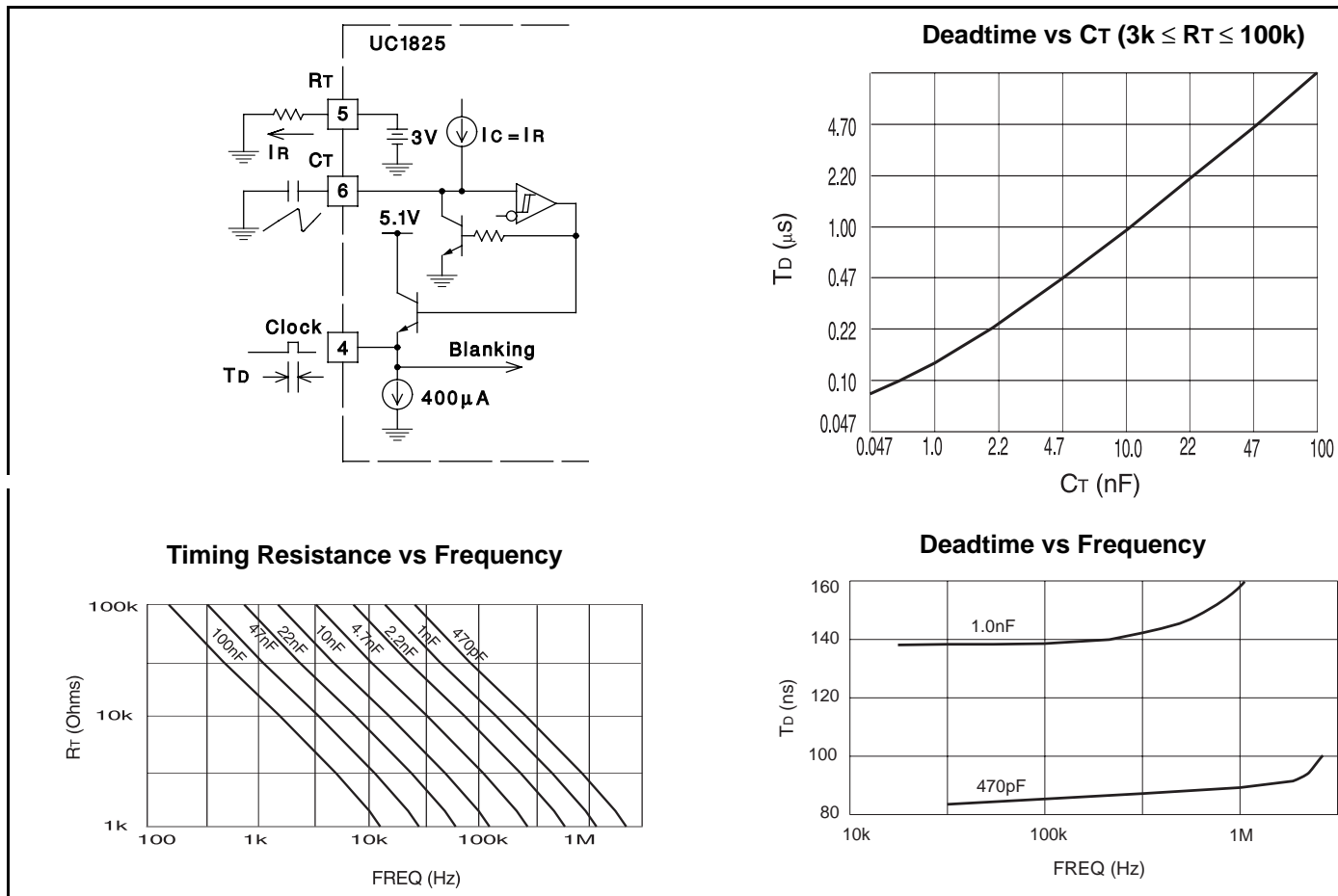
### Error Amplifier Circuit



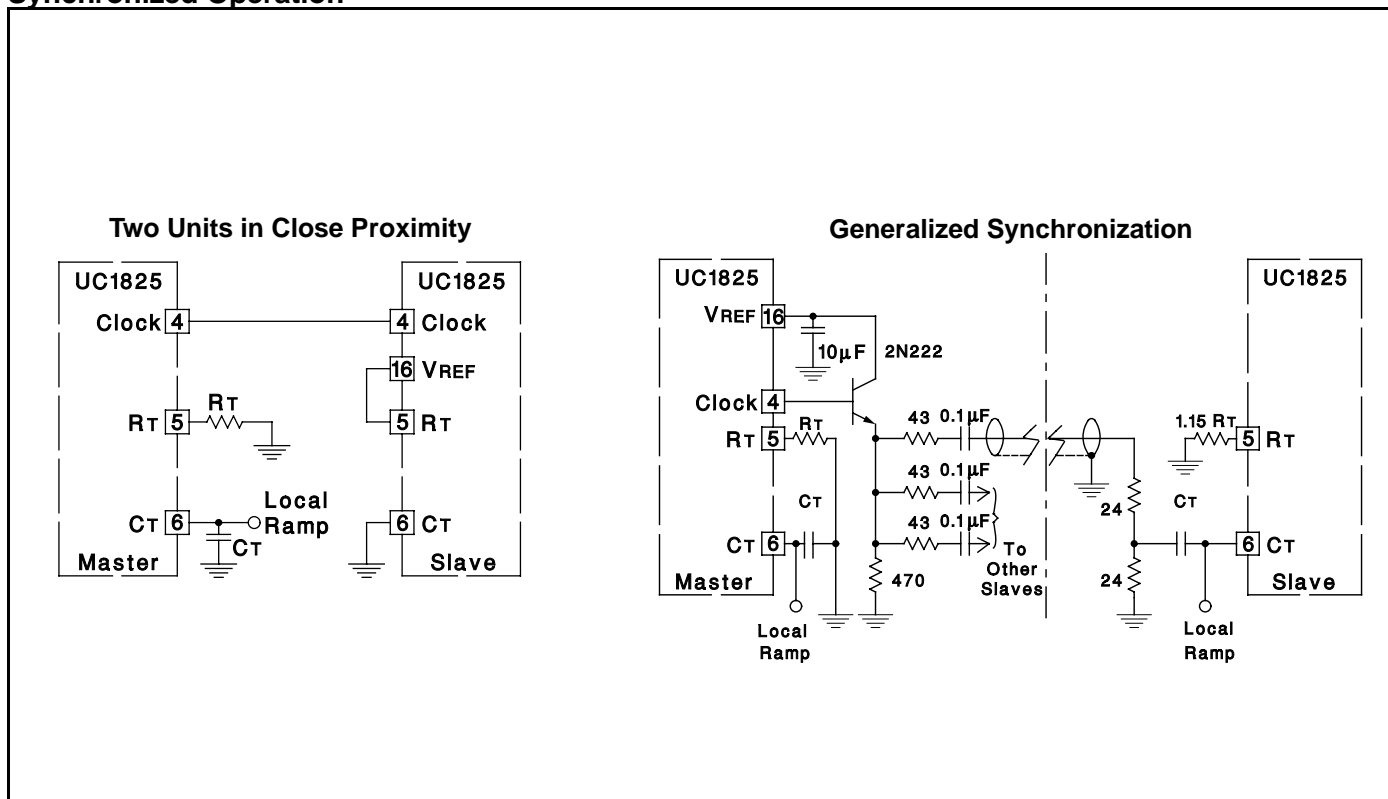
### PWM Applications



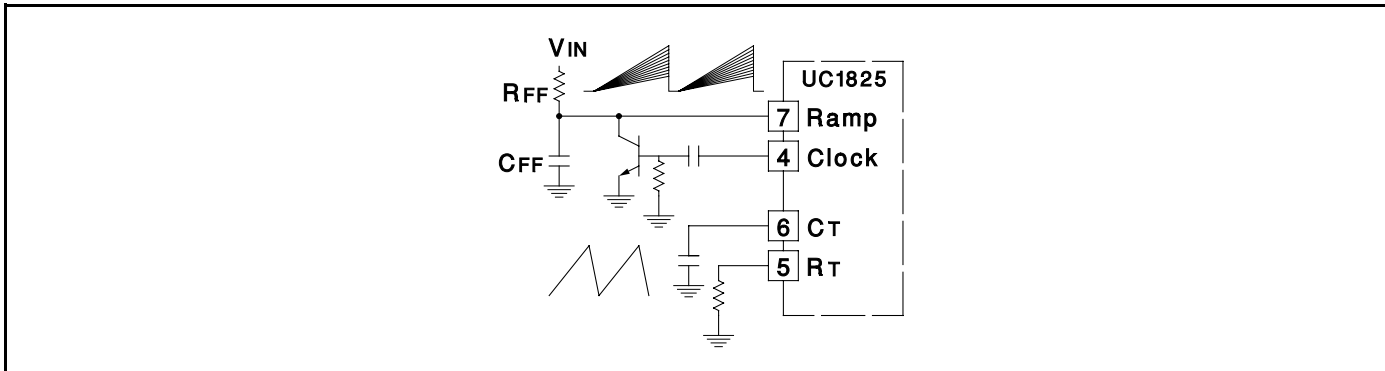
### Oscillator Circuit



### Synchronized Operation

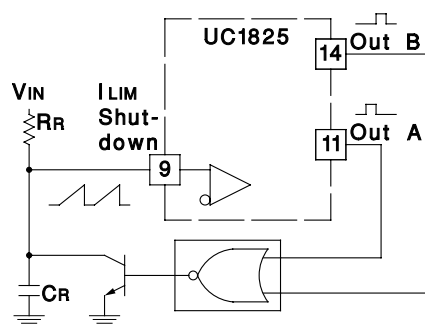


### Forward Technique for Off-Line Voltage Mode Application



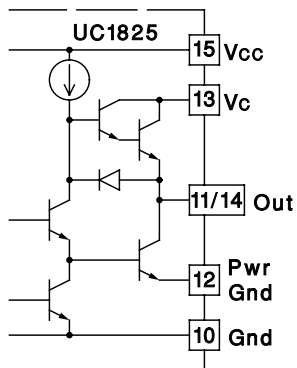
### Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

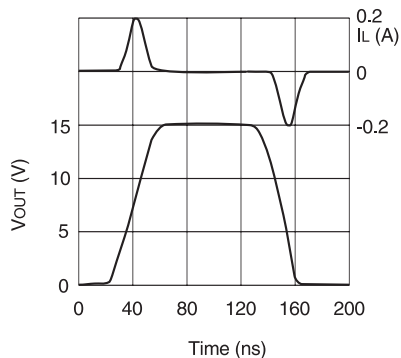


### Output Section

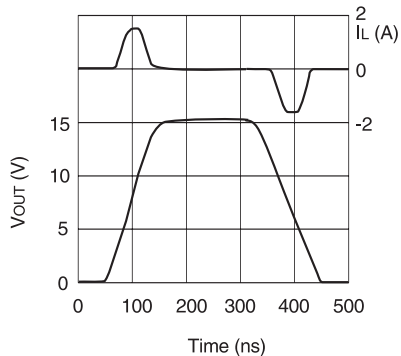
#### Simplified Schematic



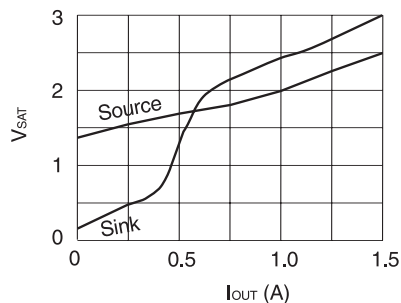
#### Rise/Fall Time (CL=1nF)



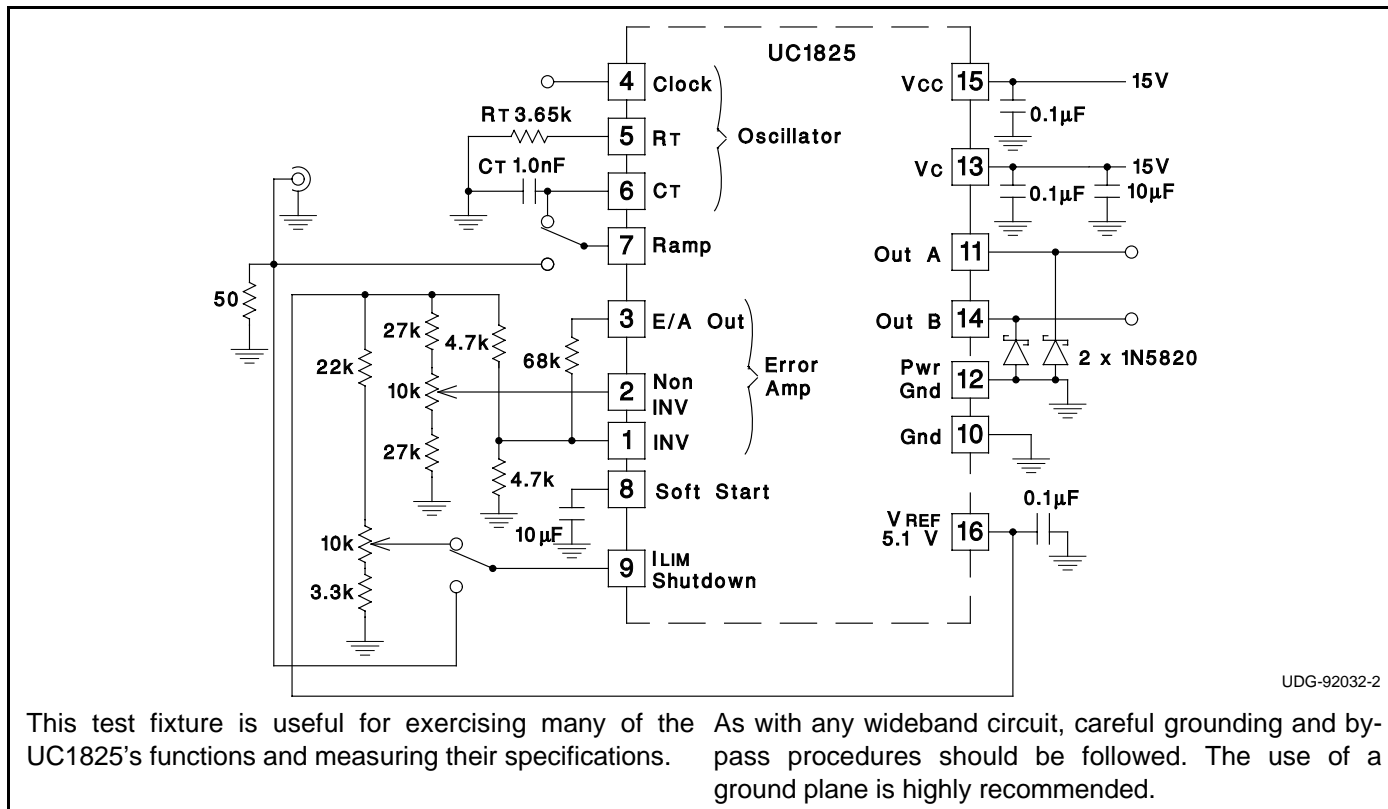
#### Rise/Fall Time (CL=10nF)



#### Saturation Curves



Open Loop Laboratory Test Fixture



Design Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency

