



Resonant-Mode Power Supply Controllers

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150µA typ.)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

Device	UVLO	Outputs	'Fixed'
1861	16.5/10.5	Alternating	Off Time
1862	16.5/10.5	Parallel	Off Time
1863	8/7	Alternating	Off Time
1864	8/7	Parallel	Off Time
1865	16.5/10.5	Alternating	On Time
1866	16.5/10.5	Parallel	On Time
1867	8/7	Alternating	On Time
1868	8/7	Parallel	On Time

DESCRIPTION

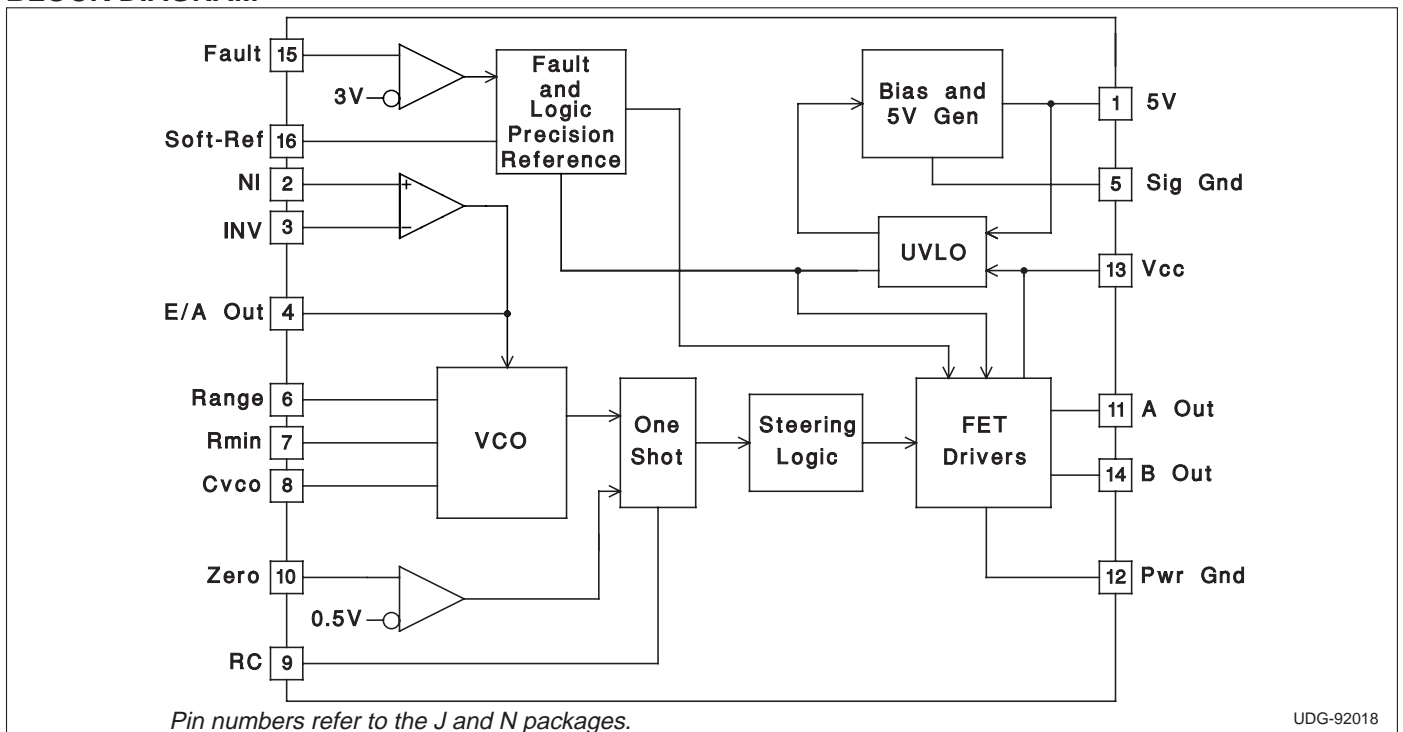
The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150 µA, and the outputs are actively forced to the low state. UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After Vcc exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison allowing a 2 Amp peak current.

ABSOLUTE MAXIMUM RATINGS

Vcc	22V
Output Current, Source or Sink (Pins 11 & 14) DC	0.5A
Pulse (0.5μs)	1.5A
Power Ground Voltage	±0.2V
Inputs (Pins 2, 3, 10, & 15)	-0.4 to 7V
Error Amp Output Current	±2mA
Power Dissipation	1W

Junction Temperature (Operating)	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages.

Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View) J or N, DW Packages

PLCC-20 & LCC-20 (Top View) Q & L Package

PACKAGE PIN FUNCTION	
FUNCTION	PIN
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
Cvco	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
Vcc	17
B Out	18
NC	19
Fault	20

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the UC186x, $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for the UC286x, and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the UC386x, $V_{CC}=12\text{V}$, $C_{VCO}=1\text{nF}$, $\text{Range}=7.15\text{k}$, $R_{MIN}=86.6\text{k}$, $C=200\text{pF}$, $R=4.02\text{k}$, and $C_{sr}=0.1\mu\text{F}$. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	$12\text{V} \leq V_{CC} \leq 20\text{V}$, $-10\text{mA} \leq I_o \leq 0\text{mA}$	4.8	5.0	5.2	V
Short Circuit Current	$V_o = 0\text{V}$	-150		-15	mA
Soft-Reference					
Restart Delay Current	$V = 2\text{V}$	10	20	35	μA
Soft Start Current	$V = 2\text{V}$	-650	-500	-350	μA
Reference Voltage	$T_J = 25^{\circ}\text{C}$, $I_o = 0\text{A}$	4.95	5.00	5.05	V
	$12\text{V} \leq V_{CC} \leq 20\text{V}$, $-200\mu\text{A} \leq I_o \leq 200\mu\text{A}$	4.85		5.15	V
Line Regulation	$12\text{V} \leq V_{CC} \leq 20\text{V}$		2	20	mV
Load Regulation	$-200\mu\text{A} \leq I_o \leq 200\mu\text{A}$		10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	$V_{CM} = 5\text{V}$, $V_o = 2\text{V}$, $I_o = 0\text{A}$	-10		10	mV
Input Bias Current	$V_{CM} = 0\text{V}$	-2.0	-0.3		μA
Voltage Gain	$V_{cm} = 5\text{V}$, $0.5\text{V} \leq V_o \leq 3.7\text{V}$, $I_o = 0\text{A}$	70	100		dB
Power Supply Rejection Ratio	$V_{cm} = 5\text{V}$, $V_o = 2\text{V}$, $12\text{V} \leq V_{CC} \leq 20\text{V}$	70	100		dB

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for $-55^{\circ}\text{C} \leq \text{T}_\text{A} \leq 125^{\circ}\text{C}$ for the UC186x, $-25^{\circ}\text{C} \leq \text{T}_\text{A} \leq 85^{\circ}\text{C}$ for the UC286x, and $0^{\circ}\text{C} \leq \text{T}_\text{A} \leq 70^{\circ}\text{C}$ for the UC386x, $\text{V}_{\text{CC}}=12\text{V}$, $\text{C}_{\text{VCO}}=1\text{nF}$, $\text{Range}=7.15\text{k}$, $\text{R}_{\text{MIN}}=86.6\text{k}$, $\text{C}=200\text{pF}$, $\text{R}=4.02\text{k}$, and $\text{C}_{\text{sr}}=0.1\mu\text{F}$. $\text{T}_\text{A}=\text{T}_\text{J}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	$0\text{V} \leq \text{V}_{\text{cm}} \leq 6\text{V}$, $\text{V}_\text{O} = 2\text{V}$	65	100		dB
V _{OUT} Low	$\text{V}_{\text{ID}} = -100\text{mV}$, $\text{I}_\text{O} = 200\mu\text{A}$		0.17	0.25	V
V _{OUT} High	$\text{V}_{\text{ID}} = 100\text{mV}$, $\text{I}_\text{O} = -200\mu\text{A}$	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
Voltage Controlled Oscillator					
Maximum Frequency	$\text{V}_{\text{ID}} (\text{Error Amp}) = 100\text{mV}$, $\text{T}_\text{J} = 25^{\circ}\text{C}$	450	500	550	kHz
	$\text{V}_{\text{ID}} (\text{Error Amp}) = 100\text{mV}$	425		575	kHz
Minimum Frequency	$\text{V}_{\text{ID}} (\text{Error Amp}) = -100\text{mV}$, $\text{T}_\text{J} = 25^{\circ}\text{C}$	45	50	55	kHz
	$\text{V}_{\text{ID}} (\text{Error Amp}) = -100\text{mV}$	42		58	kHz
One Shot					
Zero Comparator V _{th}		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	$\text{V}_{\text{ZERO}} = 1\text{V}$	850	1000	1150	ns
Maximum to Minimum Pulse Width Ratio	$\text{V}_{\text{ZERO}} = 0\text{V}$ UCx861 – UCx864	2.5	4	5.5	
	$\text{V}_{\text{ZERO}} = 0\text{V}$ UCx865 – UCx868	4	5.5	7	
Output Stage					
Rise and Fall Time	$\text{C}_{\text{LOAD}} = 1\text{nF}$ (Note 4)		25	45	ns
Output Low Saturation	$\text{I}_\text{O} = 20\text{mA}$		0.2	0.5	V
	$\text{I}_\text{O} = 200\text{mA}$		0.5	2.2	V
Output High Saturation	$\text{I}_\text{O} = -200\text{mA}$, down from V _{CC}		1.7	2.5	V
UVLO Low Saturation	$\text{I}_\text{O} = 20\text{mA}$		0.8	1.5	V
Fault Comparator					
Fault Comparator V _{th}		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns
UVLO					
V _{CC} Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
V _{CC} Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
I _{CC} Start	$\text{V}_{\text{CC}} = \text{V}_{\text{CC}(\text{on})} - 0.3\text{V}$		150	300	μA
I _{CC} Run	$\text{V}_{\text{ID}} = 100\text{mV}$		25	32	mA

Note 1: Currents are defined as positive into the pin.

Note 2: Pulse measurement techniques are used to insure that $\text{T}_\text{J} = \text{T}_\text{A}$.

Note 3: $\text{V}_{\text{ID}} = \text{V}(\text{NI}) - \text{V}(\text{INV})$.

Note 4: This parameter is not 100% tested in production but guaranteed by design.

Note 5: $\text{V}_\text{i} = 0$ to 4V $\text{tr}(\text{V}_\text{i}) \leq 10\text{ns}$ $\text{tpd} = \text{t}(\text{V}_\text{o} = 6\text{V}) - \text{t}(\text{V}_\text{i} = 3\text{V})$

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and V_{CC} is less than the upper UVLO threshold, I_{CC} will be less than 300 μA , the 5V generator will be off, and the outputs will be actively held low.

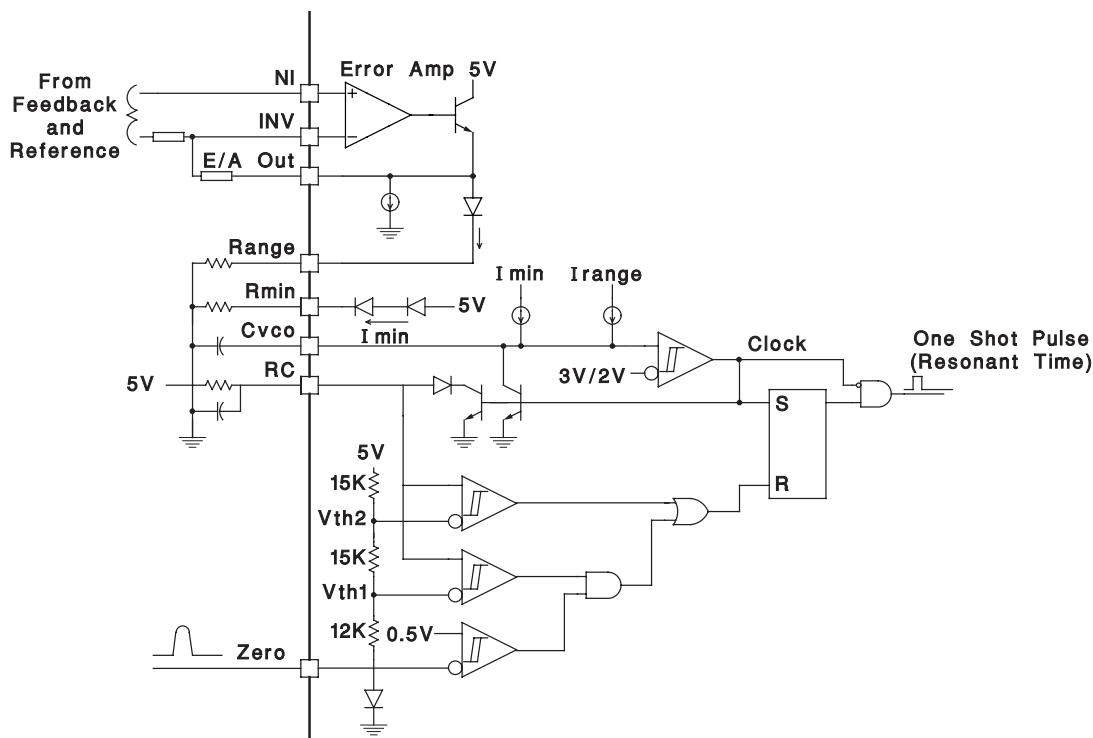
When V_{CC} exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1 μF capacitor. The capacitor should have low equivalent series resistance and inductance.

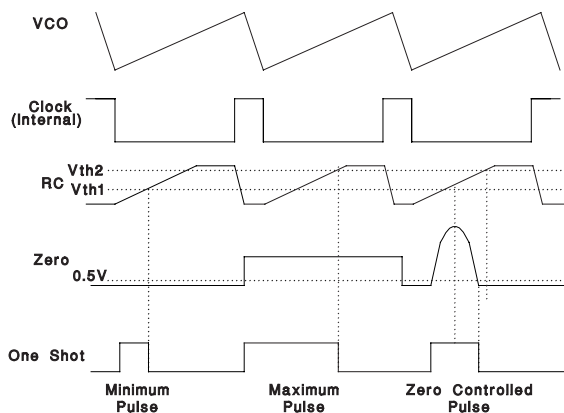
FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200 μA , this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1 μF . This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch re-

Error Amp, Voltage Controlled Oscillator, and One Shot



UDG-92022-1



UDG-92023-1

Figure 2

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{4.3}{R_{MIN} \cdot C_{VCO}}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.3}{(R_{MIN} // Range) \cdot C_{VCO}}$$

The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum

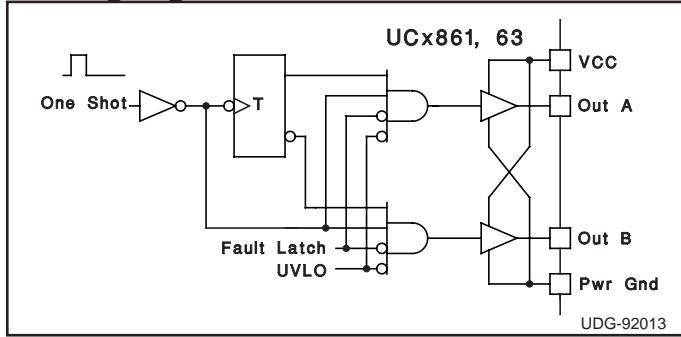
frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tp_{w}(min) \cong 0.3 \cdot R \cdot C.$$

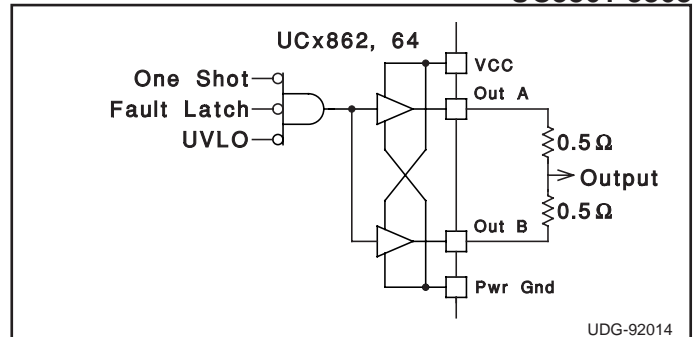
The maximum pulse width is approximately given by:

$$Tp_{w}(max) \cong 1.2 \cdot R \cdot C.$$

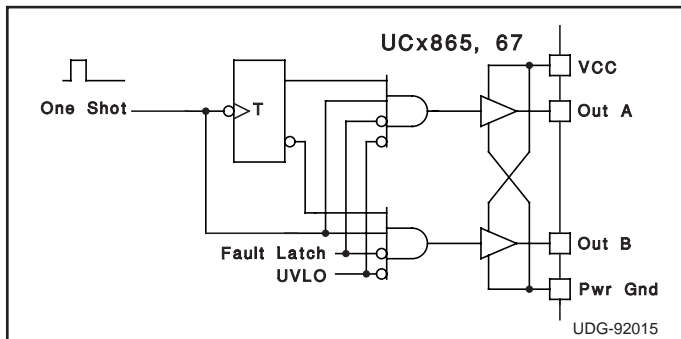
Steering Logic



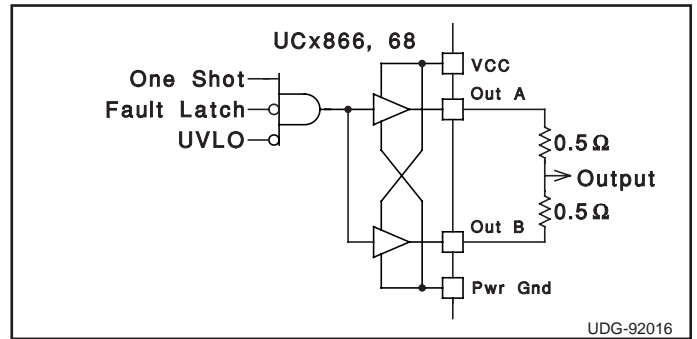
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

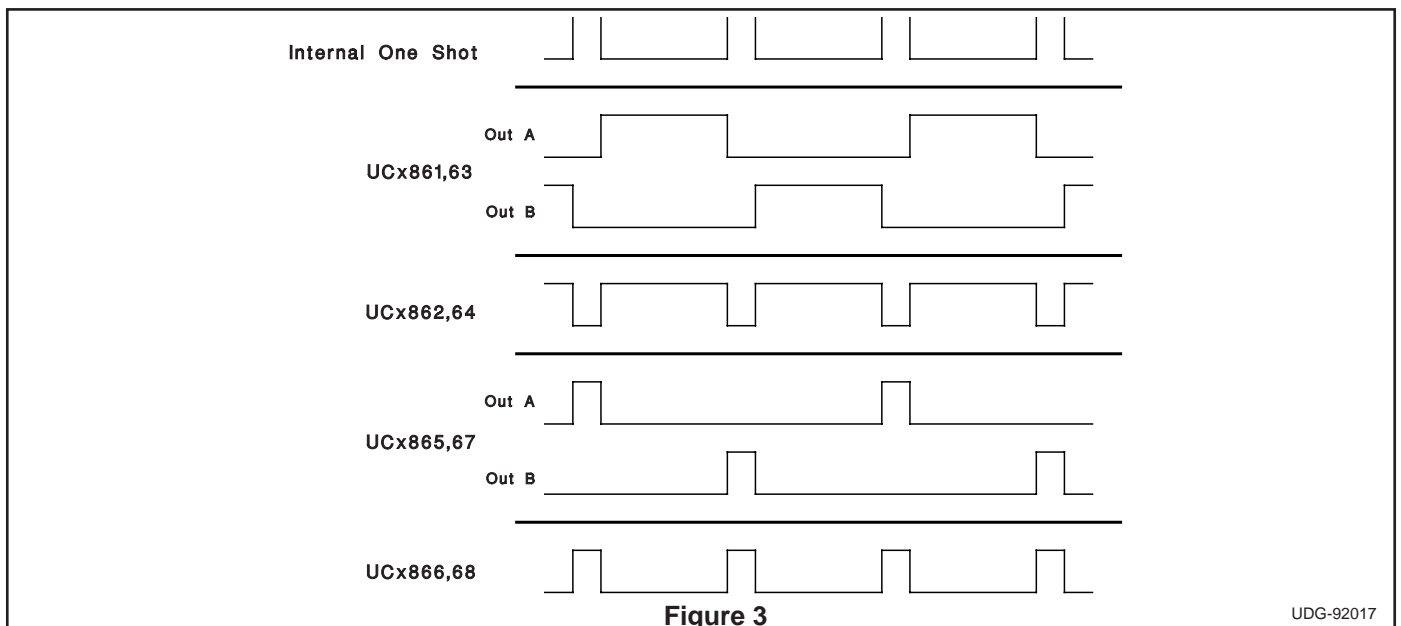


Figure 3

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