UNITRODE

UCC1582
UCC2582
UCC3582

PRELIMINARY

High Efficiency Synchronous, Step Down Controller

FEATURES

- BiCMOS Voltage Mode PWM Controller
- 4.5V to 7V Input Voltage Range
- Output Voltages as low as 1.25V
- Sleep Mode (I_C = 15µA typ)
- Lossless Short Circuit Current Limiting
- >90% Typical Efficiency
- 0% to 100% Duty Cycle Range
- 8-Pin Surface Mount Package

DESCRIPTION

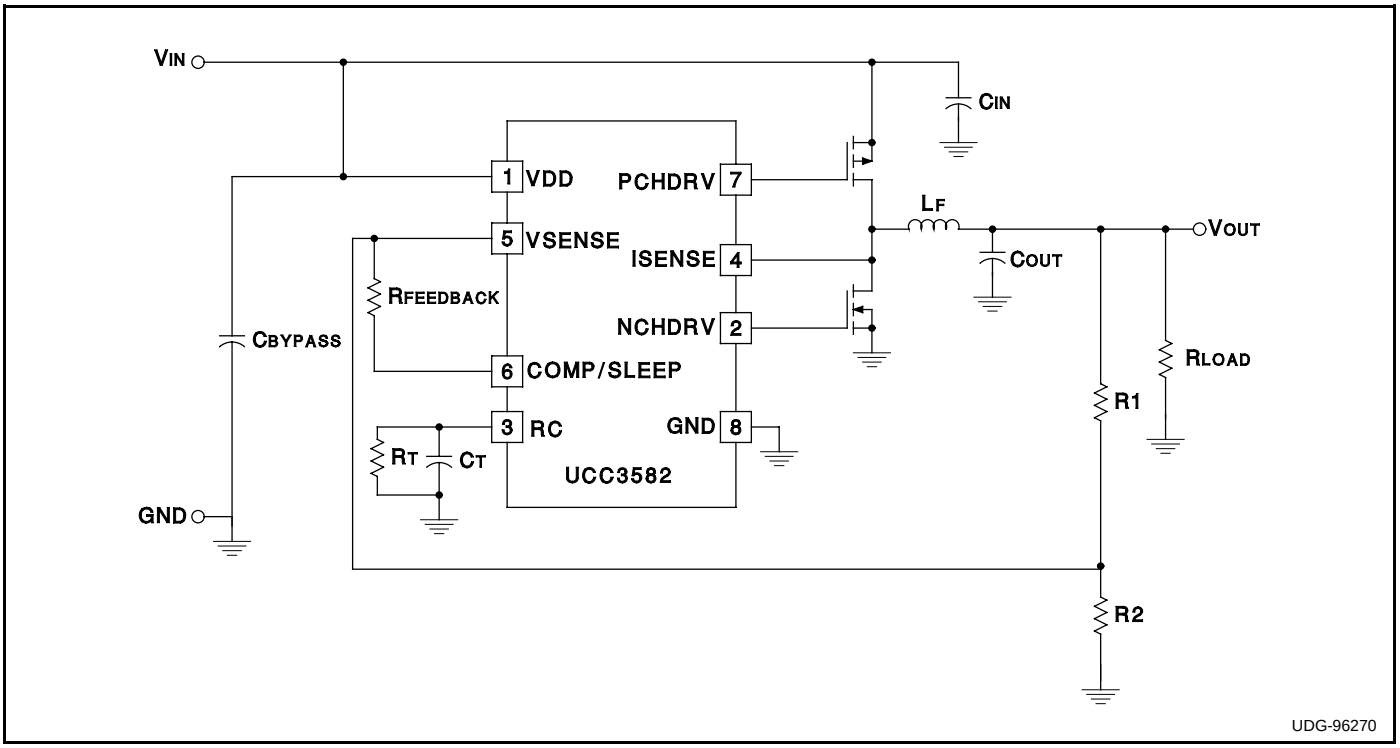
The UCC3582 family of synchronous step-down (Buck) regulators provides accurate high efficiency power conversion from input voltages ranging from 4.5V to 7V volts. Using few external components, the UCC3582 in an 8-pin surface mount package is especially suited for low voltage, battery powered applications where cost, small size and high efficiency are critical. A high level of integration and novel design allow this 8-pin controller to provide a complete control solution. High efficiency is obtained through the use of synchronous rectification.

Synchronous regulators replace the catch diode in the standard buck converter with a low R_{DS}(on) N-channel MOSFET switch allowing for significant efficiency improvements. The external high side switch is a P-channel MOSFET, negating the need for a charge pump and a complex high side driver. The UCC3582 provides the out of phase and non-overlapping gate drive signals needed to drive the external MOSFETs. The P-channel MOSFET voltage drop during conduction is sensed for lossless short circuit current limiting.

100% duty cycle operation allows the UCC3582 to operate as a low dropout regulator in the event of a low battery condition. A low power sleep mode can be commanded by externally forcing the COMP pin below 0.5V. Quiescent supply current in sleep mode is typically less than 15µA. The internal 5ms soft start provides for controlled ramp up of the output voltage with minimal overshoot. The undervoltage lockout threshold is set at 4.5V with 200mV of hysteresis.

Available packages include the 8-pin SOIC and Plastic and Ceramic Dips.

TYPICAL APPLICATION



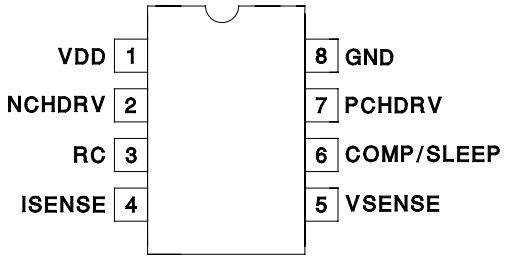
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD) 7V
Output Drivers (PCHDRV, NCHDRV) Currents
Continuous . . . . . ±0.25A
Peak. . . . . ±500mA
Inputs (VSENSE,COMP/SLEEP, RC, ISENSE) . . –0.3V to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8
D, N and J Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 470pF, RT = 10k, TA = -55°C to 125°C for UCC1582, –25°C to 85°C for UCC2582, 0°C to 70°C for UCC3582, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Sleep	V_{COMP} = 0V		14	25	µA
Supply Current, Operating			1.5	3	mA
VCC Turn-on Threshold			4.5	4.75	V
VCC Turn-off Threshold		4	4.3		V
Error Amplifier					
Input Voltage		1.23	1.25	1.27	V
VSENSE Bias Current		–500	25	500	nA
Open Loop Gain	V_{COMP} = 1V to 3V	70	100		dB
V_{OUT} High	R_{COMP} = 100k to GND		4.3		V
V_{OUT} Low	R_{COMP} = 100k to 5V		0.7		V
Output Source Current	VSENSE = 1.23V, V_{COMP} = 4V		–2		mA
Output Sink Current	VSENSE = 1.27V, V_{COMP} = 1V		2		mA
Oscillator					
Initial Accuracy	T_A = 25°C	180	200	220	kHz
Voltage Stability	VCC = 5V to 7V		1		%
Total Variation	Line, Temperature	175		225	kHz
Ramp Amplitude (p-p)			3.6	4.2	V
Ramp Valley Voltage		0.8	1.5		V
Sleep, Soft Start, Current Limit					
Sleep Threshold	Measured at V_{COMP}	0.3	0.4	0.5	V
Sleep Input Bias Current	V_{COMP} = 0V		–10		µA
Soft Start Time		2.5	5	7.5	ms
Reverse Current Offset		5	20	35	mV
Current Limit Threshold	Reference to V_{IN}	–360	–450	–540	mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
N-Channel and P-Channel Driver Outputs					
Output High Voltage	I_{OUT} = –50mA	4.0	4.5		V
Output Low Voltage	I_{OUT} = 50mA		0.5		V
Output Resistance	I_{OUT} = 100mA		15		Ω
Output Low (UVLO)	I_{OUT} = 10mA, VCC = 0V		0.9		V
Output Rise Time	C_{OUT} = 1nF		30		ns
Output Fall Time	C_{OUT} = 1nF		30		ns
Output Dead Time	C_{OUT} = 1nF		200		ns
Overcurrent Blank Time			300		ns
Reverse Current Blank Time			300		ns

PIN DESCRIPTIONS

COMP/SLEEP: This is the output of the voltage amplifier. The voltage at this output is inverted internally and connected to the non-inverting input of the PWM comparator. A lead-lag network around the voltage amplifier compensates for the two pole LC filter characteristic inherent to voltage mode control, and is required in order to optimize the dynamic performance of the voltage mode control loop. Sleep mode is invoked if COMP is pulled and held below 0.5V which can be accomplished by an external gate or transistor. Sleep mode supply current is 15μA typical.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

ISENSE: This input is connected to the junction between the two external power MOSFET transistors. The voltage drop across the upper P-channel device is monitored by ISENSE during conduction, and forms the current limit signal. When this drop exceeds 450mV the overcurrent comparator and logic sets the PWM latch and terminates the output pulse. The controller stops switching and goes through a soft start sequence. This prevents excess power dissipation in the NMOSFET during a short circuit. The reverse current comparator senses the drop across the lower N-channel MOSFET and disables the drive signal if a small positive voltage is present. A positive voltage is indicative of either P-channel conduction or reverse inductor current. To disable the overcurrent comparator, connect ISENSE to VDD.

PCHDRV, NCHDRV: The output drivers are rated for 0.5A peak currents. The PWM circuitry provides complementary drive signals to the output stages. Cross conduction of the external MOSFETs is prevented by monitoring the voltage on the P-channel and N-channel driver pins in conjunction with a time delay optimized for FET turn-off characteristics.

RC: A parallel capacitor and resistor combination from RC to GND sets the PWM oscillator frequency according to the following equation:

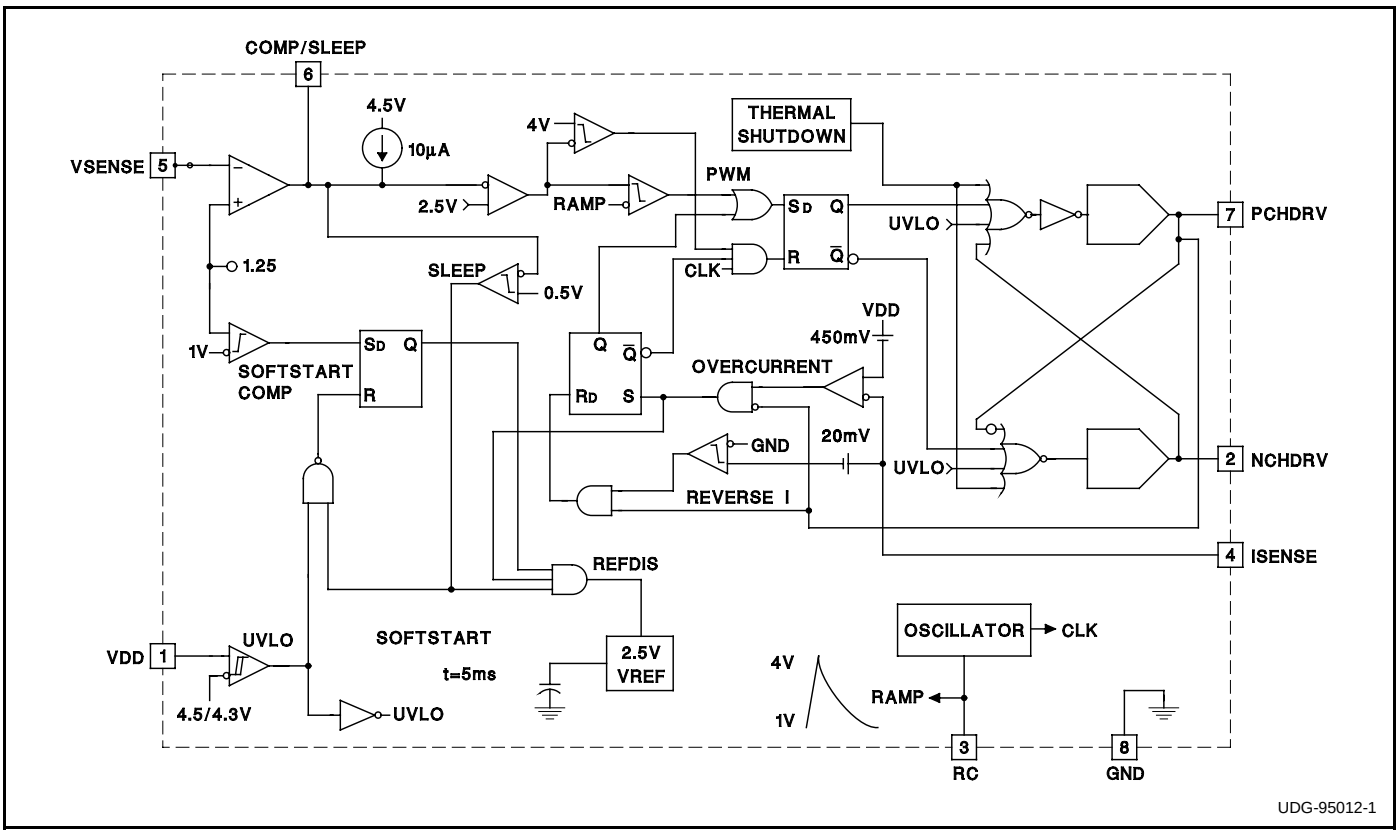
$$F \approx \frac{0.72}{RC}$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum C_T value of 200pF ensures good accuracy and less susceptibility to circuit layout parasitics. The waveform on RC has a fast linear charge and slow RC exponential discharge characteristic. The exponential characteristic improves converter response to input line voltage changes. The oscillator and PWM are designed to provide practical operation to 500kHz.

VDD: Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 1μF low ESL/ESR ceramic capacitor.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. It senses the output voltage through an external divider.

BLOCK DIAGRAM



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