12-Bit, 3 MSPS, A to D Converter

AD1672

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. This brochure may be found at: http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD1672

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD1672-703D	12-Bit , 3 MSPS, A to D Converter
AD1672-703F	12-Bit , 3 MSPS, A to D Converter
AD1672-713D	12-Bit , 3 MSPS, A to D Converter with radiation test
AD1672-713F	12-Bit , 3 MSPS, A to D Converter with radiation test

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
D	GDIP2-T28	28-Lead Sidebrazed DIP package
F	CDFP3-F28	28-Lead bottom-brazed flatpack

PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
DRCOM	1	P	Digital Output Driver Ground.
BIT 12	2	DO	Data Bit (LSB).
BIT 2–11	3–12	DO	Data Bits.
BIT 1	13	DO	Data Bit (MSB).
DRV_{DD}	14	P	+5 V Digital Output Driver Supply.
OTR	15	DO	Out of Range is Active High on the leading edge of Code 0 or the trailing edge of Code 4096. See Output Data Format Table V.
CLOCK	16	DI	Sample Clock.
V_{DD}	17	P	+5 V Digital Supply.
DCOM	18	P	Digital Ground.
REFCOM	19, 24	P	Analog Ground.
REFOUT	20	AO	2.5 V Reference Output (Decouple with 1 µF ceramic capacitor to REFCOM).
AIN1	21	AI	Analog Input.
AIN2	22	AI	Analog Input.
REFIN	23	AI	Reference Input.
NCOMP2	25	AO	Noise Compensation (Decouple with 1 µF ceramic capacitor to ACOM).
NCOMP1	26	AO	Noise Compensation (Decouple with 1 µF ceramic capacitor to ACOM).
ACOM	27	P	Analog Ground.
V_{CC}	28	P	+5 V Analog Supply.

TYPE: AI = Analog Input; DI = Digital Input; P = Power; AO = Analog Output; DO = Digital Output.

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{CC} with respect to ACOM.....-0.5 to +6.5V
V_{DD} with respect to DCOM.....-0.5 to +6.5V
DRV_{DD} with respect to DRCOM .....-0.5 to +6.5V
ACOM with respect to DCOM, DRCOM.....-0.5 to +0.5V
Clock with respect to DCOM.....-0.5 to V_{DD} + 0.5V
Digital Outputs with respect to DCOM..... -0.5V to DRV_{DD} + 0.5V
AIN with respect to ACOM .....-6.5V to +6.5V
REFIN with respect to ACOM..... -0.5V to V_{CC} + 0.5V
Junction Temperature (T_J).....+150°C
Operating Temperature Range.....-55°C to + 125°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (10 sec).....+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

3.1 Thermal Characteristics:

Thermal Resistance, Sidebrazed (D) Package

Junction-to-Case (Θ_{JC}) = 28°C/W Max

Junction-to-Ambient (Θ_{JA}) = 70°C/W Max

Thermal Resistance, Bottom brazed (F) Package

Junction-to-Case (Θ_{JC}) = 22°C/W Max

Junction-to-Ambient (Θ_{JA}) = 60°C/W Max

4.0 Electrical Table:

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min.	Limit Max	Units
RESOLUTION		No Missing Codes	1,2,3	12		Bits
Supply Current	I_{VCC} I_{VDD} I_{DRVDD}		1,2,3		65 2 2	mA
Power dissipation	PD		1,2,3		363	mW
Power supply rejection 3/	PSR	V_{CC}=5.0V ± 0.25V V_{DD}=5.0V ± 0.25V V_{DRDD}=3.0V to 5.25V	1,2,3	-0.3 -0.3 -0.1	0.3 0.3 0.1	%FSR
ACCURACY Integral Nonlinearity Differential Nonlinearity Offset Error Zero Error 5/ Gain Error 2/	 INL DNL VOSE		1,2,3	 -2.5 -1 -0.75 -0.75 -1.5	 2.5 1.5 0.75 0.75 1.5	 LSB LSB %FSR %FSR %FSR
Internal Voltage Reference	V_O	Iout = 0.5 mA 4/	1,2,3	2.475	2.525	V
Analog Input		2.5V Range Unipolar 5.0V Range Unipolar	1,2,3	0 0	2.5 5	V

4.0 Electrical Table: (Cont'd)

Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min.	Limit Max	Units
		5.0V Bipolar		-2.5	2.5	
Input Resistance		2.5V Input Range 5.0V Input Range	1,2,3	1.5 3	2.5 5	Kohm
Output Voltage, High	V_{OH}	$I_{OH=}$ 0.5 mA	1,2,3	2.4		V
Output Voltage, Low	V_{OL}	$I_{OL=}$ 1.6 mA	1,2,3		0.4	V
Logic Inputs Logic "0" Input Current Logic "1" Input Current	 I_{IH} I_{IL}	 $V_{IH}=V_{DD}$ $V_{IL}=0V$	1,2,3	-10	10	uA
AC Parameters:						
Parameter See notes at end of table	Symbol	Conditions 1/ Unless Otherwise Specified	Sub Group	Limit Min.	Limit Max	Units
Signal to Noise Distortion (S/(N+D))		f_{input}=500KHz	9 10,11	63 62		dB
Signal to Noise Ratio	SNR	f_{input}=500KHz	9 10,11	66 62		dB
Total Harmonic Distortion	THD	f_{input}=500KHz	9,10,11	-64		dB
Spurious Free Dynamic Range	SFDR	f_{input}=500KHz	9,10,11	-65		dB

NOTES:

1/ $V_{CC} = V_{DD} = V_{DRVDD} = +5.0V$.
2/ Includes internal reference error.
3/ Change in full scale as a function of the dc supply voltage.
4/ Current available for external loads. External load should not change during conversion.
5/ Bipolar Mode

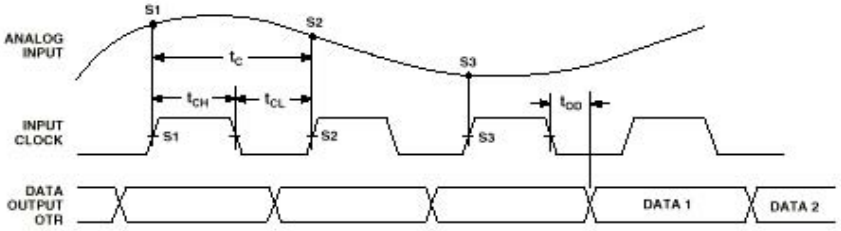

Figure 1. Timing Diagram

SWITCHING SPECIFICATIONS

Parameter	Symbol	Value	Units
Clock Period	t_C	334	ns min
Clock			
Pulse Width High	t_{CH}	167	ns min
Pulse Width Low	t_{CL}	167	ns min
Output Delay	t_{OD}	15	ns min
		30	ns typ
Pipeline Delay (Latency)		2.5	Clock Cycles

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 9, 10, 11 1/ 2/
Group A Test Requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. No other subgroups are included in PDA.
2/ See table III for delta parameters.

4.2 Table III. Life Test/Burn-In test delta limits.

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
I_{CC}	65	±10%	mA
V_{OH}	2.4	±0.24	V
V_{OL}	0.4	±0.1	V

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition D.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Apr. 20, 2000
B	Add Flatpack, Add radiation part number, Add timing information on page 3.	Mar. 22, 2001
C	Update web address.	Feb. 7, 2002
D	Change subgroups 4, 5, 6 to 9, 10, 11. Update web address	Jan. 9, 2003
E	Delete Burn-In circuit.	Aug. 5, 2003
F	Update header/footer and add to 1.0 Scope description	Feb. 19,2008
G	Add Operating Temperature Range to Section 3.0 & Remove (See Figure 2) in Sections 5.2 and 5.3	April 4, 2008