Single Channel, 16-Bit, Serial Input, Unipolar/Bipolar Voltage Output DAC

Preliminary Technical Data

AD5502

FEATURES

16-Bit Resolution and Monotonicity
Voltage Output Ranges:
0-5V, 0-10V, 0-40V, ±5V, ±10V,
10% over-range
0.05% Total Unadjusted Error (TUE)
3ppm/°C Output Drift
Flexible Serial Digital Interface
On-Chip Reference (10 ppm/°C Max)
Asynchronous CLR Function
Dual Power Supply Range
AV_{DD} : 10.8V to 26.4 V
AV_{SS} : -26.4V to -3V/0V
Single Power Supply Range
AV_{DD} : 10.8V to 42 V
Temperature Range: -40°C to +85°C
TSSOP Package

APPLICATIONS

Process Control
Actuator Control
PLC
Motor Control

GENERAL DESCRIPTION

The AD5502 is a low-cost, precision, fully integrated 16-bit converter offering a programmable voltage output designed to meet the requirements of industrial process control applications.

The output voltage range is programmable to provide four ranges; 0V to 5V, 0V to 10V, 0V to 40V, ±5V and ±10V.

Analog outputs are short circuit protected and can drive capacitive loads of 1uF. The device is specified to operate with a single power supply range from 10.8 V to 42 V and a dual power supply range up to ±26.4V.
The flexible serial interface is SPI and MICROWIRE compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on-reset function ensuring that the device powers up in a known state and an asynchronous CLR pin which sets the outputs to zero-scale / mid-scale voltage output.The total output error is typically 0.05% FSR.

FUNCTIONAL BLOCK DIAGRAM

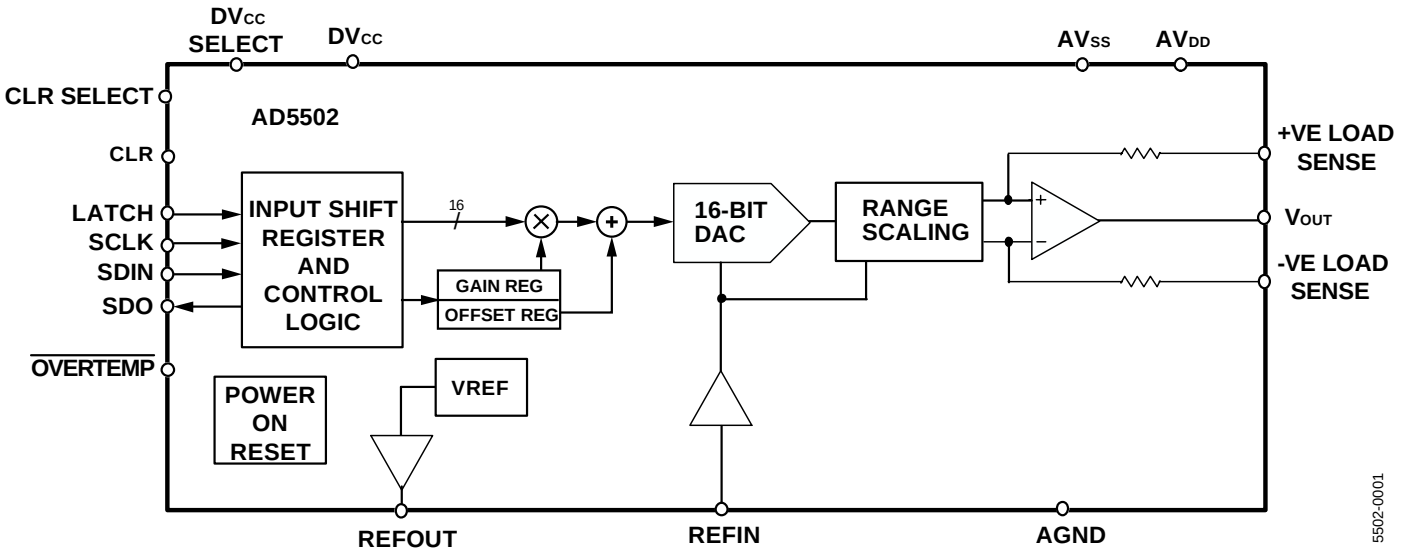

Figure 1

Rev. Pr B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

Pr B – Preliminary Version.

SPECIFICATIONS

AV_{DD} = 10.8V to 26.4V, AV_{SS} = -26.4V to -3V/0V, AV_{DD} + |AV_{SS}| < 52.8V, GND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 2 kΩ, C_L = 200 pF, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

Parameter	Value[1]	Unit	Test Conditions/Comments
Output Voltage Ranges	0 to 5	V	
	0 to 10	V	
	0 to 40	V	AV_{DD} = 42V
	-5 to +5	V	
	-10 to +10	V	
ACCURACY			Output unloaded
Bipolar Output			
Resolution	16	Bits	
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time, typically 0.05% FSR
TUE TC[2]	±3	ppm typ	
Relative Accuracy (INL)	±4	LSB max	B Grade
	±8	LSB max	A Grade
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Bipolar Zero Error	±5	mV max	@ 25°C, error at other temperatures obtained using bipolar zero TC
Bipolar Zero TC[2]	±3	ppm FSR/°C max	
Zero-Scale Error	±1	mV max	@ 25°C, error at other temperatures obtained using zero scale TC
Zero-Scale TC[2]	±3	ppm FSR/°C max	
Gain Error	±0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC[2]	±8	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC[2]	±3	ppm FSR/°C max	
Unipolar Output			AV_{SS} = 0 V
Resolution	16	Bits	
Total Unadjusted Error (TUE)	0.1	% FSR max	Over temperature, supplies, and time, typically 0.05% FSR
Relative Accuracy (INL)	±4	LSB max	B Grade
	±8	LSB max	A Grade
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Zero Scale Error	+10	mV max	@ 25°C, error at other temperatures obtained using gain TC
Zero Scale TC[2]	±3	ppm FSR/°C max	
Offset Error	±10	mV max	
Gain Error	±0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC[2]	±3	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC[2]	±3	ppm FSR/°C max	
OUTPUT CHARACTERISTICS[2]			
Headroom	1.4	V max	
	0.5	V typ	
Output Voltage TC	±3	ppm FSR/°C max	
Output Voltage Drift vs. Time	±12	ppm FSR/500 hr typ	Output value
	±15	ppm FSR/1000 hr typ	

Parameter	Value[1]	Unit	Test Conditions/Comments
Short-Circuit Current	10	mA max	
Load	2	kΩ min	For specified performance
Capacitive Load Stability			
$R_L = \infty$	2000	pF max	
$R_L = 2$ kΩ	TBD	pF max	
DC Output Impedance	0.3	Ω typ	
Power-On Time	TBD	µs typ	
PSRR	TBD	µV/V	
REFERENCE INPUT/OUTPUT			
Reference Input[2]			
Reference Input Voltage	5	V nom	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±10	µA max	Typically ±30 nA
Reference Range	4/5.002	V min/V max	
Reference Output			
Output Voltage	4.998/5.002	V min/V max	@ 25°C
Reference TC	±10	ppm/°C max	
Output Noise (0.1 Hz to 10 Hz)[2]	18	µV p-p typ	
Noise Spectral Density[2]	75	nV/√Hz typ	@ 10 kHz
Output Voltage Drift vs. Time[2]	±40	ppm/500 hr typ	
	±50	ppm/1000 hr typ	
Line Regulation[2]	10	ppm/V typ	
Load Regulation[2]	TBD	ppm/mA	
Thermal Hysteresis[2]	TBD	ppm	
DIGITAL INPUTS[2]			DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±1	µA max	Per pin
Pin Capacitance	10	pF typ	Per pin
DIGITAL OUTPUTS (SDO)[2]			
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 5 V ± 10%, sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} − 1	V min	DV_{CC} = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DV_{CC} = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} − 0.5	V min	DV_{CC} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	
High Impedance Output Capacitance	5	pF typ	
POWER REQUIREMENTS			
AV_{DD}	10.8 to 42	V min to V max	Single supply mode; AV_{SS} = 0 V
AV_{DD}	10.8 to 26.4	V min to V max	Dual supply mode
AV_{SS}	-26.4 to -3/0	V min to V max	
DV_{CC}	2.7 to 5.5	V min to V max	
AI_{DD}	TBD	mA	Output unloaded
AI_{SS}	TBD	mA	Output unloaded
DI_{CC}	1	mA max	$V_{IH} = DV_{CC}$, V_{IL} = GND, TBD mA typ
Power Dissipation	TBD	mW typ	AV_{DD} = 24V, AV_{SS} = -24 V, V_{OUT} unloaded

[1] Temperature range: -40°C to +85°C; typical at +25°C.
[2] Guaranteed by characterization. Not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 10.8V to 26.4V, AV_{SS} = -26.4V to -3V/0V, AV_{DD} + $|AV_{SS}|$ < 52.8V, GND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 2 kΩ, C_L = 200 pF, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 2.

Parameter[1]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	8	µs typ	Full-scale step (10 V) to ±0.03% FSR
	10	µs max	
	5	µs max	512 LSB step settling
Output Current Settling Time	10	µs max	To 0.1% FSR
Slew Rate	1	V/µs typ	
Power-On Glitch Energy	10	nV-sec typ	
Digital-to-Analog Glitch Energy	10	nV-sec typ	
Glitch Impulse Peak Amplitude	20	mV typ	
Digital Feedthrough	1	nV-sec typ	
Output Noise (0.1 Hz to 10 Hz Bandwidth)	0.1	LSB p-p typ	
Output Noise (100 kHz Bandwidth)	80	µV rms max	
1/f Corner Frequency	1	kHz typ	
Output Noise Spectral Density	100	nV/√Hz typ	Measured at 10 kHz
AC PSRR	TBD	dB	200mV 50/60Hz Sinewave superimposed on power supply voltage.

[1] Guaranteed by characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 10.8V to 26.4V, AV_{SS} = -26.4V to -3V/0V, AV_{DD} + |AV_{SS}| < 52.8V, GND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 2 kΩ, C_L = 200 pF, all specifications T_{MIN} to T_{MAX} unless otherwise noted.

Table 3.

Parameter[1,2,3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
Write Mode			
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK low time
t_3	13	ns min	SCLK high time
t_4	13	ns min	LATCH delay time
t_5	40	ns min	LATCH high time
t_5	5	µs min	LATCH high time (After a write to the Control register)
t_6	5	ns min	Data setup time
t_7	5	ns min	Data hold time
t_8	40	ns min	LATCH low time
t_9	20	ns min	CLR pulsewidth
t_{10}	5	µs max	CLR activation time
Readback Mode			
t_{11}	82	ns min	SCLK cycle time
t_{12}	33	ns min	SCLK low time
t_{13}	33	ns min	SCLK high time
t_{14}	13	ns min	LATCH delay time
t_{15}	40	ns min	LATCH high time
t_{16}	5	ns min	Data setup time
t_{17}	5	ns min	Data hold time
t_{18}	40	ns min	LATCH low time
t_{19}	40	ns max	Serial output delay time ($C_{L\ SDO}$[4] = 15pF)
t_{20}	33	ns max	LATCH rising edge to SDO tri-state
Daisychain Mode			
t_{21}	82	ns min	SCLK cycle time
t_{22}	33	ns min	SCLK low time
t_{23}	33	ns min	SCLK high time
t_{24}	13	ns min	LATCH delay time
t_{25}	40	ns min	LATCH high time
t_{26}	5	ns min	Data setup time
t_{27}	5	ns min	Data hold time
t_{28}	40	ns min	LATCH low time
t_{29}	40	ns max	Serial output delay time ($C_{L\ SDO}$[4] = 15pF)

[1] Guaranteed by characterization. Not production tested.
[2] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2V.
[3] See Figure 2, Figure 3 and Figure 4.
[4] $C_{L\ SDO}$ = Capactive load on SDO output.

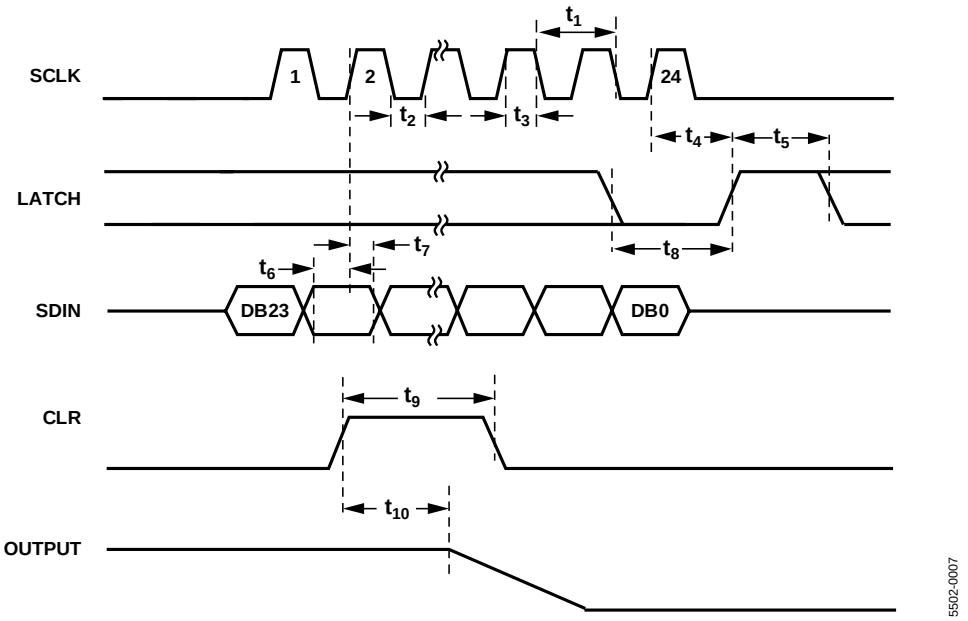


Figure 2. Write Mode Timing Diagram

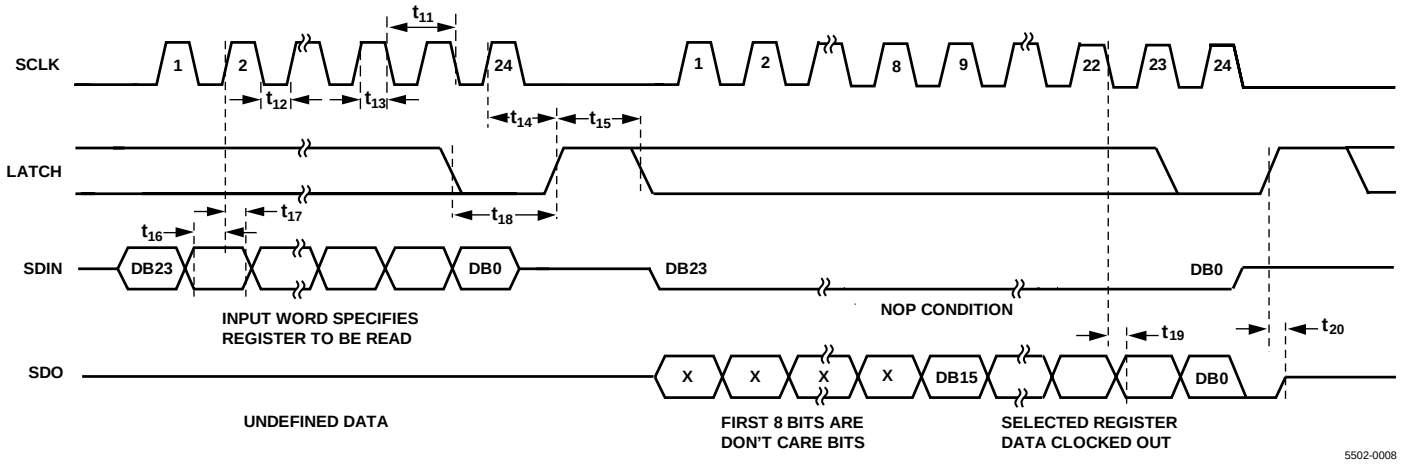


Figure 3. Readback Mode Timing Diagram

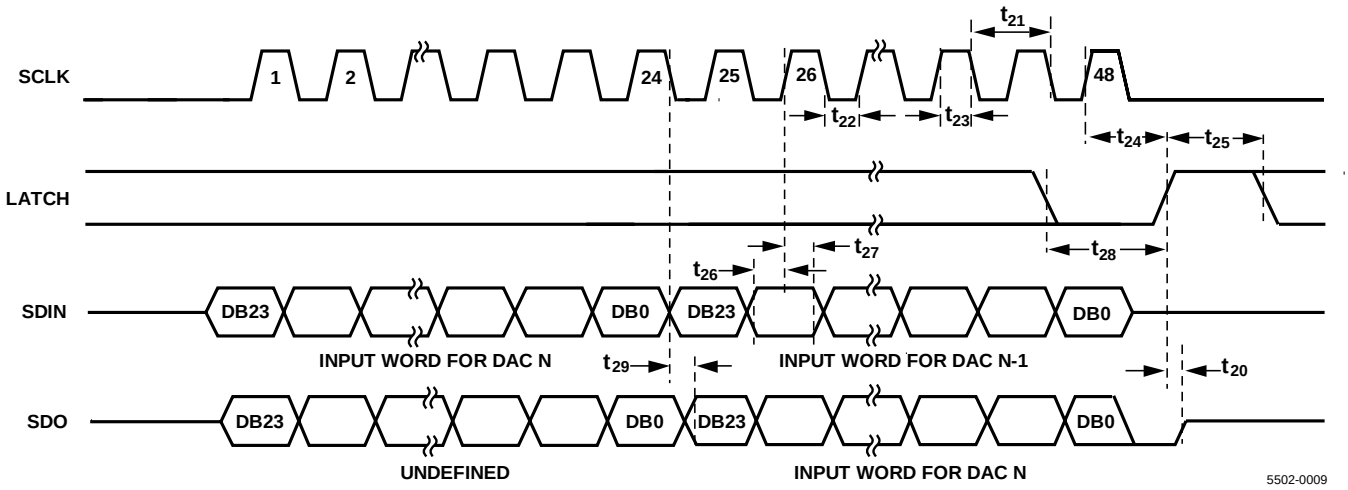


Figure 4. Daisychain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to 48 V
AV_{SS} to AGND	+0.3 V to −48 V
AV_{DD} to AV_{SS}	-0.3 V to 60 V
DV_{CC} to AGND	−0.3 V to +7 V
Digital Inputs to AGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to AGND,	−0.3 V to DV_{CC} + 0.3 V or 7V (whichever is less)
REFIN/REFOUT to AGND,	−0.3 V to +7 V
V_{OUT} to AGND,	AV_{SS} to AV_{DD}
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	42°C/W
Power Dissipation	(T_J max – T_A)/ θ_{JA}
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

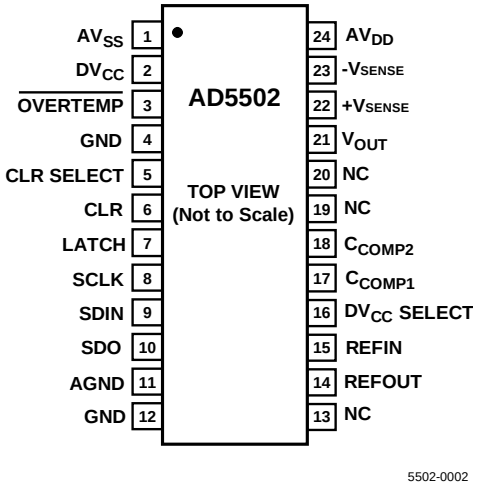


Figure 5. TSSOP Pin Configuration

Table 5. Pin Function Descriptions

TSSOP Pin No.	Mnemonic	Description
1	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from –26.4 V to –3 V. This pin can be connected to 0V if output voltage range is unipolar.
2	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
3	$\overline{\text{OVERTEMP}}$	Over Temperature alert, This pin is asserted low when an over temperature event is detected. The output pin is open drain and must be connected to a pull-up resistor.
4,12	GND	These pins must be connected to 0V.
13,19,20	NC	No Connection.
5	CLR SELECT	Selects the voltage output CLR value, either zero-scale or mid-scale code. See Table 19
6	CLR	Active High Input. Asserting this pin sets the voltage output to the user selected value (zero-scale or mid-scale).
7	LATCH	Positive edge sensitive latch, a rising edge parallel loads the input shift register data into the DAC register, also updating the output.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is clocked out on the falling edge of SCLK and is valid on the falling edge of SCLK.
11	AGND	Ground reference pin.
14	REFOUT	Internal Reference Voltage Output.
15	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for specified performance.
16	DV_{CC} SELECT	This pin when connected to GND disables the internal supply and an external supply must be connected to the DV_{CC} pin. Leaving this pin unconnected enables the internal supply. Refer to Features section for more information.
17	C_{COMP1}	Optional compensation capacitor connection for the voltage output buffer. Connecting a 4nF
18	C_{COMP2}	capacitor between these pins allows the voltage output to drive capacitive loads of up to 1µF.
21	V_{OUT}	Buffered Analog Output Voltage. The output amplifier is capable of directly driving a 2 kΩ, 2000 pF load.
22	$+V_{SENSE}$	Positive load connection sense input.
23	$-V_{SENSE}$	Ground load connection sense input.
24	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8V to 26.4V.
Paddle	AV_{SS}	Negative Analog Supply Pin. Voltage ranges from –26.4V to –3 V. This pin can be connected to 0V if output voltage range is unipolar.

TYPICAL PERFORMANCE CHARACTERISTICS

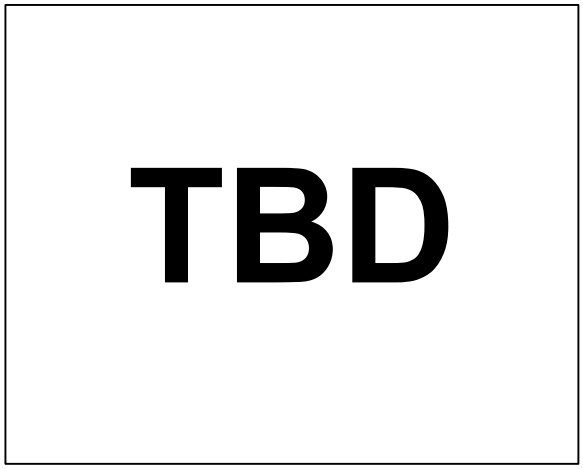


Figure 6. Integral Non Linearity Error vs DAC Code (Four Traces)

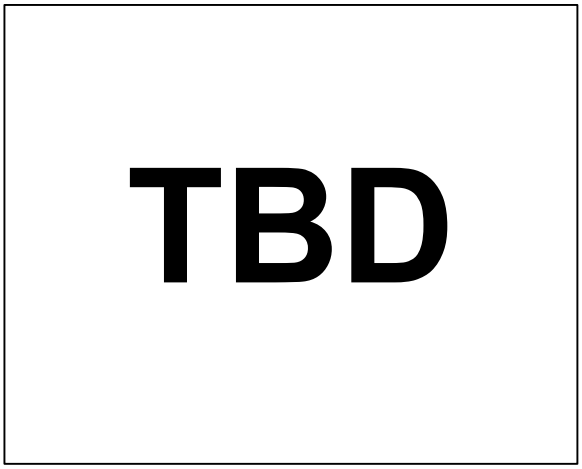


Figure 9. Integral Non Linearity vs. Temperature (Four Traces)

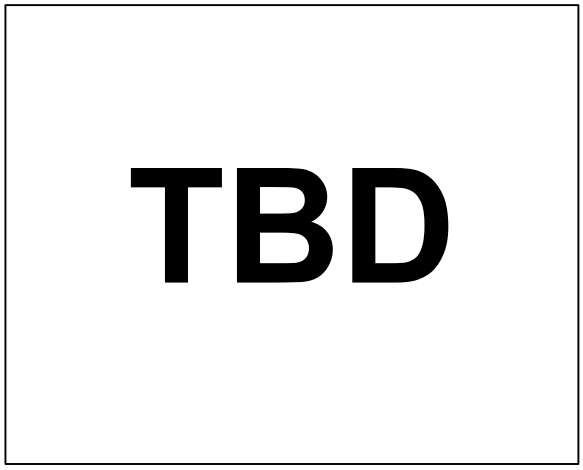


Figure 7. Differential Non Linearity Error vs. DAC Code (Four Traces)

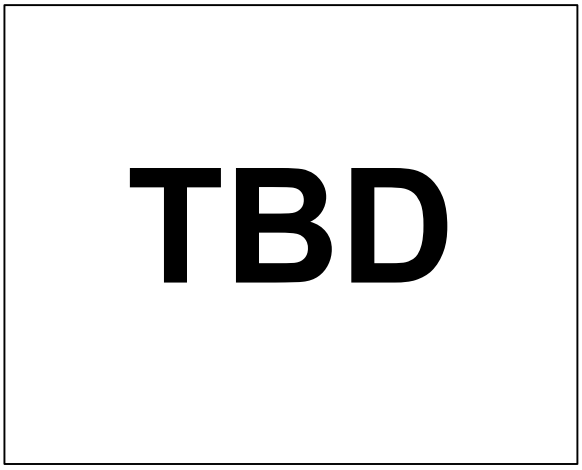


Figure 10. Differential Non Linearity vs. Temperature (Four Traces)

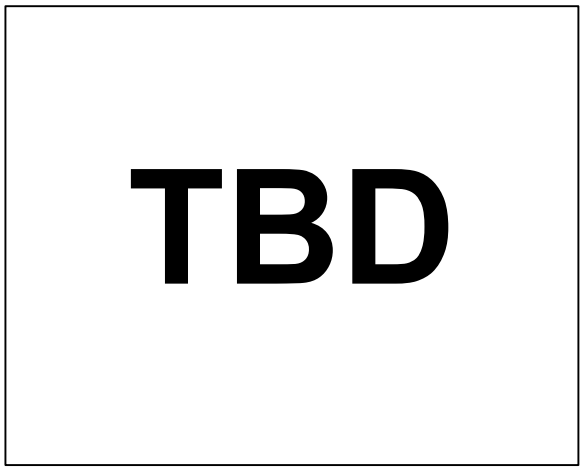


Figure 8. Total Unadjusted Error vs. DAC Code (Four Traces)

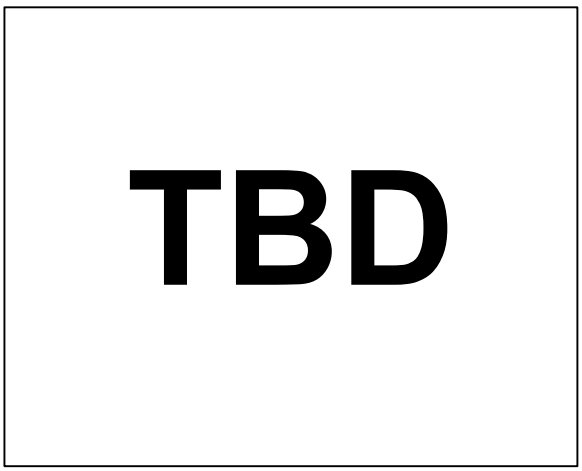


Figure 11. Integral Non Linearity vs. Supply Voltage (Four Traces)

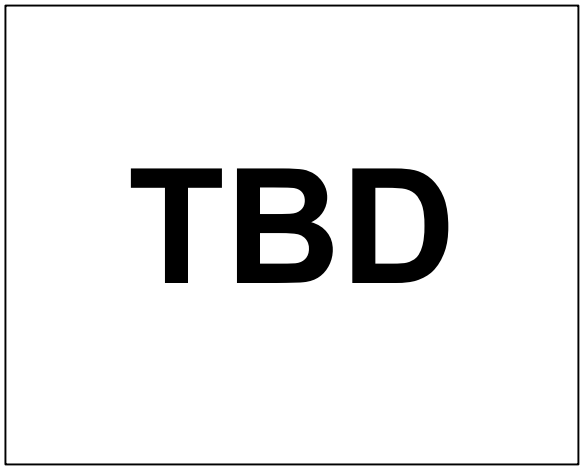


Figure 12.Differential Non Linearity Error vs. Supply Voltage (Four Traces)

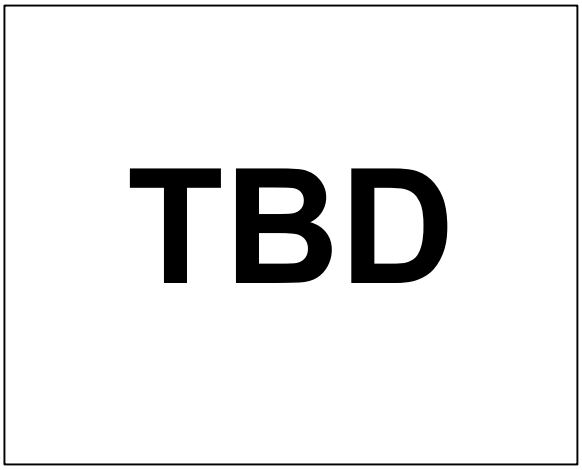


Figure 15. Total Unadjusted Error vs.Reference Voltage (Four Traces)

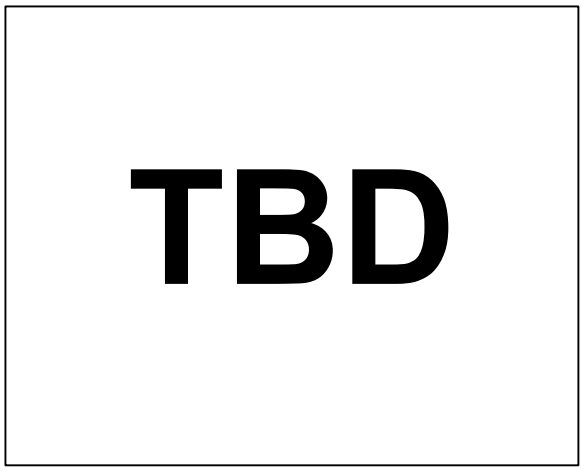


Figure 13. Integral Non Linearity Error vs. Reference Voltage (Four traces)

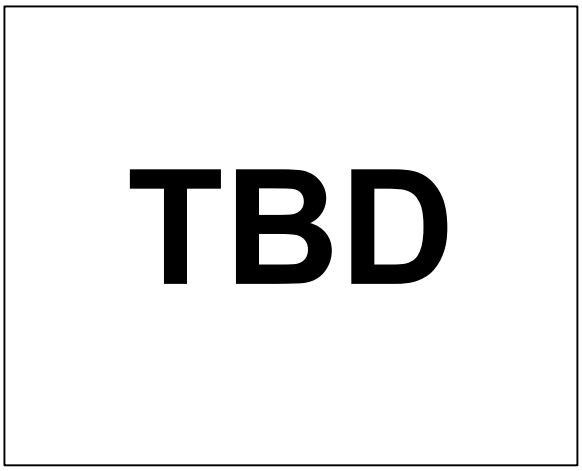


Figure 16. Total Unadjusted Error vs. Supply Voltage (Four Traces)

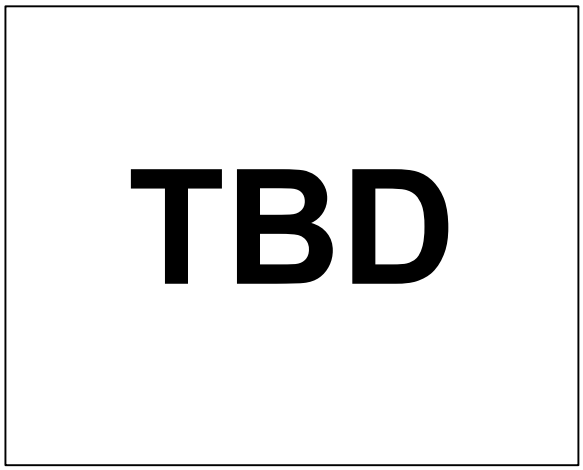


Figure 14. Differential Non Linearity Error vs. Reference Voltage (Four Traces)

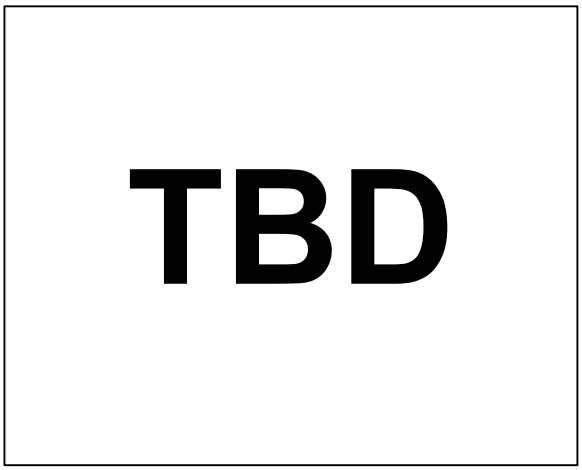


Figure 17. Offset Error vs.Temperature

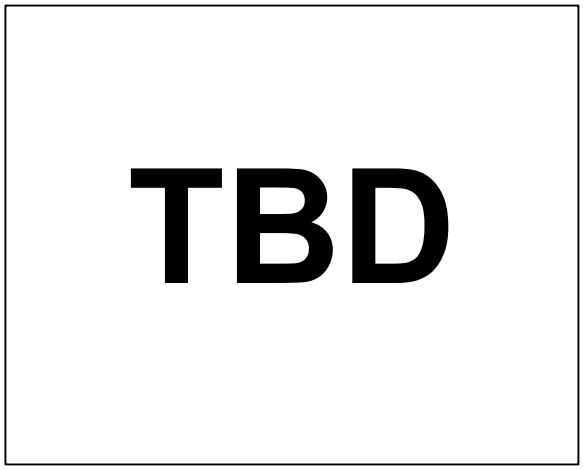


Figure 18. Bipolar Zero Error vs. Temperature

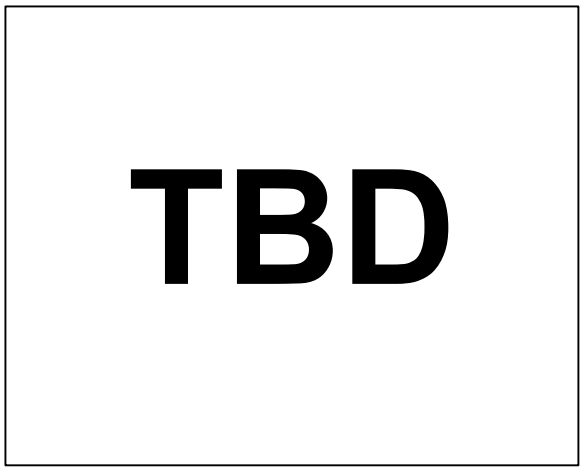


Figure 19. Zero-Scale Error vs. Temperature

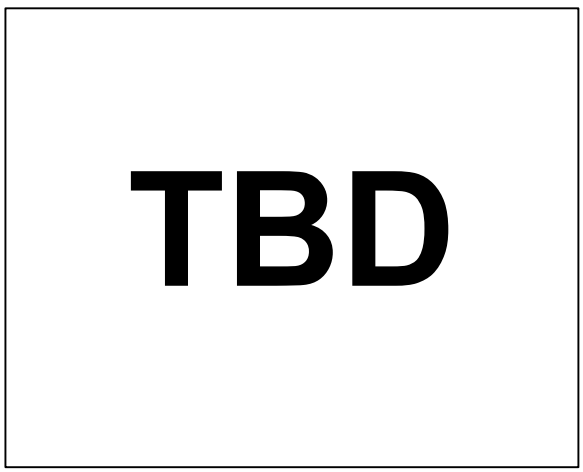


Figure 20. Gain Error vs. Temperature

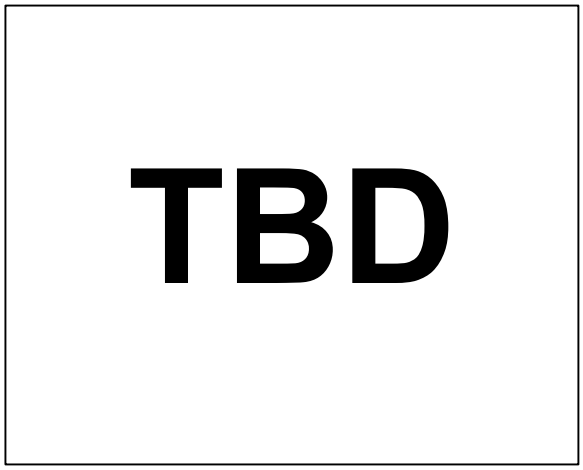


Figure 21. Source and Sink Capability of Output Amplifier Full-Scale Code Loaded

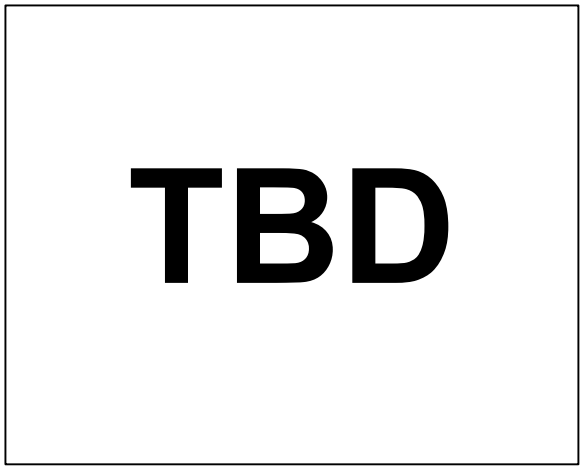


Figure 22. Source and Sink Capability of Output Amplifier Zero-Scale Loaded

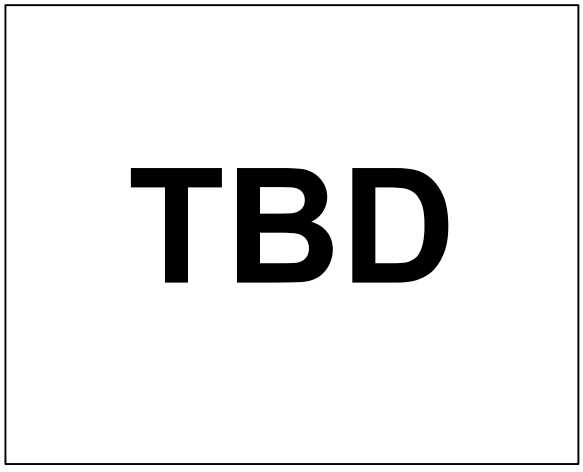


Figure 23.Full-Scale Positive Step

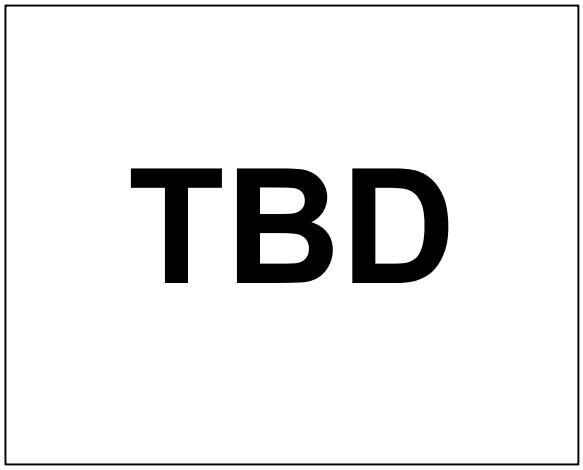


Figure 24. Full-Scale Negative Step

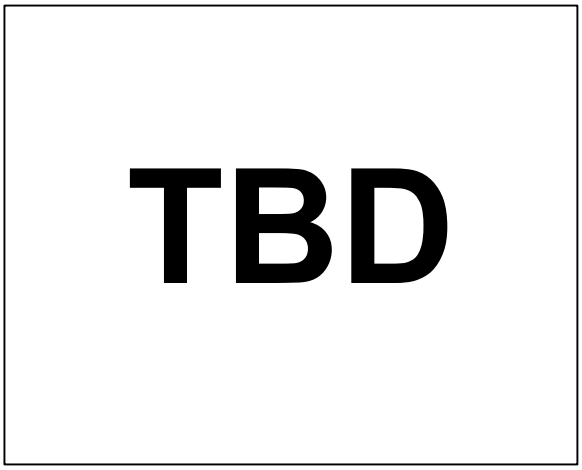


Figure 27. Peak-to-Peak Noise (100kHz Bandwidth)

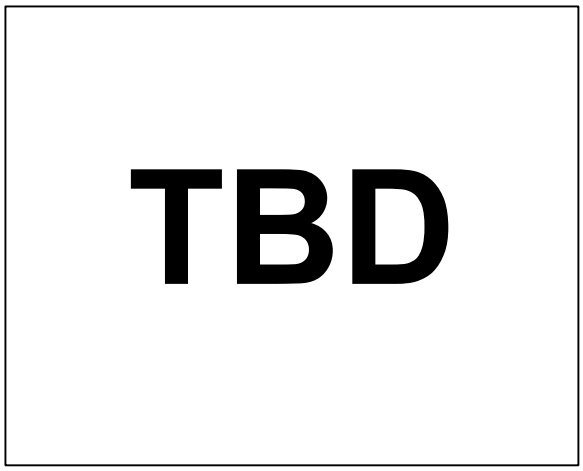


Figure 25. Digital-to-Analog Glitch Energy

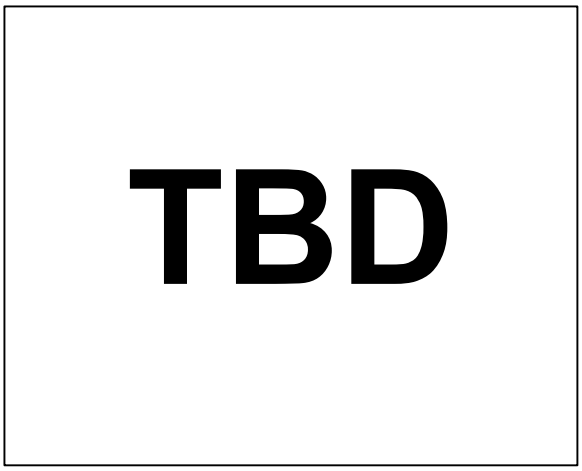


Figure 28. Output Voltage Settling Time

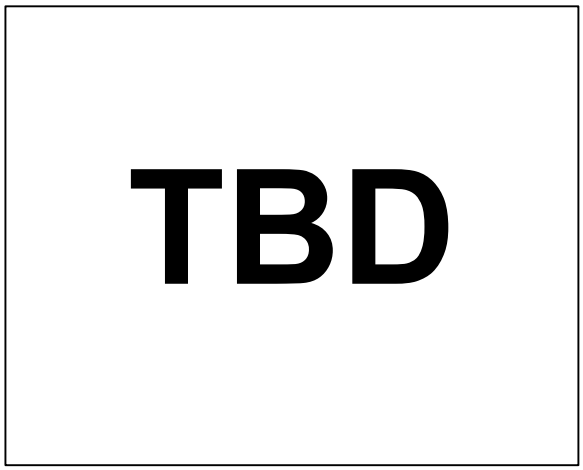


Figure 26. Peak-to-Peak Noise (0.1Hz to 10Hz Bandwidth)

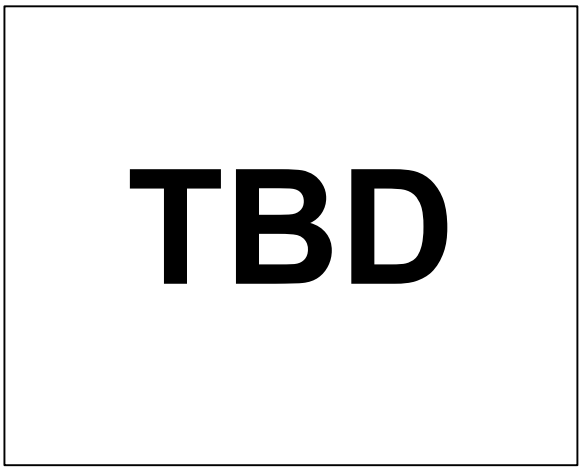


Figure 29. V_{OUT} vs. Time on Power-up

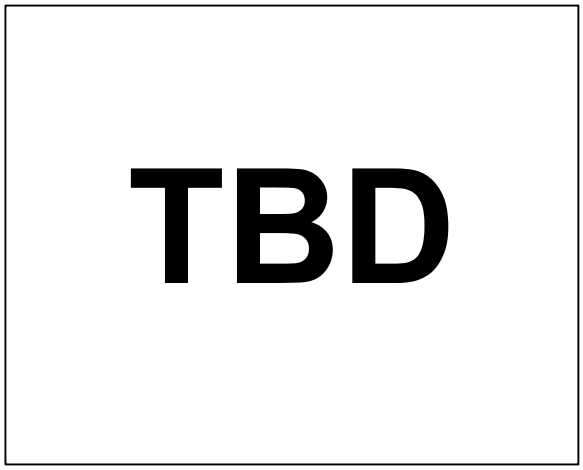


Figure 30. V_{OUT} vs, Time on Output Enabled

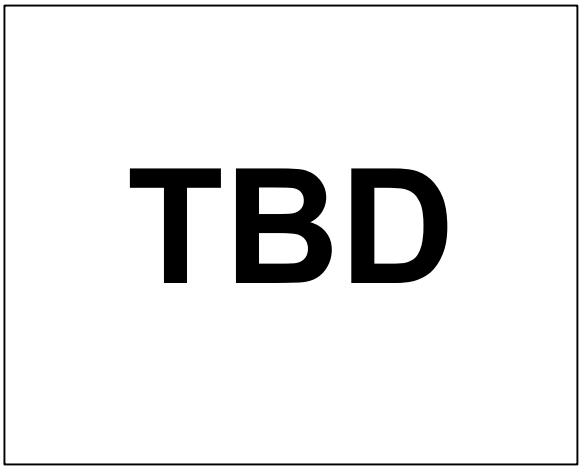


Figure 33. AI_{DD} vs AV_{DD}

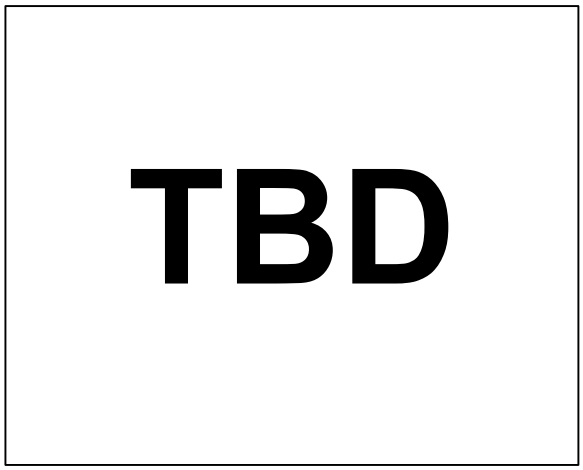


Figure 31. DI_{CC} vs.Logic Input Voltage

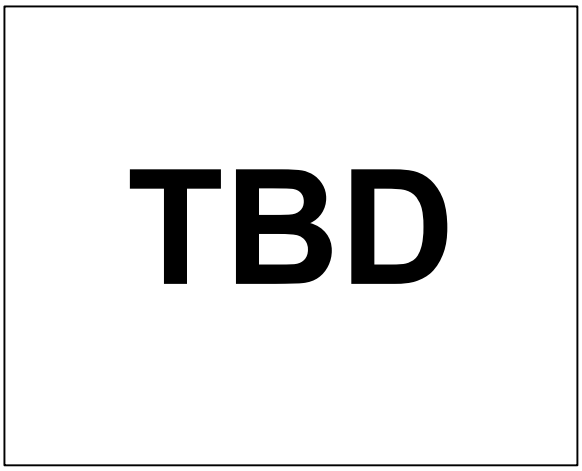


Figure 34. DV_{CC} Output Voltage vs. DI_{CC} Load Current

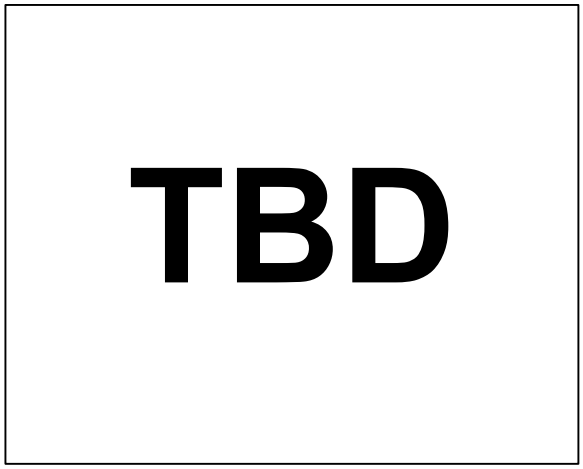


Figure 32. AI_{DD}/AI_{SS} vs AV_{DD}/AV_{SS}

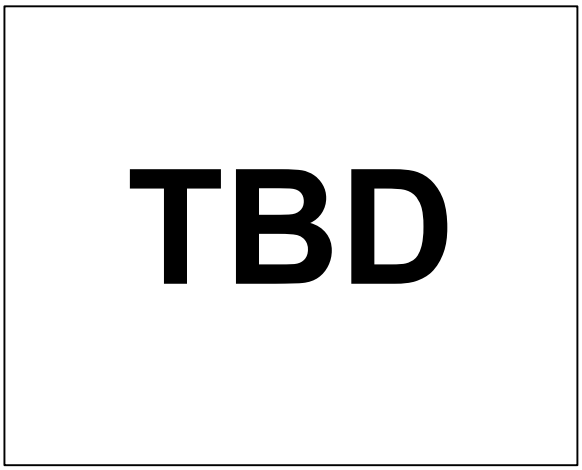


Figure 35. Refout Turn-on Transient

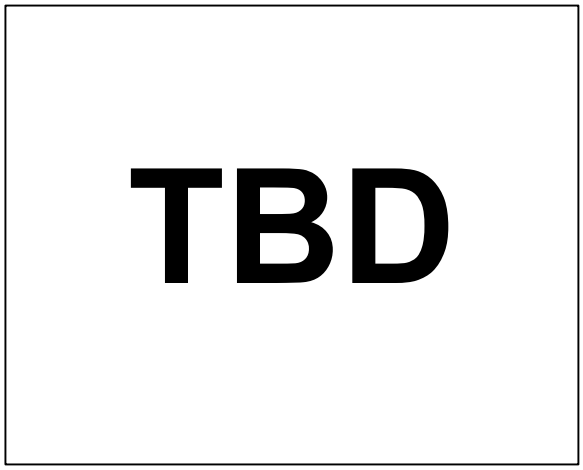


Figure 36. Refout Output Noise (0.1Hz to 10Hz Bandwidth)

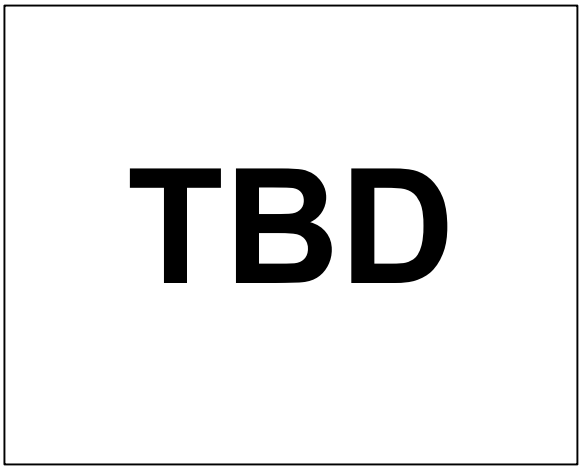


Figure 39. Refout Load Transient

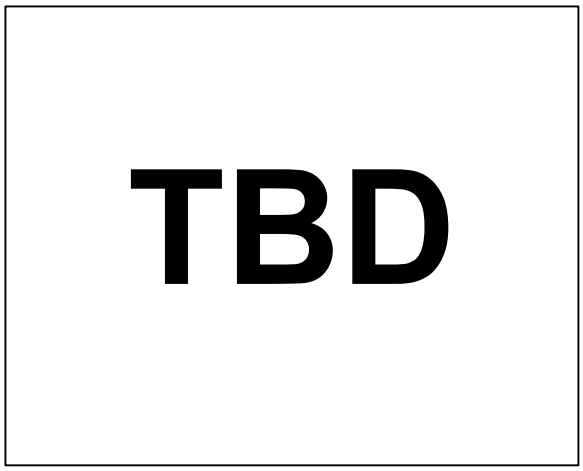


Figure 37. Refout Output Noise (100kHz Bandwidth)

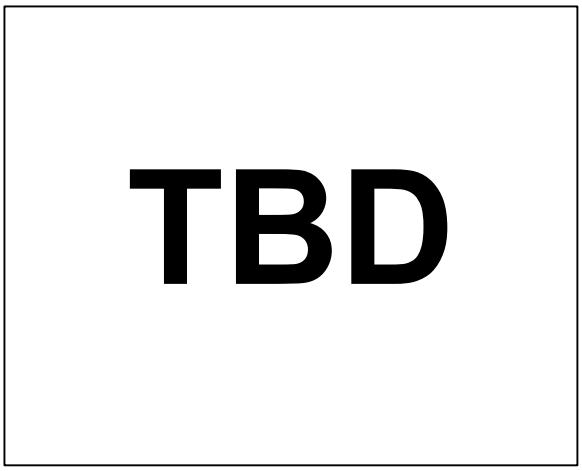


Figure 40. Refout Histogram of Thermal Hysteresis

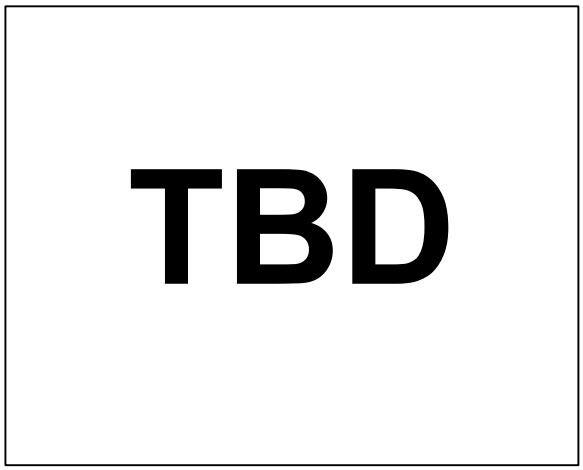


Figure 38. Refout Line Transient

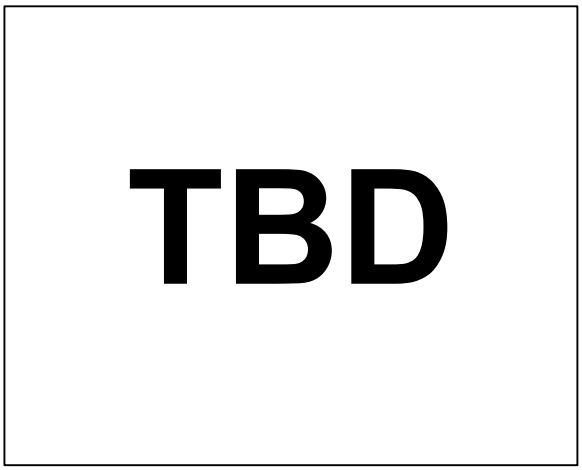


Figure 41. Refout Voltage vs. Load Current

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 6.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 9.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5502 is monotonic over the full operating temperature range.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 18.

Bipolar Zero Temperature Coefficient (TC)
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Full-Scale Error
Full-Scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale – 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

Negative Full-Scale Error/Zero-Scale Error
Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be negative full-scale – 1 LSB. A plot of zero-scale error vs. temperature can be seen in Table TBD

Zero-Scale TC
This is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. A plot of settling time can be seen in Figure 28

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/μs.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Table TBD

Gain TC
This is a measure of the change in gain error with changes in temperature. Gain Error TC is expressed in ppm FSR/°C.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5502 is powered-on. It is specified as the area of the glitch in nV-sec. See Table TBD

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 25

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Table TBD.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

Line Regulation

Line regulation is the change in reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

Thermal Hysteresis

Thermal hysteresis is the change of reference output voltage after the device is cycled through temperatures from +25°C to −40°C to +85°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle. See Table TBD for a histogram of thermal hysteresis.

$$V_{O\_HYS} = V_O(25°\text{C}) - V_{O\_TC}$$

$$V_{O\_HYS}(ppm) = \frac{V_O(25°\text{C}) - V_{O\_TC}}{V_O(25°\text{C})} \times 10^6$$

where:

$V_O(25°\text{C})$ = V_O at 25°C
V_{O_TC} = V_O at 25°C after temperature cycle

THEORY OF OPERATION

The AD5502 is a precision digital to analog voltage output converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost single-chip solution for generating unipolar and bipolar voltage outputs. The voltage output ranges, programmable via the serial interface, are; 0 to 5 V, 0 to 10 V, 0 to 40 V, ±5 V and ±10 V.

ARCHITECTURE

The DAC core architecture of the AD5502 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 42. The 4 MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects 1 of 15 matched resistors to either ground or the reference buffer output. The remaining 12 bits of the data-word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

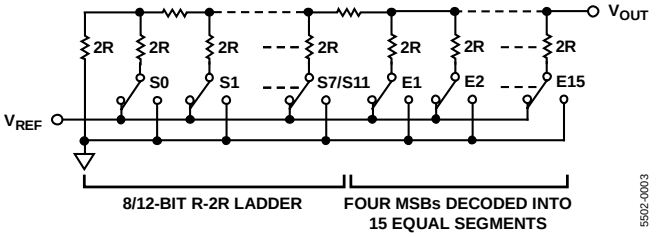


Figure 42. DAC Ladder Structure

The voltage output from the DAC core is buffered and scaled to output a software selectable unipolar or bipolar voltage range (See diagram, Figure 43).

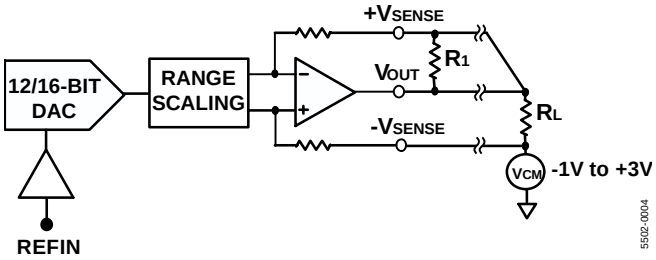


Figure 43. Voltage Output

Output Amplifier

The output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 2 kΩ in parallel with 1 µF to AGND. The source and sink capabilities of the output amplifier can be seen in Figure TBD. The slew rate is 1 V/µs with a full-scale settling time of 10 µs, (10 V step). Figure 43 shows the voltage output driving a load, R_L on top of a common mode voltage of up to −1 V to +3V.

In output module applications where a cable could possibly become disconnected from $+V_{SENSE}$ resulting in the amplifier loop being broken and causing V_{OUT} to output a voltage at the supply rails, a resistor, R_1, of value 2kΩ to 5kΩ should be included as shown to ensure the amplifier loop is kept closed.

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacitive loads of up to 1uF with the addition of a non-polarised 4nF compensation capacitor between the C_{COMP1} and C_{COMP2} pins. Without the compensation capacitor, up to 20nF capacitive loads can be driven.

Reference Buffers

The AD5502 can operate with either an external or internal reference. The reference input has an input range of 4 V to 5 V. This input voltage is then buffered before it is applied to the DAC.

SERIAL INTERFACE

The AD5502 is controlled by a versatile 4-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI®, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. The input register consists of 8 control bits and 16 data bits as shown in Table 6. Data is clocked into the input register on the rising edge of SCLK. On the rising edge of LATCH the data that is present in the input register is latched LATCH must remain high for at least 40ns before more data can be clocked into the input register. The timing diagram for this operation is shown in Figure 2.

Table 6. Input Shift Register Format

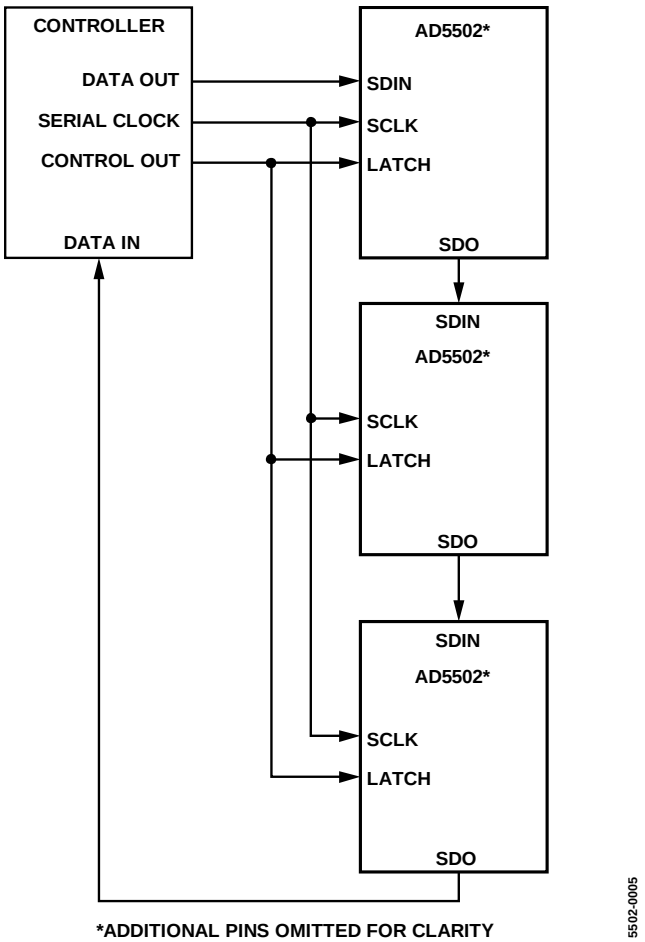
MSB																							LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDRESS WORD								Data WORD															

Table 7. Control Word Functions

Address Word	Function
00000000	No Operation (NOP)
00000001	Data Register
00000010	Readback register value as per Read Address (See Table 9)
01010101	Control Register
01010110	RESET Register

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of data bits have been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The first rising edge of SCLK that clocks in the MSB of the dataword marks the beginning ot the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24th rising SCLK edge, the data written is invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data is also invalid.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 44. Daisy Chaining the AD5502

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy chain several devices together as shown in Figure 44. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisychain mode is enabled by setting the DCEN bit of the Control register. The first rising edge of SCLK that clocks in the MSB of the dataword marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the falling edge of SCLK and is valid on the next rising edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × *N*, where *N* is the total number of AD5502 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. See Figure 4 for a timing diagram.

Readback Operation

Readback mode is invoked by setting the control word and read address as shown in Table 8 and Table 9 when writing to the input register. The next write to the AD5502 should be a NOP command which clocks out the data from the previously addressed register as shown in Figure 3.
By default the SDO pin is disabled, after having addressed the AD5502 for a read operation, a rising edge on LATCH enables the SDO pin in anticipation of data being clocked out, after the data has been clocked out on SDO, a rising edge on LATCH disables (three-states) the SDO pin once again.
To read back the data register for example, the following sequence should be implemented:

1. Write 0x020001 to the AD5502 input register. This configures the part for read mode with the data register selected.
2. Follow this with a second write, a NOP condition, 0x000000 During this write, the data from the register is clocked out on the SDO line.

Table 8. Input Shift Register Contents for a read operation

MSB																							LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Address	

Table 9. Read Address Decoding

Read Address	Function
00	Read Status Register
01	Read Data Register
10	Read Control Register

DEFAULT CONFIGURATION

On initial power-up of the AD5502 the power-on-reset circuit ensures that all registers are loaded with zero-code, as such the voltage output pin is in three-state. An alternative voltage output range may be selected via the Control register. To enable the output the OUTEN bit of the Control register must be set.

TRANSFER FUNCTION

For a unipolar voltage output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right]$$

For a bipolar voltage output range, the output voltage expression is given by

$$V_{OUT} = V_{REFIN} \times Gain\left[\frac{D}{2^N}\right] - \frac{Gain \times V_{REFIN}}{2}$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.
V_{REFIN} is the reference voltage applied at the REFIN pin.
Gain is an internal gain whose value depends on the output range selected by the user as shown in Table 10.

Table 10.

Output Range	Gain Value
+5 V	2
+10 V	4
+20V	8
±5 V	4
±10 V	8
+ 40 V	16

DATA REGISTER

The Data register is addressed by setting the control word of the input shift register to 0x01. The data to be written to the Data register is entered in positions D15 to D0 as shown in Table 11,

Table 11. Programming the Data Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data WORD															

CONTROL REGISTER

The Control register is addressed by setting the control word of the input shift register to 0x55. The data to be written to the Control register is entered in positions D15 to D0 as shown in Table 12. The Control register functions are shown in Table 13.

Table 12. Programming the Control Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CLRSEL	OVRRNG	0	OUTEN	0	0	0	0	0	0	0	0	DCEN	R2	R1	R0

Table 13. Control Register Functions

Option	Description
CLRSEL	See Table 19 for a description of the CLRSEL operation
OVRRNG	Setting this bit increases the voltage output range by 10%. Further details in Features section
OUTEN	Output enable. This bit is set to enable the output.
DCEN	Daisychain enable
R2,R1,R0	Output range select. See Table 14

Table 14. Output Range Options

R2	R1	R0	Output Range Selected
0	0	0	0 V to +5 V Voltage Range
0	0	1	0 V to +10 V Voltage Range
0	1	0	±5 V Voltage Range
0	1	1	±10 V Voltage Range
1	0	0	0 V to +40 V Voltage Range

RESET REGISTER

The Reset register is addressed by setting the control word of the input shift register to 0x56. The data to be written to the Reset register is entered in positions D15 to D0 as shown in Table 15. The RESET register options are shown in Table 15 and Table 16.

Table 15. Programming the Reset Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															RESET

Table 16. Reset register Functions

Option	Description
RESET	Setting this bit performs a reset operation, restoring the AD5502 to its initial power on state

STATUS REGISTER

The Status register is a read only register. The Status register functionality is described in Table 17 and Table 18.

Table 17. Decoding the Status Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															OVERTEMP

Table 18. Status Register Functions

Option	Description
OVERTEMP	This bit is set if the AD5502 core temperature exceeds approx. 150°C.

FEATURES

OVER TEMPERATURE ALERT

The AD5502 is equipped with an $\overline{\text{OVERTEMP}}$ pin, this is an open-drain output allowing several AD5502 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{OVERTEMP}}$ pin is forced active If the core temperature of the AD5502 exceeds approx. 150°C. The OVERTEMP bit of the Status register also alerts the user to an over temperature situation.

VOLTAGE OUTPUT SHORT CIRCUIT PROTECTION

Under normal operation the voltage output can sink/source 5mA and maintain specified operation. The maximum current that the voltage output can deliver is 10mA, this is the short circuit current.

ASYNCHRONOUS CLR (CLR)

CLR is an active high CLR that allows the voltage output to be CLRed to either zero-scale code or mid-scale code, user-selectable via the CLR SELECT pin or the CLRSEL bit of the Control register as described in Table 19. (The CLR select feature is a logical OR function of the CLR SELECT pin and the CLRSEL bit). It is necessary to maintain CLR high for a minimum amount of time (see Figure 2) to complete the operation. When the CLR signal is returned low, the output remains at the CLRed value until a new value is programmed. A CLR operation can also be performed via the CLR command in the control register.

.

Table 19. CLR SELECT Options

CLR SELECT	Output CLR Value	
	Unipolar Output Range	**Bipolar Output Range**
0	0 V	0 V
1	Mid-Scale	Negative Full-Scale

INTERNAL REFERENCE

The AD5502 contains an integrated +5V voltage reference with initial accuracy of ±2mV max and a temperature drift coefficient of ±10 ppm max. The reference voltage is buffered and externally available for use elsewhere within the system. See Figure 41 for a load regulation graph of the Integrated reference.

VOLTAGE OUTPUT OVER-RANGE

An over-range facility is provided on the voltage output. When enabled via the Control register, the selected output range is over-ranged by 10%.

DIGITAL POWER SUPPLY

By default the DV_{CC} pin accepts a power supply of 2.7V to 5.5V, alternatively, via the DV_{CC} SELECT pin an internal 4.5V power supply may be output on the DV_{CC} pin for use as a digital power supply for other devices in the system or as a termination for pull-up resistors. This facility offers the advantage of not having to bring a digital supply across an isolation barrier. The internal power supply is enabled by leaving the DV_{CC} SELECT pin unconnected. To disable the internal supply, DV_{CC} SELECT should be tied to 0V

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5502 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5502 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5502 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5502 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. The *i*Coupler® family of products from Analog Devices provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5502 make it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 45 shows a 4-channel isolated interface to the AD5502 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

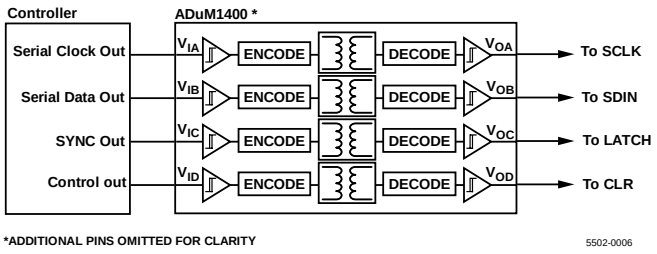


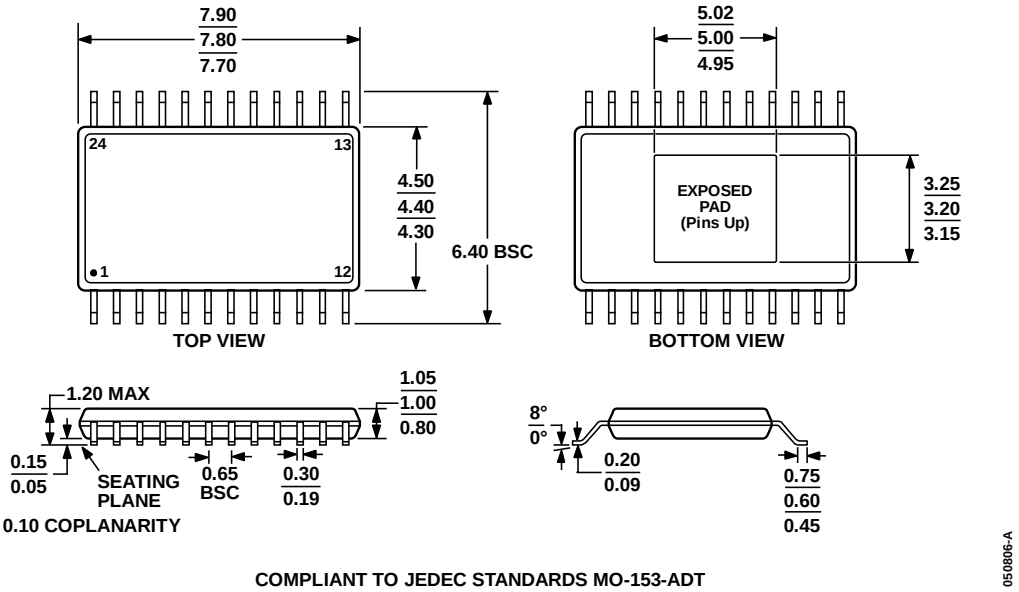
Figure 45. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5502 is via a serial bus that uses protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a latch signal. The AD5502 require a 24-bit data-word with data valid on the rising edge of SCLK.

For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-ADT

Figure 46. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-24)
Dimensions shown in millimeters

NOTES

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