High Speed, Precision Sample-and-Hold Amplifier

AD585

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD585

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD585-703Q	High Speed, Precision Sample-and-Hold Amplifier
AD585-713Q	Radiation Tested, High Speed, Precision Sample-and-Hold Amplifier
AD585-703M	High Speed, Precision Sample-and-Hold Amplifier
AD585-713M	Radiation Tested, High Speed, Precision Sample-and-Hold Amplifier

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)
M	GDFP1-F14	14-Lead ceramic flat pack (CERPAK)

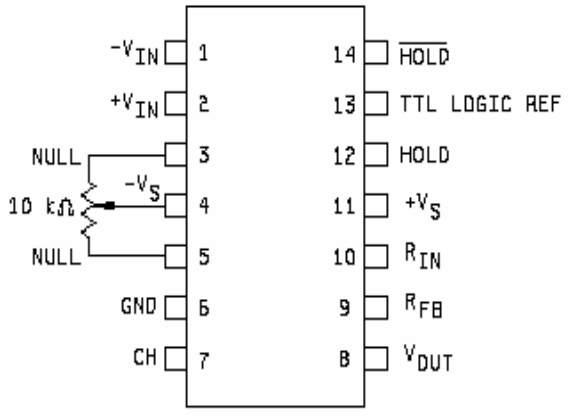

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. 1/

Supply voltage.....±18V
Logic inputs.....$\pm V_S$
Analog inputs.....$\pm V_S$
R_{IN}, R_{FB} pins.....$\pm V_S$
Output short circuit to ground.....Indefinite
TTL logic reference short circuit to ground.....Indefinite
Storage temperature range.....-65°C to +150°C
Ambient operating temperature range (T_A).....-55°C to +125°C
Junction Temperature (T_J).....+150°C
Lead temperature (soldering, 10 seconds).....+300°C

1/ Unless otherwise specified, all voltages are referenced to ground.

3.1 Recommended operating conditions.

Supply voltage range:

$+V_S$.....+5V to +18V dc
$-V_S$.....-12V dc to -18V dc

3.2 Thermal Characteristics:

Thermal Resistance, cerdip (Q) Package
Junction-to-Case (Θ_{JC}) = 28°C/W Max
Junction-to-Ambient (Θ_{JA}) = 110°C/W Max
Thermal Resistance, cerpak (M) Package
Junction-to-Case (Θ_{JC}) = 60°C/W Max
Junction-to-Ambient (Θ_{JA}) = 140°C/W Max

4.0 Electrical Table:

Table I						
Parameter See notes at end of table	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
Offset voltage	V_{OS}	VOUT = 0V	1, 2, 3	-3	3	mV
			4	-2	2	
Bias current	I_B	VIN = 0V	1	-2	2	nA
			2	-50	50	
TTL reference output	V_{LREF}	50 µA load	1	1.2	1.6	V
			2, 3	0.8	1.9	
Logic input high voltage	V_{IH}	Hold = V_{LREF}	1	2.0		
			2, 3	2.0		
Logic input low voltage 2/	V_{IL}	Hold = V_{LREF}	1		0.8	
			2, 3		0.7	
Logic input current	I_{IL}	VS = ±18V	1, 2, 3		50	µA
Supply current	I_{SS}	RL = infinite	1, 2, 3		10	mA
Power supply rejection	PSRR	+VS = +5V to +18V -VS = -12V to -18V VIN = VOUT = 0V	1	70		dB
Acquisition time	Tacq	10V step to 0.01%	7		3	µS
		20V step to 0.01% 3/			5	
Droop rate 2/ 4/	V_{DRP}	V_{IN} = 0V	4		1	mV/mS
Sample to hold offset 2/	SH_{OS}	V_{IN} = 0V	4		3	mV
Application resistor mismatch	ΔRM		1, 2, 3		0.3	%
Common mode rejection	CMRR	V_{CM} = ±10V	1	80		dB
			2, 3	77		
Slew current 5/	I_{SL}		4	850		µA
			2, 3	600		
Output resistance	R_{OUT}	I_{OUT} = ±10mA	1		0.05	Ω
			2, 3		0.10	
Output current	I_{OUT}	RL = 100Ω	1	12		mA

TABLE I NOTES:

1/ V_S = ±15 V, C_H = Internal, R_L = Infinite, A = +1, Hold active, sample mode unless otherwise noted.
2/ Tested in hold mode.
3/ Guaranteed if not tested to the limits specified.
4/ Doubles every 10°C.
5/ V_{OUT} = 20 Vp-p. Slew rate = slew current/C_H.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 7
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. Deltas excluded from PDA

2/ See table III for delta limits.

4.2 Table III. Burn-in test delta limits.

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
SHOS	±3	±3	mV

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition D.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	June 5, 2000
B	Update web address. Paragraph 5.2, change BI condition from B to D. Delete subgroups 5 & 6 from Table II (they are not on Table I) Add subgroup 7 to group A requirements on Table II.	Feb. 14, 2002
C	Update web address. Remove burn-in and radiation bias circuits	16-May-03
D	Add AD585-703M and AD585-713M.	4-April-05
E	Update header/footer & add to 1.0 scope description.	Feb. 21, 2008
F	Add Junction Temperature (T_J)…..+150°C to 3.0 Absolute Maximum Ratings	March 31, 2008