

FEATURES

Throughput: 10 MSPS

SNR: 93dB

INL: ± 0.5 LSB typical, ± 1 LSB maximum

DNL: ± 0.3 LSB typical, ± 0.5 LSB maximum

Power dissipation: 140 mW

32-lead LFCSP (5 mm \times 5 mm)

SAR architecture

No latency/no pipeline delay

16-bit resolution with no missing codes

Zero error: ± 1.5 LSB

Differential input range: ± 4.096 V

Serial LVDS interface

Self-clocked mode

Echoed-clock mode

LVDS or CMOS option for conversion control (CNV signal)

Reference options

Internal: 4.096 V

External (1.2 V) buffered to 4.096 V

External: 4.096 V

APPLICATIONS

High dynamic range telecommunications

Receivers

Digital imaging systems

Digital X-RAY

Digital MRI

IR Cameras

High speed data acquisition

Spectrum analysis

Test equipment

FUNCTIONAL BLOCK DIAGRAM

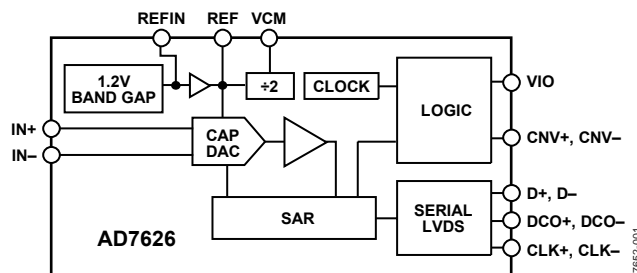


Figure 1.

GENERAL DESCRIPTION

The AD7626 is a 16-bit, 10 MSPS, charge redistribution successive approximation register (SAR) based architecture analog-to-digital converter (ADC). SAR architecture allows unmatched performance both in noise (92 dB SNR) and in linearity (1 LSB). The AD7626 contains a high speed, 16-bit sampling ADC, an internal conversion clock, and an internal buffered reference. On the CNV edge, it samples the voltage difference between the IN+ and IN- pins. The voltages on these pins swing in opposite phase between 0 V and REF. The 4.096 V reference voltage, REF, can be generated internally or applied externally.

All converted results are available on a single LVDS self-clocked or echoed-clock serial interface, reducing external hardware connections.

The AD7626 is housed in a 32-lead, 5 mm \times 5 mm LFCSP with operation specified from -40°C to $+85^{\circ}\text{C}$.

Table 1. Fast PuLSAR[®] ADC Selection

Input Type	Resolution (Bits)	1 MSPS to <2 MSPS	2 MSPS to 3 MSPS	6 MSPS	10 MSPS
Differential (Ground Sense)	16	AD7653 AD7667 AD7980 AD7983			
True Bipolar	16	AD7671			
Differential (Antiphase)	16	AD7677 AD7623	AD7621 AD7622 AD7641	AD7625	AD7626
Differential (Antiphase)	18	AD7643 AD7982 AD7984			

Rev. PrE

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REVISION HISTORY

SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.5 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	V _{IN+} – V _{IN–}	–V _{REF}		+V _{REF}	V
Operating Input Voltage	V _{IN+} , V _{IN–} to AGND	–0.1		V _{REF} + 0.1	V
Common-Mode Input Range		V _{REF} /2 – 0.05	V _{REF} /2	V _{REF} /2 + 0.05	V
CMRR	f _{IN} = 1 MHz		60		dB
Input Current	Midscale input		77		μA
THROUGHPUT					
Complete Cycle				100	ns
Throughput Rate		0.1		10	MSPS
DC ACCURACY					
Integral Linearity Error		–1	±0.45	+1	LSB
No Missing Codes		16			Bits
Differential Linearity Error		–0.5	±0.3	+0.5	LSB
Transition Noise			0.6		LSB
Zero Error, T _{MIN} to T _{MAX}		–4	±1.5	+4	LSB
Zero Error Drift			0.5		ppm/°C
Gain Error, T _{MIN} to T _{MAX}			8	20	LSB
Gain Error Drift			0.4		ppm/°C
Power Supply Sensitivity ¹	VDD1 = 5 V ± 5%		0.4		LSB
	VDD2 = 2.5 V ± 5%		0.2		LSB
AC ACCURACY					
External Reference	f _{IN} = 20 kHz				
Dynamic Range		92.5	93.2		dB
Signal-to-Noise Ratio		92	93		dB
Spurious-Free Dynamic Range			106		dB
Total Harmonic Distortion			–105.5		dB
Signal-to-(Noise + Distortion)		91.5	92		dB
Internal Reference	f _{IN} = 20 kHz				
Dynamic Range		92.5	93.2		dB
Signal-to-Noise Ratio		91.5	92.9		dB
Spurious-Free Dynamic Range			106		dB
Total Harmonic Distortion			–105.5		dB
Signal-to-(Noise + Distortion)		91	92.5		dB
–3 dB Input Bandwidth			100		MHz
Aperture Jitter			0.25		ps rms
Aperture Delay					ps rms
INTERNAL REFERENCE					
Output Voltage	REFIN @ 25°C		1.2		V
Temperature Drift	–40°C to +85°C		±15		ppm/°C
REFERENCE BUFFER					
REFIN Input Voltage Range			1.2		V
REF Output Voltage Range		4.076	4.096	4.116	V
Line Regulation	VDD1 ± 5%, VDD2 ± 5%		5		mV
EXTERNAL REFERENCE					
Voltage Range	REF		4.096		V
VCM PIN	@ 25°C				
Output Voltage			REF/2		V
Output Impedance		4	5	6	kΩ

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LVDS I/O (ANSI-644)					
Data Format		Serial LVDS twos complement			
Differential Output Voltage, V_{OD}	$R_L = 100\ \Omega$	270	350	454	mV
Common-Mode Output Voltage, V_{OCM}	$R_L = 100\ \Omega$	1120 ²	1250	1375	mV
Differential Input Voltage, V_{ID}		100		650	mV
Common-Mode Input Voltage, V_{ICM}		800		1575	mV
POWER SUPPLIES					
Specified Performance					
VDD1		4.75	5	5.25	V
VDD2		2.37	2.5	2.63	V
VIO		2.37	2.5	2.63	V
Operating Currents					
Static—Not Converting					
VDD1			5		mA
VDD2			20		mA
VIO	Self-clocked mode and echoed-clock mode		15		mA
With Internal Reference	10 MSPS throughput				
VDD1			10		mA
VDD2			25		mA
VIO	Echoed-clock mode		18		mA
	Self-clocked mode		14		
Without Internal Reference	10 MSPS throughput				
VDD1			9		mA
VDD2			21		mA
VIO	Echoed-clock mode		18		mA
	Self-clocked mode		14		
Power Dissipation ³					
Static—Not Converting			100		mW
With Internal Reference	10 MSPS throughput		140		mW
Without Internal Reference	10 MSPS throughput		120		mW
Energy per Conversion	10 MSPS throughput		14		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

¹ Using an external reference.

² The ANSI-644 LVDS specification has a minimum output common mode (V_{OCM}) of 1125 mV.

³ Power dissipation is for the AD7626 device only. In self-clocked interface mode, 9 mW is dissipated in the 100 Ω terminator. In echoed-clock interface mode, 18 mW is dissipated in two 100 Ω terminators.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.37 V to 2.63 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions ¹	t _{CYC}	100		10000	ns
Acquisition Time	t _{ACQ}	40			ns
CNV High Time	t _{CNVH}	10		40	ns
CNV to D (MSB) Delay	t _{MSB}			100	ns
CNV to Last CLK (LSB) Delay	t _{CLKL}			70	ns
CLK Period ²	t _{CLK}	(t _{CYC} - t _{MSB} + t _{CLKL})/n	4	3.33	ns
CLK Frequency	f _{CLK}		250	300	MHz
CLK to DCO Delay (Echoed-Clock Mode)	t _{DCO}	0	4	7	ns
DCO to D Delay (Echoed-Clock Mode)	t _D		0	1	ns
CLK to D Delay	t _{CLKD}	0	4	7	ns

¹ The maximum time between conversions is 10,000 ns. If CNV± is left idle for a time greater than the maximum value of t_{CYC}, the subsequent conversion result is invalid.

² For the minimum CLK period, the window available to read data is t_{CYC} - t_{MSB} + t_{CLKL}. Divide this time by the number of bits (n) that are read. In echoed-clock interface mode, n = 16; in self-clocked interface mode, n = 18.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs IN+, IN– to GND ¹	–0.3 V to REF + 0.3 V or ±130 mA
REF ² to GND	–0.3 V to +6 V
VCM, CAP2 to GND	–0.3 V to +6 V
CAP1, REFIN to GND	–0.3 V to +2.7 V
Supply Voltage	
VDD1	–0.3 V to +6 V
VDD2, VIO	–0.3 V to +3 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Input Current to Any Pin Except Supplies ³	±10 mA
Operating Temperature Range (Commercial)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
ESD	1 kV

¹ See the Analog Inputs section.² Keep CNV+/CNV– low for any external REF voltage > 4.3 V applied to the REF pin.³ Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

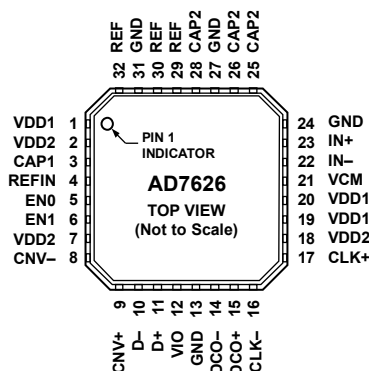
Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_VQ	40	4	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT THE EXPOSED PAD TO THE GROUND PLANE OF THE PCB USING MULTIPLE VIAS.

07662-002

Figure 2.

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type ¹	Description
1	VDD1	P	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
2	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor. The 2.5 V supply source should supply this pin first, then be traced to the other VDD2 pins (Pin 7 and Pin 18).
3	CAP1	AO	Connect this pin to a 10 nF capacitor.
4	REFIN	AI/O	Prebuffer Reference Voltage. When using the internal reference, this pin outputs the band gap voltage and is nominally at 1.2 V. It can be overdriven with an external reference voltage such as the ADR280 . In either internal or external reference mode, a 10 μ F capacitor is required. If using an external 4.096 V reference (connected to REF), this pin is a no connect and does not require any capacitor.
5, 6	EN0, EN1	DI	Enable Pins. The logic levels of these pins set the operation of the device as follows: EN1 = 0, EN0 = 0: Power Down Mode. EN1 = 0, EN0 = 1: External 1.2 V reference applied to REFIN pin is required. EN1 = 1, EN0 = 0: External 4.096 V reference applied to REF pin required. EN1 = 1, EN0 = 1: Internal reference and internal reference buffer in use.
7	VDD2	P	Digital 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
8, 9	CNV–, CNV+	DI	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV– is grounded; otherwise, CNV+ and CNV– are differential LVDS inputs.
10, 11	D–, D+	DO	LVDS Data Outputs. The conversion data is output serially on these pins.
12	VIO	P	Input/Output Interface Supply. Use a 2.5 V supply and decouple this pin with a 100 nF capacitor.
13	GND	P	Ground. Return path for the 100 nF capacitor connected to Pin 12.
14, 15	DCO–, DCO+	DO	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self-clocked interface mode is selected. In this mode, the 16-bit results on D are preceded by a 2-bit header (10) to allow synchronization of the data by the digital host with simple logic. When DCO+ is not grounded, the echoed-clock interface mode is selected. In this mode, DCO \pm is a copy of CLK \pm . The data bits are output on the falling edge of DCO+ and can be latched in the digital host on the next rising edge of DCO+.
16, 17	CLK–, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
18	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
19, 20	VDD1	P	Analog 5 V Supply. Isolate these pins from Pin 1 with a ferrite bead and decouple them with a 100 nF capacitor.
21	VCM	AO	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
22	IN–	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN–.
24	GND	P	Ground.

Pin No.	Mnemonic	Type ¹	Description
25, 26, 28	CAP2	AO	Connect all three CAP2 pins together and decouple them with the shortest trace possible to a single 10 μ F, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 27 (GND).
27	GND	P	Ground. Return path for the 10 μ F capacitor connected to Pin 25, Pin 26, and Pin 28.
29, 30, 32	REF	AI/O	Buffered Reference Voltage. When using the internal reference or the 1.2 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference, such as the ADR434 or the ADR444 , the internal reference buffer must be disabled. In either case, connect all three REF pins together and decouple them with the shortest trace possible to a single 10 μ F, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 31 (GND).
31	GND	P	Ground. Return path for the 10 μ F capacitor connected to Pin 29, Pin 30, and Pin 32.
EP	Exposed Pad		The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias. See the Exposed Paddle section for more information.

¹ AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

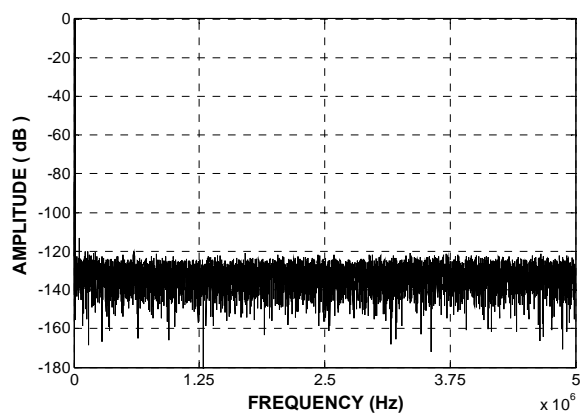


Figure 3. FFT, 10kHz, -0.5dB Input Tone, Wide View,
External Reference and Reference Buffer

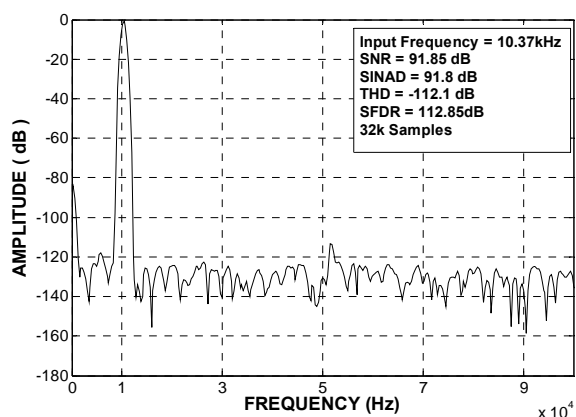


Figure 6. FFT, 10kHz, -0.5dB Input Tone Zoom In,
External Reference and Reference Buffer

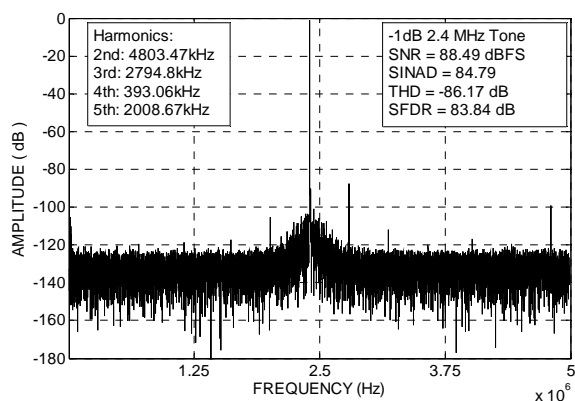


Figure 4 FFT, 2.4 MHz, -0.1dB Input Tone, Wide View

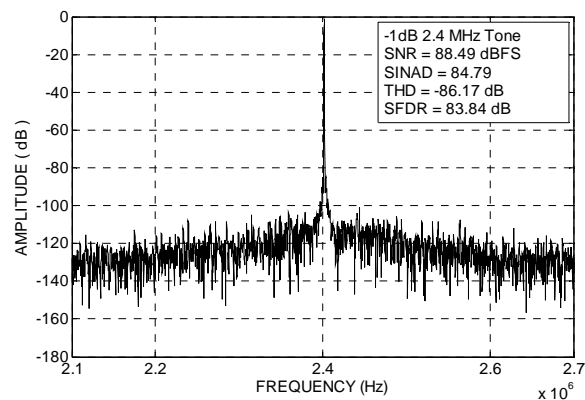


Figure 7. FFT, 2.4 MHz, -0.1dB Input Tone Zoom In,

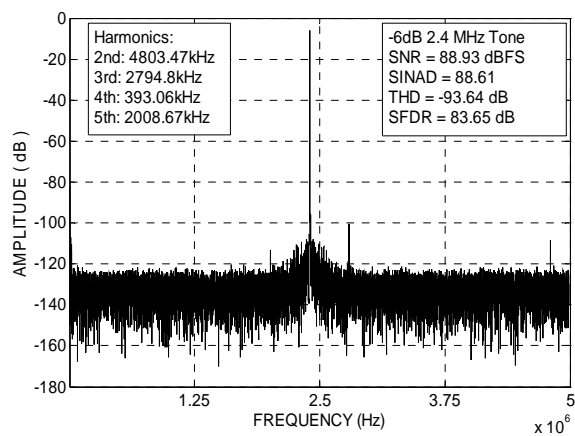


Figure 5. FFT, 2.4 MHz, -6dB Input Tone, Wide View

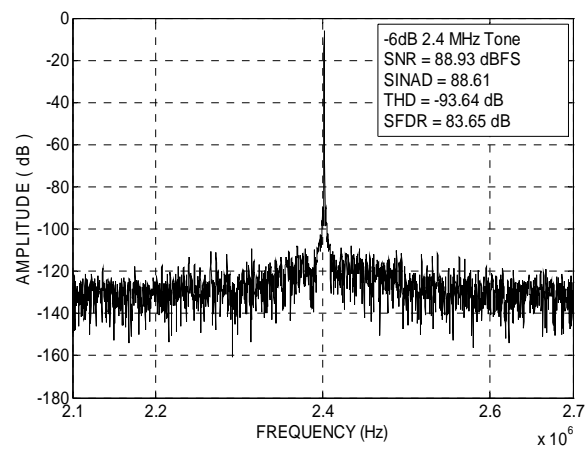


Figure 8. FFT, 2.4 MHz, -6dB Input Tone Zoom In

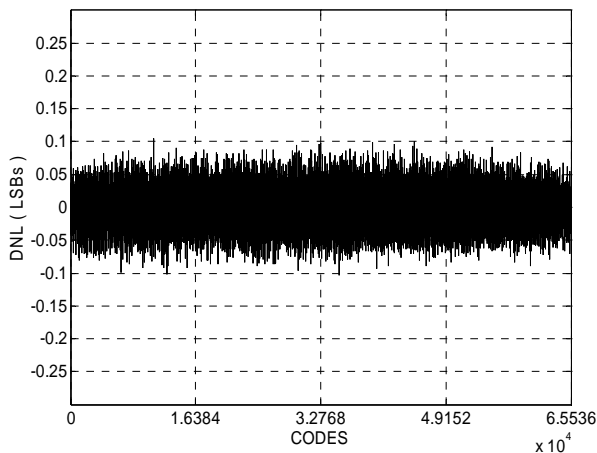


Figure 9 Differential Nonlinearity vs. Code
(Internal Reference and Reference Buffer)

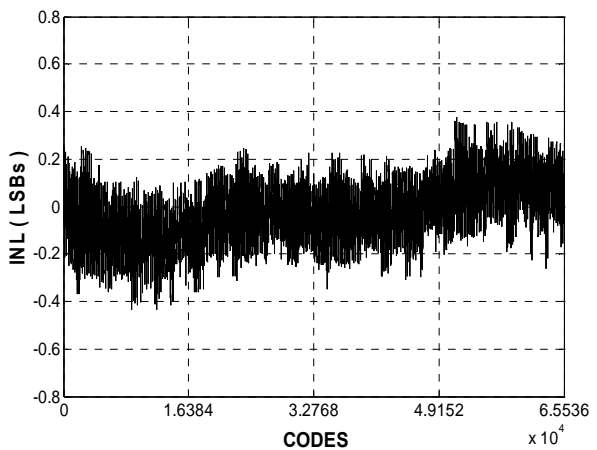


Figure 12 Integral Nonlinearity vs. Code
(Internal Reference and Reference Buffer)

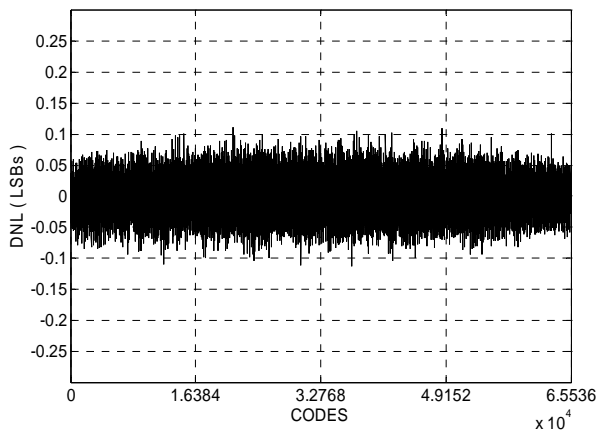


Figure 10 Differential Nonlinearity vs. Code
(External Reference and Reference Buffer)

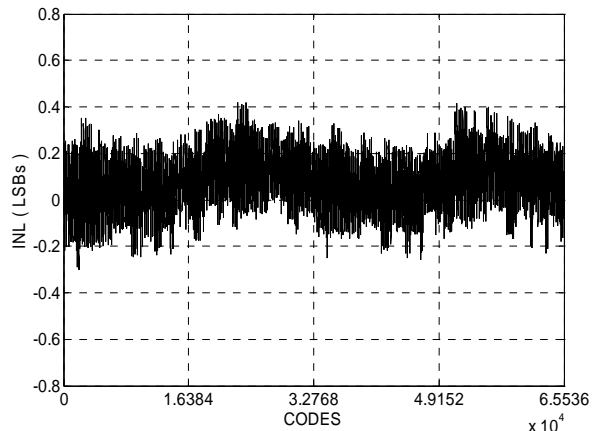


Figure 13 Integral Nonlinearity vs. Code
(External Reference and Reference Buffer)

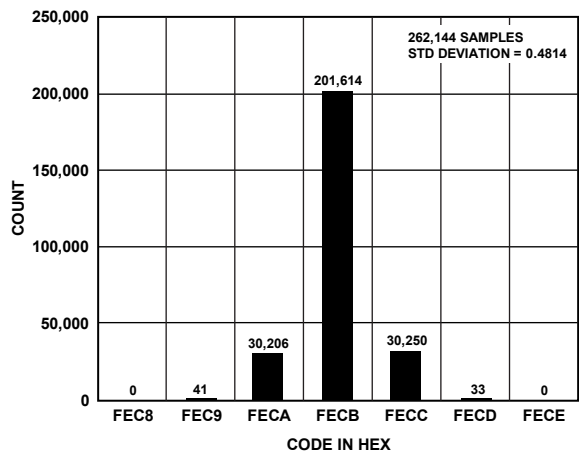


Figure 11 Histogram of 262,144 Conversions of a DC Input
at the Code Center (External Reference)

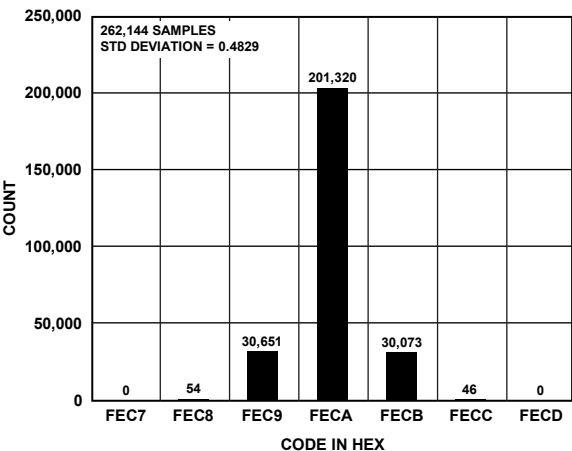


Figure 14 Histogram of 262,144 Conversions of a DC Input
at the Code Center (Internal Reference)

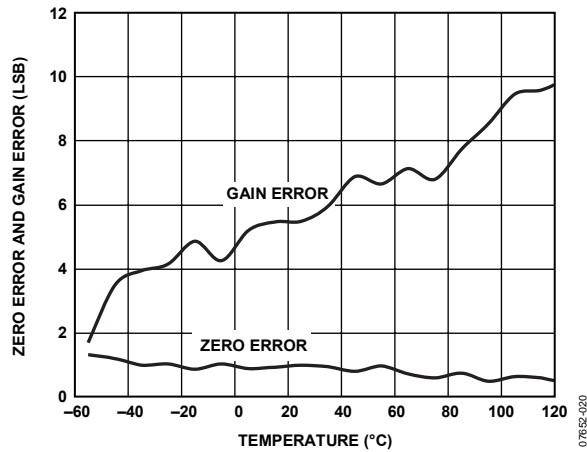


Figure 15 Zero Error and Gain Error vs. Temperature

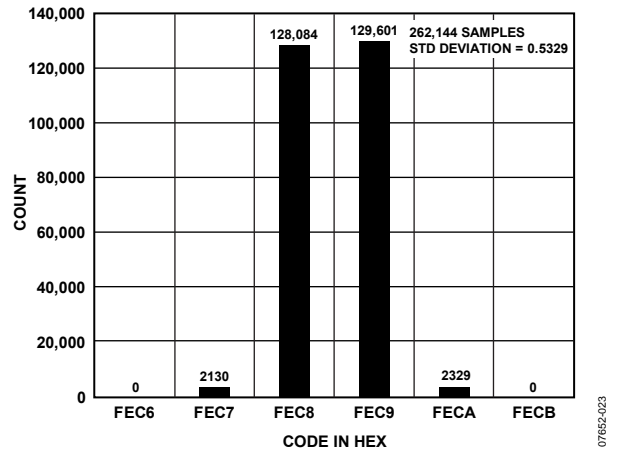


Figure 18 Histogram of 262,144 Conversions of a DC Input at the Code Transition (Internal Reference)

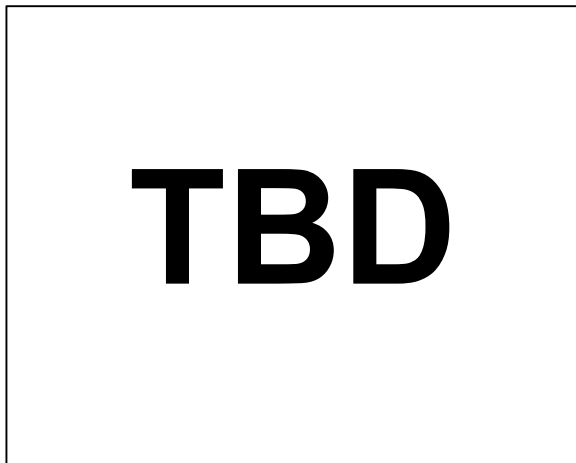


Figure 16

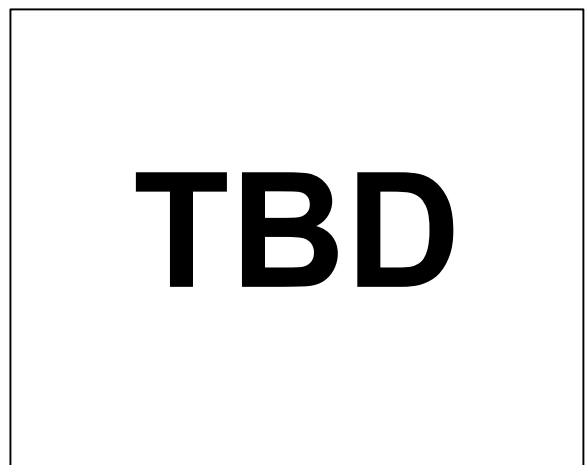


Figure 19

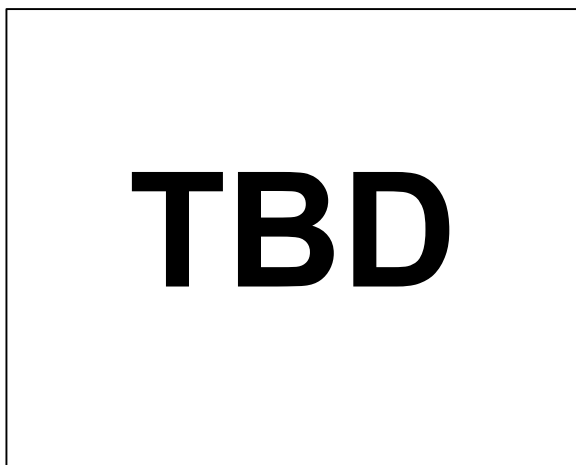


Figure 17

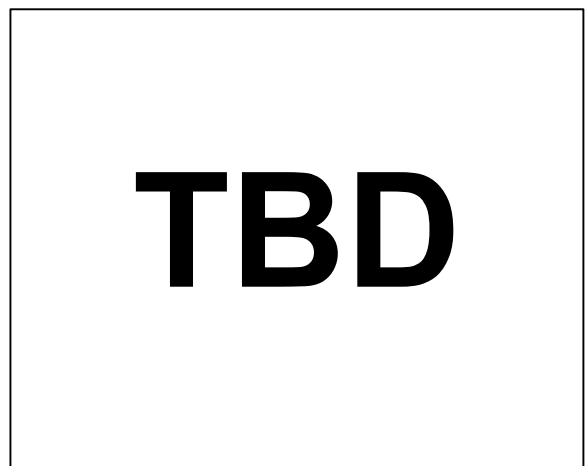


Figure 20

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of an 80 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} at frequency f_s .

$$CMRR \text{ (dB)} = 10\log(P_f/P_{f_s})$$

where:

P_f is the power at frequency f in the ADC output.

P_{f_s} is the power at frequency f_s in the ADC output.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs $\frac{1}{2}$ LSB before the first code transition. Positive full scale is defined as a level $1\frac{1}{2}$ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at -60 dB. The value for dynamic range is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

Gain Error

The first transition (from 100 ... 000 to 100 ... 001) should occur at a level $\frac{1}{2}$ LSB above nominal negative full scale (-4.0959375 V for the ± 4.096 V range). The last transition (from 011 ... 110 to 011 ... 111) should occur for an analog voltage $1\frac{1}{2}$ LSB below the nominal full scale ($+4.0959375$ V for the ± 4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB \text{ (V)} = \frac{V_{INp-p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Reference Voltage Temperature Coefficient

The reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN} , $T(25^\circ\text{C})$, and T_{MAX} . It is expressed in ppm/ $^\circ\text{C}$ as

$$TCV_{REF} \text{ (ppm}/^\circ\text{C)} = \frac{V_{REF} \text{ (Max)} - V_{REF} \text{ (Min)}}{V_{REF} \text{ (25}^\circ\text{C)} \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF} \text{ (Max)}$ = maximum V_{REF} at T_{MIN} , $T(25^\circ\text{C})$, or T_{MAX} .

$V_{REF} \text{ (Min)}$ = minimum V_{REF} at T_{MIN} , $T(25^\circ\text{C})$, or T_{MAX} .

$V_{REF} \text{ (25}^\circ\text{C)}$ = V_{REF} at 25°C .

T_{MAX} = $+85^\circ\text{C}$.

T_{MIN} = -40°C .

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error

Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

THEORY OF OPERATION

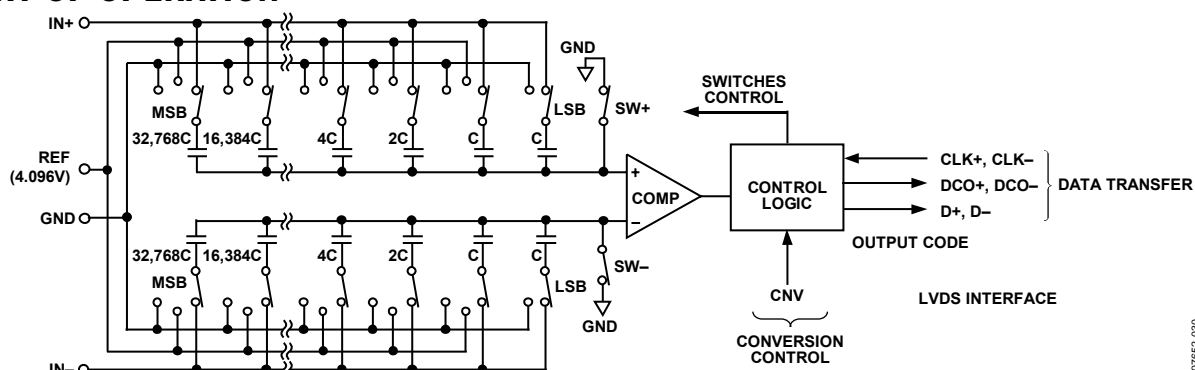


Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7626 is a 10 MSPS, high precision, power efficient, 16-bit ADC that uses SAR based architecture to provide performance of 93 dB SNR, ± 0.45 LSB INL, and ± 0.3 LSB DNL.

The AD7626 is capable of converting 10,000,000 samples per second (10 MSPS). The device typically consumes 140 mW. The AD7626 offers the added functionality of a high performance on-chip reference and on-chip reference buffer.

The AD7626 is specified for use with 5 V and 2.5 V supplies (VDD1, VDD2). The interface from the digital host to the AD7626 uses 2.5 V logic only. The AD7626 uses an LVDS interface to transfer data conversions. The CNV+ and CNV- inputs to the part activate the conversion of the analog input. The CNV+ and CNV- pins can be applied using a CMOS or LVDS source.

The AD7626 is housed in a space-saving, 32-lead, 5 mm \times 5 mm LFCSP.

CONVERTER INFORMATION

The AD7626 is a 10 MSPS ADC that uses SAR based architecture incorporating a charge redistribution DAC. Figure 21 shows a simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW-. All independent switches are connected to the analog inputs. In this way, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN- inputs. A conversion phase is initiated when the acquisition phase is complete and the CNV input goes high. Note that the AD7626 can receive a CMOS or LVDS format CNV signal.

When the conversion phase begins, SW+ and SW- are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs (IN+ and IN-) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and 4.096 V (the reference voltage), the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$... $V_{REF}/65536$). The control logic toggles these switches, MSB first, to bring the comparator back into a balanced condition. At the completion of this process, the control logic generates the ADC output code.

The AD7626 digital interface uses Low Voltage Differential Signaling (LVDS) to enable high data transfer rates.

The AD7626 conversion result is available for reading after t_{MSB} (time from the conversion start until MSB is available) has elapsed. The user must apply a burst LVDS CLK \pm signal to the AD7626 to transfer data to the digital host.

The CLK \pm signal outputs the ADC conversion result onto the data output D \pm . The bursting of the CLK \pm signal is illustrated in Figure 32 and Figure 33 and is characterized as follows:

The differential voltage on CLK \pm should be held to create logic low in the time between t_{CLKL} and t_{MSB} .

The AD7626 has two data read modes. For more information about the echoed-clock and self-clocked interface modes, see the Digital Interface section.

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TRANSFER FUNCTIONS

The AD7626 uses a 4.096 V reference. The AD7626 converts the differential voltage of the antiphase analog inputs (IN+ and IN-) into a digital output. The analog inputs, IN+ and IN-, require a 2.048 V common-mode voltage (REF/2).

The 16-bit conversion result is in MSB first, twos complement format.

The ideal transfer functions for the AD7626 are shown in Figure 22 and Table 7.

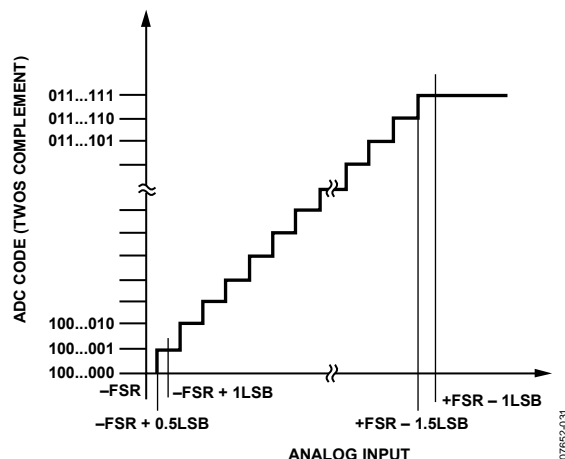


Figure 22. ADC Ideal Transfer Functions (FSR = Full-Scale Range)

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ - IN-) REF = 4.096 V	Digital Output Code Twos Complement (Hex)
FSR - 1 LSB	+4.0959375 V	0x1FFF
Midscale + 1 LSB	+62.5 μ V	0x0001
Midscale	0 V	0x0000
Midscale - 1 LSB	-62.5 μ V	0xFFFF
-FSR + 1 LSB	-4.0959375 V	0x1001
-FSR	-4.096 V	0x1000

ANALOG INPUTS

The analog inputs, IN+ and IN-, applied to the AD7626 must be 180° out of phase with each other. Figure 23 shows an equivalent circuit of the input structure of the AD7626.

The two diodes provide ESD protection for the analog inputs, IN+ and IN-. Care must be taken to ensure that the analog input signal does not exceed the reference voltage by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the [ADA4899-1](#) in Figure 27) are different from those of the reference, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the part.

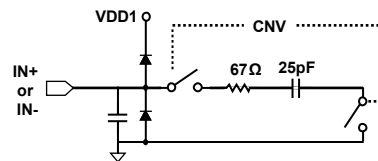


Figure 23. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN-. By using these differential inputs, signals common to both inputs are rejected. The AD7626 shows some degradation in THD with higher analog input frequencies.

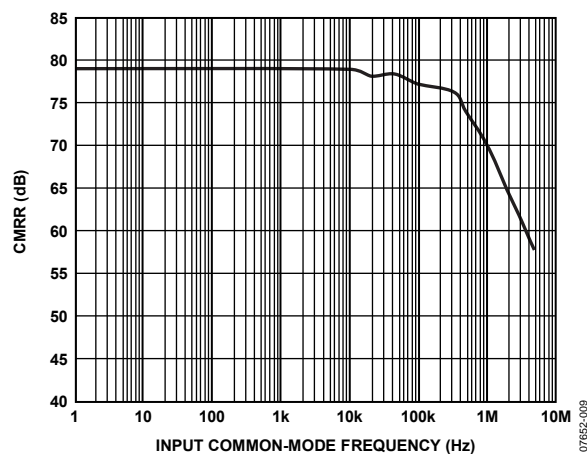
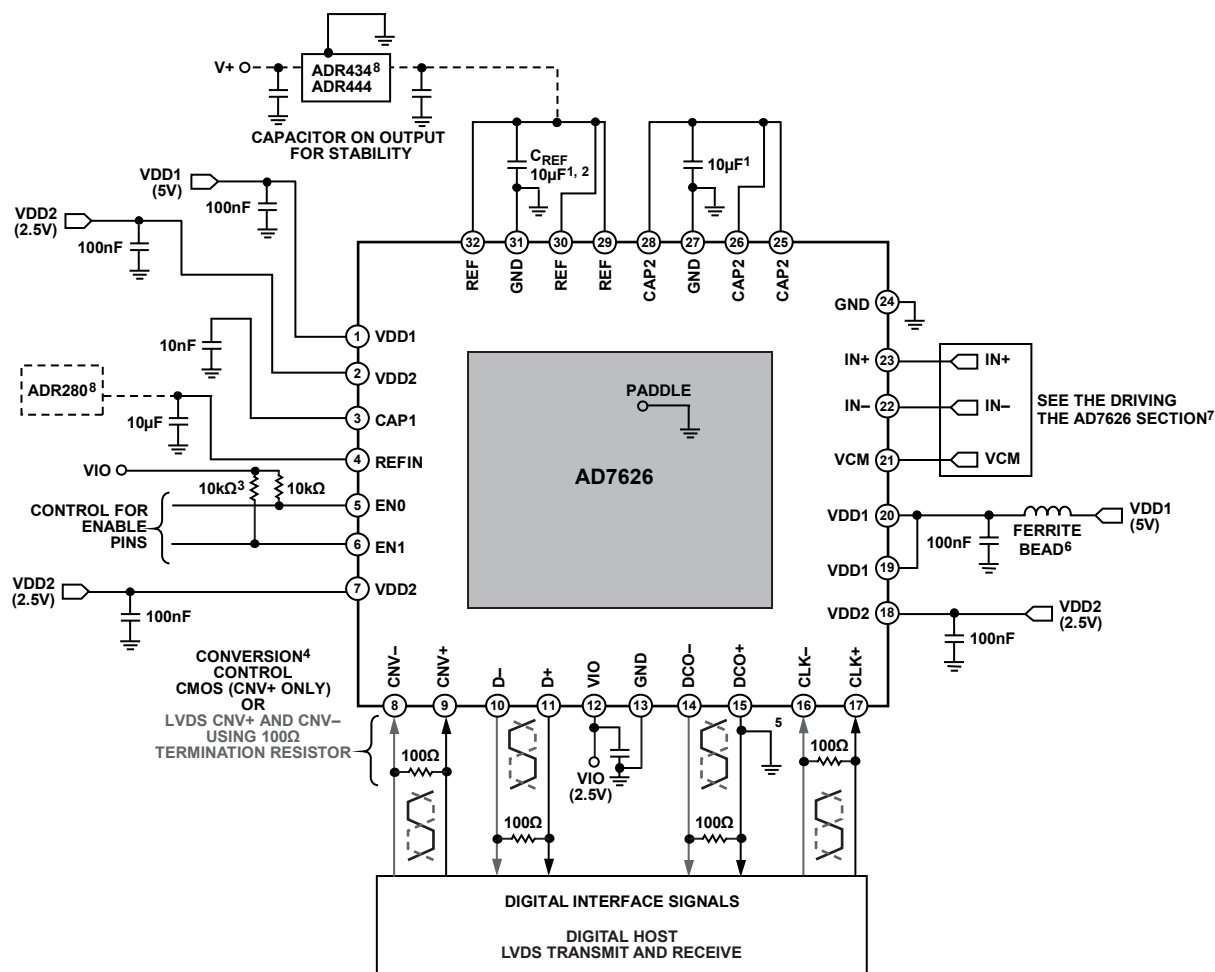


Figure 24. Analog Input CMRR vs. Frequency

TYPICAL CONNECTION DIAGRAM



¹ SEE THE LAYOUT, DECOUPLING, AND GROUNDING SECTION.

² C_{REF} IS USUALLY A 10μF CERAMIC CAPACITOR WITH LOW ESR AND ESL.

³ USE PULL-UP OR PULL-DOWN RESISTORS TO CONTROL EN0, EN1 DURING POWER-UP. EN0 AND EN1 INPUTS CAN BE FIXED IN HARDWARE OR CONTROLLED USING A DIGITAL HOST (EN0 = 0 AND EN1 = 0 PUTS THE ADC IN POWER DOWN).

⁴ OPTION TO USE A CMOS (CNV+) OR LVDS (CNV±) INPUT TO CONTROL CONVERSIONS.

⁵ TO ENABLE SELF-CLOCKED MODE, TIE DCO+ TO GND.

⁶ CONNECT PIN 19 AND PIN 20 TO VDD1 SUPPLY; ISOLATE FROM PIN 1 USING A FERRITE BEAD SIMILAR TO WURTH 74279266.

⁷ SEE THE DRIVING THE AD7626 SECTION FOR DETAILS ON AMPLIFIER CONFIGURATIONS.

⁸ SEE THE VOLTAGE REFERENCE OPTIONS SECTION FOR DETAILS.

Figure 25. Typical Application Diagram

DRIVING THE AD7626

Differential Analog Input Source

Figure 27 shows an ADA4899-1 driving each differential input to the AD7626.

Single-Ended-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver, as shown in Figure 26, allows for a differential input into the part. This configuration, when provided with an input signal of 0 V to 4.096 V, produces a differential ± 4.096 V with midscale at 2.048 V. The one-pole filter using $R = 33\ \Omega$ and $C = 56\ \text{pF}$ provides a corner frequency of 86 MHz. The VCM output of the AD7626 can be buffered and then used to provide the required 2.048 V common-mode voltage.

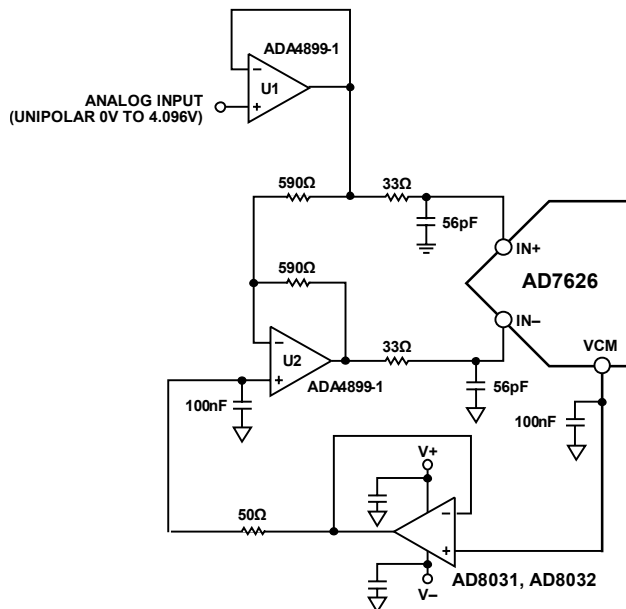
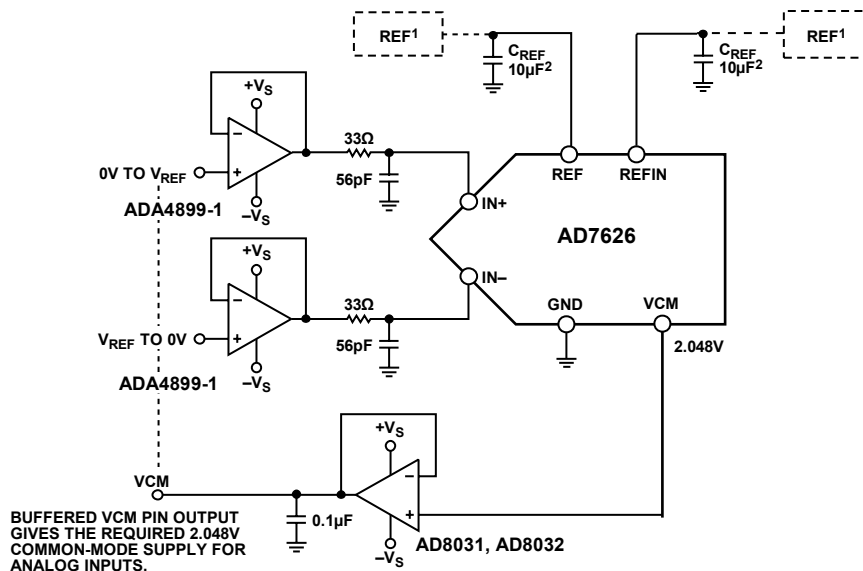


Figure 26. Single-Ended-to-Differential Driver Circuit



¹SEE THE VOLTAGE REFERENCE OPTIONS SECTION. CONNECTION TO EXTERNAL REFERENCE SIGNALS IS DEPENDENT ON THE EN1 AND EN0 SETTINGS.

²C_{REF} IS USUALLY A 10μF CERAMIC CAPACITOR WITH LOW ESL AND ESR.

THE REF AND REFIN PINS ARE DECOUPLED DEPENDENT ON EN1 AND EN0 SETTINGS.

Figure 27. Driving the AD7626 from a Differential Analog Source

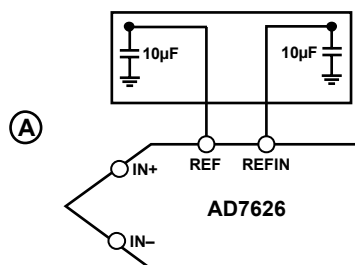
VOLTAGE REFERENCE OPTIONS

The AD7626 allows flexible options for creating and buffering the reference voltage. The AD7626 conversions refer to 4.096 V only. The various options creating this 4.096 V reference are controlled by the EN1 and EN0 pins (see Table 8).

Table 8. Voltage Reference Options

Option	EN1	EN0	Reference Mode
A	1	1	Power Up Internal reference and internal reference buffer in use.
B	0	1	External 1.2 V reference applied to REFIN pin is required.
C	1	0	External 4.096 V reference applied to REF pin required.
	0	0	Power Down Mode

DECOUPLE THE REF AND REFIN PINS EXTERNALLY.

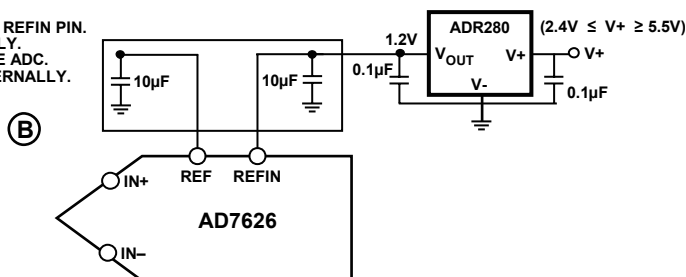


EN1 = 1 AND EN0 = 1

Power Up - Internal Reference and Reference buffer in use.
No External Reference Circnternal Required.

Figure 28. Powered up, Internal Reference and Internal Reference Buffer

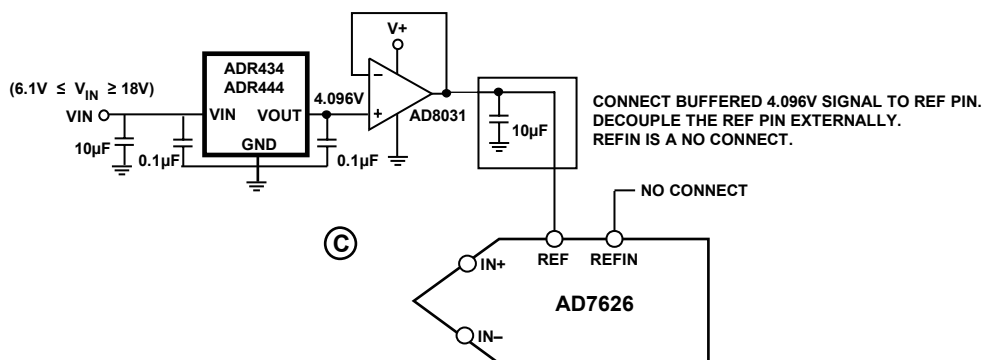
CONNECT 1.2V EXTERNAL REFERENCE TO REFIN PIN.
1.2V REFIN INPUT IS BUFFERED INTERNALLY.
IT CREATES A 4.096V REFERENCE FOR THE ADC.
DECOUPLE THE REF AND REFIN PINS EXTERNALLY.



EN1 = 0 AND EN0 = 1

External 1.2V reference connected to REFIN pin is required.

Figure 29. External 1.2V Reference using internal reference buffer.



EN1 = 1 AND EN0 = 0

External 4.096V Reference connected to REF pin is required.

Figure 30. External 4.096V Reference applied to REF pin

POWER SUPPLY

The AD7626 uses both 5 V (VDD1) and 2.5 V (VDD2) power supplies, as well as a digital input/output interface supply (VIO). VIO allows a direct interface with 2.5 V logic only. VIO and VDD2 can be taken from the same 2.5 V source; however, it is best practice to isolate the VIO and VDD2 pins using separate traces and also to decouple each pin separately.

The 5 V and 2.5 V supplies required for the AD7626 can be generated using Analog Devices, Inc., LDOs such as the [ADP3330-2.5](#), [ADP3330-5](#), [ADP3334](#), and [ADP1708](#).

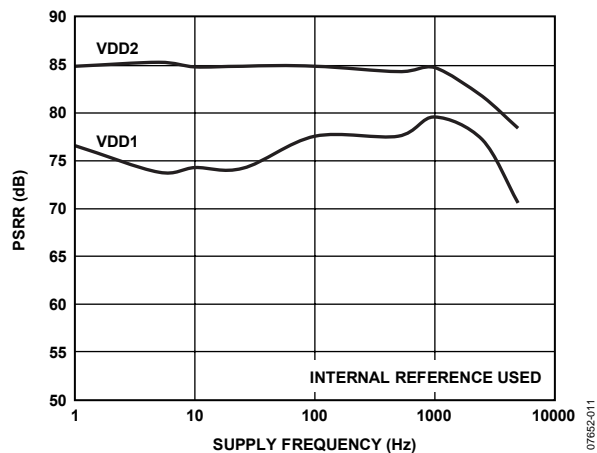


Figure 31. PSRR vs. Supply Frequency
(350 mV pp Ripple on VDD2, 600 mV Ripple on VDD1)

Power-Up

As is best practice for all ADCs, the core supplies should be powered on prior to applying an external reference (where applicable). Lastly apply the analog inputs.

When powering up the AD7626 device, apply the 5V (VDD1) and 2.5V (VDD2, VIO) to the device. Set the reference configuration pins EN0 and EN1 to the correct values. In the case where an external reference is preferred (governed by EN1 and EN0 values), apply the external reference of 1.2V to REFIN pin or 4.096V to REF pin. EN0 = 0 and EN1 = 0 means that the AD7626 is in power down mode.

DIGITAL INTERFACE

Conversion Control

All analog-to-digital conversions are controlled by the CNV signal. This signal can be applied in the form of a CNV+/CNV– LVDS signal, or it can be applied in the form of a 2.5 V CMOS logic signal to the CNV+ pin. The conversion is initiated by the rising edge of the CNV signal.

After the AD7626 is powered up, the first conversion result generated is invalid. Subsequent conversion results are valid provided that the time between conversions does not exceed the maximum specification for t_{CYC} .

The two methods for acquiring the digital data output of the AD7626 via the LVDS interface are described in the following sections.

Echoed-Clock Interface Mode

The digital operation of the AD7626 in echoed-clock interface mode is shown in Figure 32. This interface mode, requiring only a shift register on the digital host, can be used with many digital hosts (FPGA, shift register, microprocessor, and so on). It requires three LVDS pairs ($D\pm$, $CLK\pm$, and $DCO\pm$) between each AD7626 and the digital host.

The clock DCO is a buffered copy of CLK and is synchronous to the data, D, which is updated on the falling edge of $DCO+$ (t_D). By maintaining good propagation delay matching between D and DCO through the board and the digital host, DCO can be used to latch D with good timing margin for the shift register.

Conversions are initiated by a CNV pulse. The CNV pulse must be returned low ($\leq t_{CNVH}$ max) for valid operation. After a conversion begins, it continues until completion. Additional CNV pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK. Note that t_{MSB} is the maximum time for the MSB of the new conversion result and should be used as the gating device for CLK. The echoed clock, DCO, and the data, D, are driven in phase with D being updated on the falling edge of $DCO+$; the host should use the rising edge of $DCO+$ to capture D. The only requirement is that the 16 CLK pulses finish before the time t_{CLKL} elapses of the next conversion phase or the data is lost. From the time t_{CLKL} to t_{MSB} , D and DCO are driven to 0s. Set $CLK\pm$ to idle low between $CLK\pm$ bursts.

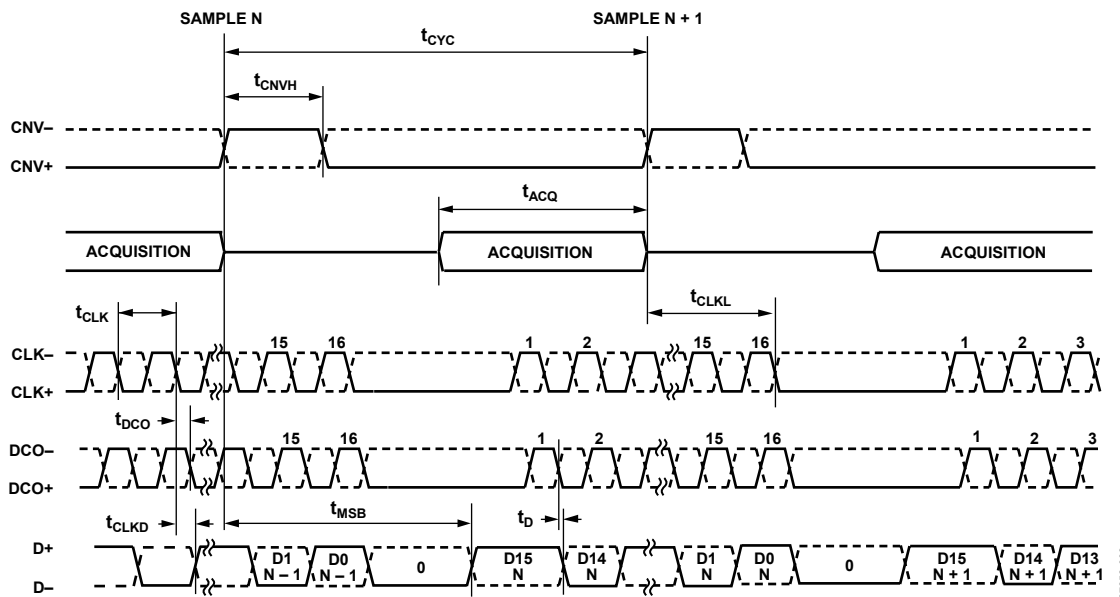


Figure 32. Echoed-Clock Interface Mode Timing Diagram

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The digital operation of the AD7626 in self-clocked interface mode is shown in Figure 33. This interface mode reduces the number of wires between ADCs and the digital host to two LVDS pairs per AD7626 (CLK \pm and D \pm) or to a single pair if sharing a common CLK using multiple AD7626s. This can ease the design in a case with multiple AD7626s in use. The digital host can adapt the interfacing scheme to account for differing propagation delays between each AD7626 device and the digital host.

Conversions are initiated by a CNV pulse. The CNV pulse must be returned low ($\leq t_{\text{CNVH max}}$) for valid operation. After a conversion begins, it continues until completion. Additional CNV pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK. Note that t_{MSB} is the maximum time for the first bit of the header and should be used as the gating device for CLK. CLK is also used internally on the host to begin the internal synchronization state machine. The next header bit and conversion results are output on subsequent falling edges of CLK. The only requirement is that the 18 CLK pulses finish before the time t_{CLKL} elapses of the next conversion phase or the data is lost. Set $\text{CLK}\pm$ to idle high between bursts of 18 CLK pulses.



APPLICATIONS INFORMATION

LAYOUT, DECOUPLING, AND GROUNDING

When laying out the printed circuit board (PCB) for the AD7626, follow the practices described in this section to obtain the maximum performance from the converter.

Exposed Paddle

The AD7626 has an exposed paddle on the underside of the package.

- Solder the paddle directly to the PCB.
- Connect the paddle to the ground plane of the board using multiple vias, as shown in Figure 34.
- Decouple all supply pins except for Pin 12 (VIO) directly to the paddle, minimizing the current return path.
- Pin 13 and Pin 24 can be connected directly to the paddle. Use vias to ground at the point where these pins connect to the paddle.

VDD1 Supply Routing and Decoupling

The VDD1 supply is connected to Pin 1, Pin 19, and Pin 20. The supply should be decoupled using a 100 nF capacitor at Pin 1. The user can connect this supply trace on to Pin 19 and Pin 20. Use a series ferrite bead to connect the VDD1 supply from Pin 1 to Pin 19 and Pin 20. The ferrite bead isolates any high frequency noise or ringing on the VDD1 supply. Decouple the VDD1

supply to Pin 19 and Pin 20 using a 100 nF capacitor decoupled to ground at the exposed paddle.

VIO Supply Decoupling

Decouple the VIO supply applied to Pin 12 to ground at Pin 13.

Layout and Decoupling of Pin 25 to Pin 32

Connect the outputs of Pin 25, Pin 26, and Pin 28 together and decouple them to Pin 27 using a 10 μ F capacitor with low ESR and low ESL.

Reduce the inductance of the path connecting Pin 25, Pin 26, and Pin 28 by widening the PCB traces connecting these pins.

A similar approach should be taken in the connections used for the reference pins of the AD7626. Connect Pin 29, Pin 30, and Pin 32 together using widened PCB traces to reduce inductance. In internal or external reference mode, a 4.096 V reference voltage is output on Pin 29, Pin 30, and Pin 32. Decouple these pins to Pin 31 using a 10 μ F capacitor with low ESR and low ESL.

Figure 34 shows an example of the recommended layout for the underside of the AD7626 device. Note the extended signal trace connections and the outline of the capacitors decoupling the signals applied to the REF pins (Pin 29, Pin 30, and Pin 32) and to the CAP2 pins (Pin 25, Pin 26, and Pin 28).

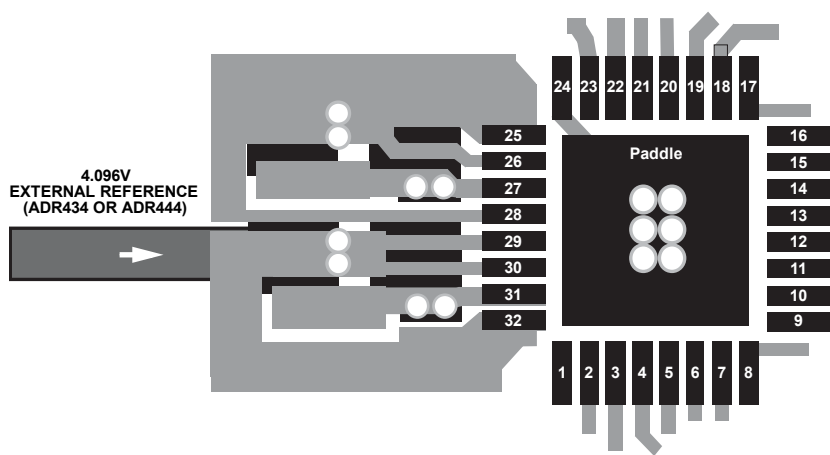


Figure 34. PCB Layout and Decoupling Recommendations for Pin 24 to Pin 32

The mechanical drawings of the 25-pin DIP package are as follows:

- TOP VIEW:** Shows an octagonal package with a square body. Dimensions include a width of 5.00 BSC SQ, a height of 4.75 BSC SQ, and a PIN 1 INDICATOR.
- BOTTOM VIEW:** Shows the exposed pad with dimensions: 0.60 MAX for the top edge, 0.50 BSC for the side edges, 0.50, 0.40, and 0.30 for the bottom edge segments, 3.50 REF for the bottom width, 0.25 MIN for the bottom edge thickness, and 3.25, 3.10 SQ, and 2.95 for the exposed pad area. Pin numbers 1 through 25 are indicated.
- SIDE VIEW:** Shows the package profile with dimensions: 1.00, 0.85, and 0.80 for the top height, 12° MAX for the lead angle, 0.80 MAX and 0.65 TYP for the lead width, 0.05 MAX and 0.02 NOM for the lead thickness, 0.30, 0.23, and 0.18 for the lead spacing, and 0.20 REF for the lead length.

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FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Dimensions shown in millimeters

Model	Temperature Range	Package Description	Package Option
AD7626BCPZ ¹	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
AD7626BCPZ-RL7 ¹	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
EVAL-AD7626EDZ ^{1,2}		Evaluation Board	
EVAL-CED1Z ^{1,3}		Converter Evaluation and Development Board	

³ This board allows the PC to control and communicate with all Analog Devices evaluation boards with model numbers ending with the ED designator.

NOTES

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