16-Bit, 2.5 MSPS PulSAR 11 mW ADC in QFN

Preliminary Technical Data

AD7985

FEATURES

16-bit resolution with no missing codes
Throughput: 2.5 MSPS (TURBO=high)
2.0 MSPS (TURBO=low)
Low power dissipation:
11 mW at 2.5 MSPS, with external reference
22mW at 2.5 MSPS with internal reference
INL: ±1.5 LSB
SNR: 90 dB, with on chip reference
91.5 dB, with external reference
4.096 V internal reference: typ drift 10 ppm/°C
Pseudo differential analog input range
0 V to V_{REF} with V_{REF} up to 5.0 V
Allows use of any input range
No pipeline delay
Logic Interface 1.8 V/2.5 V/2.7 V
Serial interface SPI-/QSPI™-/MICROWIRE™-/DSP-compatible
Ability to daisy-chain multiple ADCs and busy indicator
20-lead 4 mm × 4 mm QFN (LFCSP)

APPLICATIONS

Battery-powered equipment
Communications
ATE
Data acquisition systems
Medical instruments

APPLICATION DIAGRAM

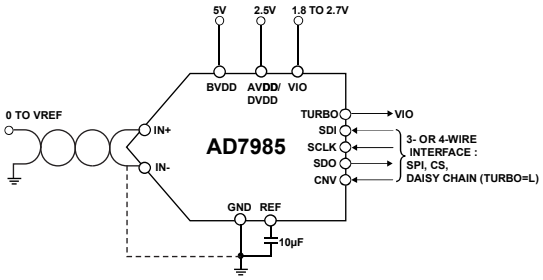

Figure 1.

GENERAL DESCRIPTION

The AD7985 is a 16-bit, 2.5 MSPS successive approximation, analog-to-digital converter (ADC). It contains a low power, high speed, 16-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), error correction circuits, and a versatile serial interface port. On rising edge of CNV, the AD7985 samples an analog input IN+ between 0V and REF with respect to a ground sense IN-. It features a very high sampling rate turbo mode (TURBO=high) and a reduced power normal mode (TURBO=low) for low power applications where the power is scaled with the throughput.

In normal mode (TURBO=low), the SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provide an optional busy indicator. It is compatible with 1.8 V, 2.5 V, and 2.7 V using the separate VIO supply.

The AD7985 is available in a 20-lead QFN (LFCSP) with operation specified from −40°C to +85°C.

Table 1. MSOP, QFN (LFCSP) 14-/16-/18-Bit PulSAR® ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥1000 kSPS	ADC Driver
14-Bit	AD7940	AD7942[1]	AD7946[1]		
16-Bit	AD7680	AD7685[1]	AD7686[1]	AD7980[1]	ADA4941-x
	AD7683	AD7687[1]	AD7688[1]	AD7983[1]	ADA4841-x
	AD7684	AD7694	AD7693[1]	AD7985	
18-Bit		AD7691[1]	AD7690[1]	AD7982[1]	ADA4941-x
				AD7984[1]	ADA4841-x
				AD7986	

[1] Pin-for-pin compatible.

Rev. PrA

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SPECIFICATIONS

AVDD = DVDD=2.5 V, BVDD=5V, VIO = 1.8 V to 2.7 V, REF = 4.096 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ – IN–	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	V
	IN –	−0.1		+0.1	V
Analog Input CMRR					dB[1]
Leakage Current at 25°C	Acquisition phase				nA
Input Impedance		See the Analog Inputs section			
ACCURACY					
No Missing Codes		16			Bits
Differential Linearity Error		−0.90	±0.50	+1.50	LSB[2]
Integral Linearity Error		−1.50	±1.00	+1.50	LSB[2]
Transition Noise			0.8		LSB[2]
Gain Error, T_{MIN} to T_{MAX}[3]					% of FS
Gain Error Temperature Drift					ppm/°C
Zero Error, T_{MIN} to T_{MAX}[3]					µV
Zero Temperature Drift					ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%				dB[1]
THROUGHPUT					
Conversion Rate		0		2.50	MSPS
Transient Response	Full-scale step				ns
AC ACCURACY					
Dynamic Range	V_{REF} = 4.096 V, internal reference		91		dB[1]
	V_{REF} = 5.0 V, external reference		92		
Signal-to-Noise, SNR	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal reference		90.0		dB[1]
	f_{IN} = 20 kHz, V_{REF} = 5.0 V, external reference		91.5		dB[1]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 20 kHz				dB[1]
Total Harmonic Distortion[4], THD	f_{IN} = 20 kHz , V_{REF} = 4.096 V, internal reference		-112		dB[1]
Signal-to-(Noise + Distortion), SINAD	f_{IN} = 20 kHz, V_{REF} = 4.096 V		90.5		dB[1]
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			20		MHz
Aperture Delay					ns

[1] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[2] LSB means least significant bit. With the 4.096 V input range, one LSB is 62.5 µV.
[3] See Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[4] Tested fully in production at f_{IN} = 1 kHz.

AVDD = DVDD=2.5 V, BVDD=5V, VIO = 1.8 V to 2.7 V, REF = 4.096 V, T_A = −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INTERNAL REFERENCE	PDREF = low				
Output Voltage	T_A= 25°C	4.081	4.096	4.111	V
Temperature Drift	−40°C to +85°C		±10		ppm/°C
Line Regulation	AVDD = 2.5 V ± 5%				ppm/V
Turn-On Settling Time	C_{REF}=10µF, $C_{REFBUFIN}$=0.1µF		40		ms
REFIN Output Voltage	REFIN @ 25°C		1.2		V
REFIN Output Resistance			6		kΩ
EXTERNAL REFERENCE	PDREF=high, Refin= low				
Voltage Range		2.4		5.1	V
Current Drain					µA
REFERENCE BUFFER					
REFIN Input Voltage Range			1.2		V
REFIN Input Current					
DIGITAL INPUTS					
Logic Levels					
V_{IL}					V
V_{IH}					V
I_{IL}					µA
I_{IH}					µA
DIGITAL OUTPUTS					
Data Format			Serial 16 bits, straight binary		
Pipeline Delay			Conversion results available immediately after completed conversion		
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
BVDD		4.75	5.0	5.25	
VIO	Specified performance	1.8	2.5	2.7	V
VIO Range					V
Standby Current[1, 2]	VDD and VIO = 2.5 V		1..0		µA
Power Dissipation					mW
With Internal Reference	2.5 MSPS throughput		22		mW
Without Internal Reference	2.5 MSPS throughput		11		mW
With Internal Reference	2.0 MSPS throughput		19		mW
Without Internal Reference	2.0 MSPS throughput		8		mW
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

AVDD = DVDD=2.5 V, BVDD=5V, VIO = 1.8 V to 2.7 V, REF = 4.096 V, T_A = −40°C to +85°C, unless otherwise noted.[1]

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available (Turbo mode / Normal mode)	t_{CONV}	350/450			ns
Acquisition Time	t_{ACQ}	100			ns
Time Between Conversions (Turbo mode / Normal mode)	t_{CYC}	400/500			ns
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
Data Read During Conversion	t_{DATA}			180	ns
Quiet Time During Acquisition from Last SCK Falling Edge to CNV Rising Edge	t_{QUIET}	20			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	9			ns
SCK Period (Chain Mode)	t_{SCK}	11			ns
SCK Low Time	t_{SCKL}	3.5			ns
SCK High Time	t_{SCKH}	3.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	2			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			4	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}			5	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			8	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	4			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

[1] See Figure 2 and Figure 3 for load conditions.

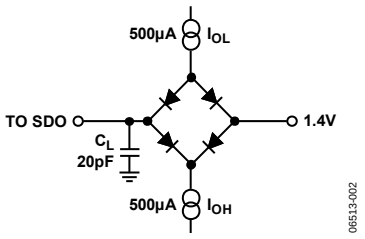

Figure 2. Load Circuit for Digital Interface Timing

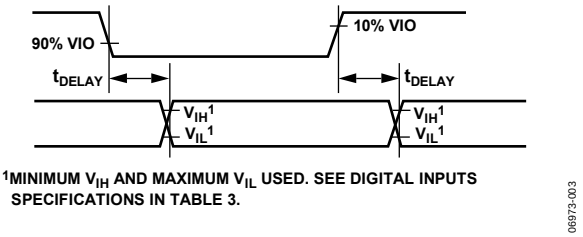

Figure 3. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN– to GND[1]	–0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, BVDD to GND,REFGND	–0.3 V to +6.0 V
AVDD,DVDD ,VIO to GND	–0.3 V to +2.7 V
VDD to VIO	+3 V to –6 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
20-Lead QFN (LFCSP)	30.4°C/W
Lead Temperatures	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Inputs section for an explanation of IN+ and IN–.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

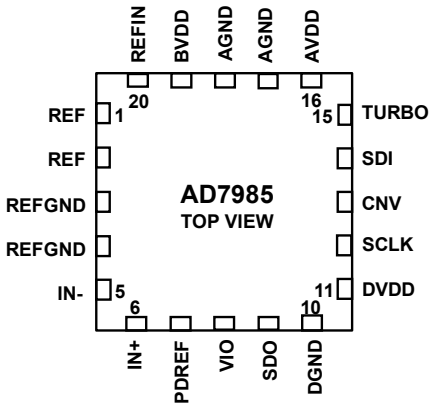

Figure 4. 10-Lead QFN (LFCSP) Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1,2	REF	AI	Reference Output / Input Voltage. When PDREF=Low, the internal reference and buffer are enabled producing 4.096V on this pin. When PDREF=High, the internal reference and buffer are disabled allowing an externally supplied voltage reference up to 5 V. Decoupling is required with or without the internal reference and buffer. This pin is referred to the REFGND pin and should be decoupled closely to the REFGND pin with a 10 µF capacitor.
3,4	REFGND	AI	Reference Input Analog Ground.
5	IN-	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
6	IN+	AI	Analog Input. It is refered to IN-. The voltage range, for example, the difference between IN+ and IN-, is 0V to V_{REF}
7	PDREF	DI	Internal Reference Power-Down Input. When low, the internal reference is enabled. When high, the internal reference is powered down, and an external reference must be used.
8	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, or 2.7V).
9	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
10	DGND	P	Digital Power Ground.
11	DVDD	P	Digital Power. Nominally at 2.5V.
12	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
13	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data should be read when CNV is high.
14	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
15	TURBO	DI	Conversion Mode Selection. When TURBO=High the maximum throughput (2.5 MSPS) is achieved. The ADC does not power down between conversions. When TURBO=Low the maximum throughput is lower (2.0 MSPS). The ADC powers down between conversions.

16	AVDD	P	Input Analog Power. Nominally at 2.5V.
17,18	AGND	P	Analog Power Ground.
19	BVDD	P	Reference buffer power. Nominally 5V If an external reference buffer is used to achieve the maximum SNR performance with 5V reference. The reference buffer must be powered down by connecting the REFIN pin to ground. The external reference buffer must be connected to the BVDD pin.
20	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. When PDREF=Low, the internal band gap reference produces a 1.2V (typical) voltage on this pin, which needs external decoupling (0.1uF typical). When PDREF=High use an external reference to provide a 1.2V (typical) to this pin. When PDREF=High and REFIN=low, the on chip reference buffer and band gap are powered down. An external reference must be connected to REF and BVDD.

[1] AI = analog input, AI/O = bi-directional analog; DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 6).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The last transition (from 111 ... 10 to 111 ... 11) should occur for an analog voltage 1½ LSB below the nominal fullscale (4.999886V for the 0V to 5V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$\textit{Noise-Free Code Resolution} = \log_2(2^N/\textit{Peak-to-Peak Noise})$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$\textit{Effective Resolution} = \log_2(2^N/\textit{RMS Input Noise})$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBF so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

THEORY OF OPERATION

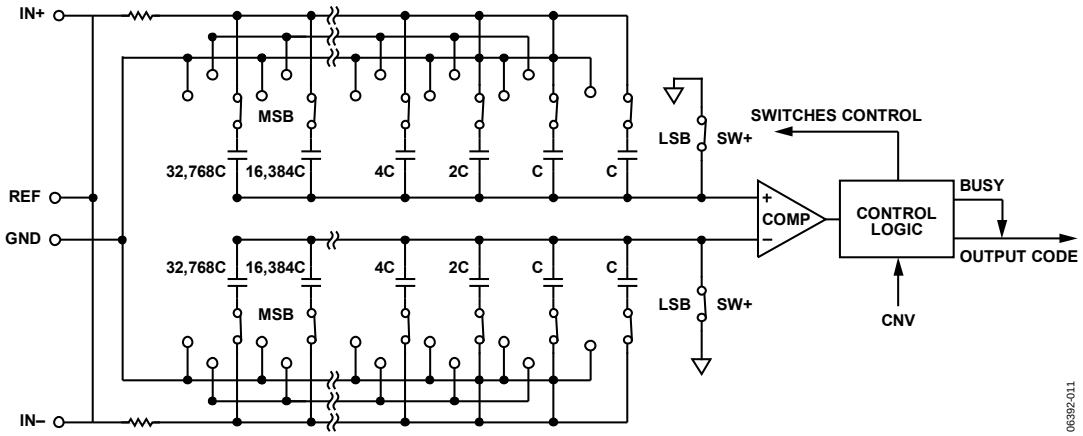

Figure 5. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7985 is a fast, low power, single-supply, precise 16-bit ADC that uses a successive approximation architecture. The AD7985 features different modes to optimize performances according to their applications. In turbo mode, the AD7985 is capable of converting 2,500,000 samples per second (2.5 MSPS).

The AD7985 provides the user with on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

Figure 5 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW–. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN– inputs. When the acquisition phase is completed and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW– are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN– captured at the end of the acquisition phase are applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65,536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7985 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

The AD7985 can be interfaced to any 1.8 V to 2.7 V digital logic family. It is available in a 20-lead QFN (LFCSP) that allows space savings and allows flexible configurations.

It is pin-for-pin compatible with the 18-bit AD7986.

CONVERTER OPERATION

The AD7985 is a successive approximation ADC based on a charge redistribution DAC.

CONVERSION MODES OF OPERATION

The AD7985 features two conversion modes of operation: turbo and normal. Turbo conversion mode (TURBO=high) allows the fastest conversion rate of up to 2.5 MSPS, and does not power down between conversions. The first conversion in turbo mode should be ignored since it contains meaningless data. For applications which require lower power and slightly slower sampling rates, the normal mode (TURBO = low) allows a maximum conversion rate of 2.0 MSPS, and powers down between conversion. The first conversion in normal mode does contain meaningful data.

Transfer Functions

The ideal transfer characteristic for the AD7985 is shown in Figure 6 and Table 7.

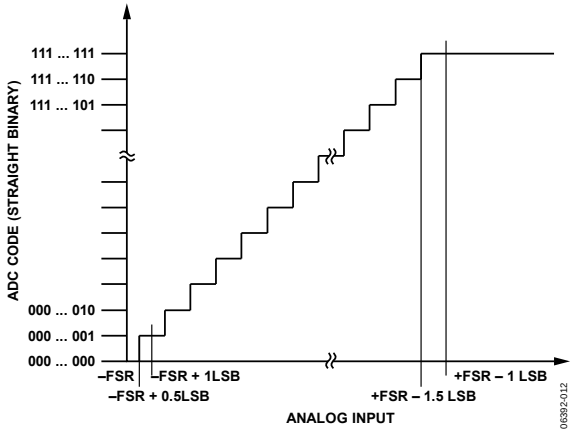

Figure 6. ADC Ideal Transfer Function

Figure 7 shows an example of the recommended connection diagram for the AD7985 when multiple supplies are available.

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input	
	V_{REF} = 4.096 V	Digital Output Code (Hexa)
FSR – 1 LSB	4.095938 V	FFFF[1]
Midscale + 1 LSB	2.048063 V	8001
Midscale	2.048 V	8000
Midscale – 1 LSB	2.047938 V	7FFF
–FSR + 1 LSB	62.5 µV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL CONNECTION DIAGRAM

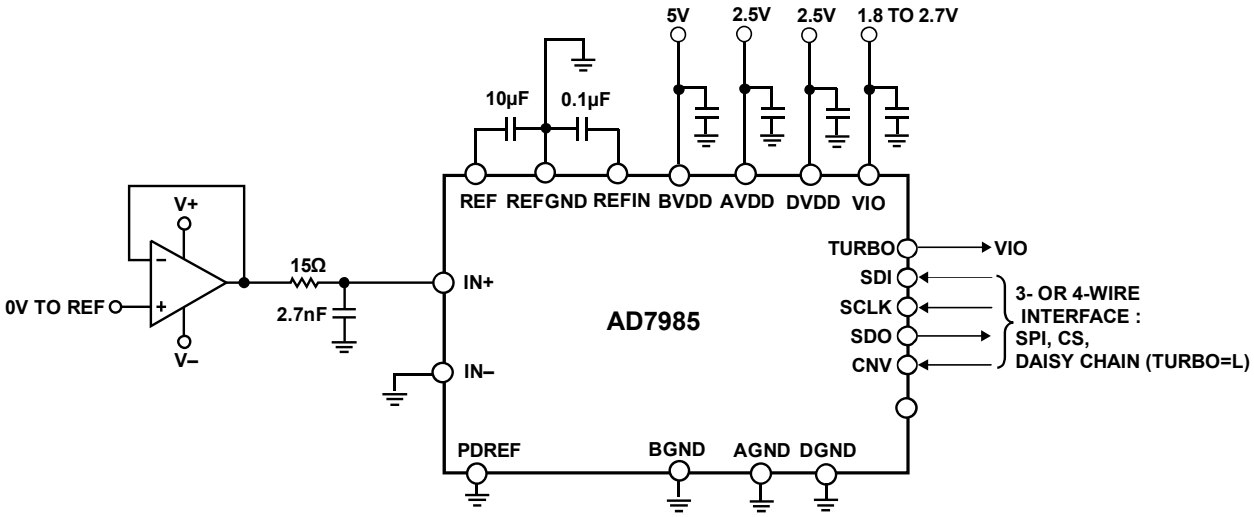

Figure 7. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 8 shows an equivalent circuit of the input structure of the AD7985.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal does not exceed the reference input Figure 7) are different from those of REF, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short-circuit), the current limitation can be used to protect the part.

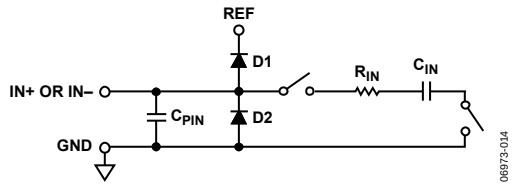

Figure 8. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the sampling phase, where the switches are closed, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

When the source impedance of the driving circuit is low, the AD7985 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7985 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7985. The noise from the driver is filtered by the AD7985 analog input circuit's 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7985 is 50 μV rms, the SNR degradation due to the amplifier is

voltage (REF) by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies, V+ and V-, of the buffer amplifier in

$$SNR_{LOSS} = 20 \log \left(\frac{50}{\sqrt{50^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

where:
f_{-3dB} is the input bandwidth, in megahertz, of the AD7985 (20 MHz) or the cutoff frequency of the input filter, if one is used.
N is the noise gain of the amplifier (for example, 1 in buffer configuration).
e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7985.
- For multichannel multiplexed applications, the driver amplifier and the AD7985 analog input circuit must settle for a full-scale step onto the capacitor array at an 16-bit level (0.0015%, 15 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at an 16-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
ADA4899-1	Ultra low noise and high frequency
AD8014	Low power, high frequency

Figure 9. Single-Ended-to-Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7985 allows the choice of either a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the AD7985 provides excellent performance and can be used in almost all applications.

Internal Reference, REF=4.096V (PDREF = Low)

To use the internal reference, the PDREF input must be low. This enables the on-chip band gap reference, and buffer, resulting in a 4.096 V reference on the REF pin (1.2V on REFIN).

The internal reference is temperature compensated to 4.096 V ± 15 mV. The reference is trimmed to provide a typical drift of 10 ppm/°C.

The output resistance of REFIN is 6 kΩ when the internal reference is enabled. It is necessary to decouple this pin with a ceramic capacitor of at least 100 nF. The output resistance of REFIN and the decoupling capacitor form an RC filter which helps to reduce noise.

Since the output impedance of REFIN is typically 6 kΩ, relative humidity (among other industrial contaminates) can directly affect the drift characteristics of the reference. A guard ring is typically used to reduce the effects of drift under such circumstances. However, the fine pitch of the AD7985 makes this difficult to implement. One solution, in these industrial and other types of applications, is to use a conformal coating, such as Dow Corning® 1-2577 or HumiSeal® 1B73.

External 1.2 V Reference and Internal Buffer (PDREF = High)

To use an external reference along with the internal buffer, PDREF should be high. This powers down the internal reference and allows the 1.2 V reference to be applied to REFIN, producing 4.096 V (typically) on the REF pin.

External Reference (PDREF = High, REFIN= low)

To apply an external reference voltage directly to the REF pin, PDREF should be tied high, and REFIN should be tied low. BVDD should also be driven to the same potential as REF. For example if REF=2.5V, BVDD should be tied to 2.5V.

The advantages of directly using the external voltage reference are:

- The SNR and dynamic range improvement (about 1.7 dB) resulting from the use of a larger reference voltage (5 V) instead of a typical 4.096 V reference when the internal reference is used. This is calculated by

$$SNR = 20\log\left(\frac{4.096}{5.0}\right)$$

- The power savings when the internal reference is powered down (PDREF high).

Reference Decoupling

The AD7985 voltage reference input, REF, has a dynamic input impedance which requires careful decoupling between the REF and REFGND pins. The Layout section describes how this can be done.

When using an external reference, a very low impedance source (for example, a reference buffer using the AD8031 or the AD8605), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, a reference decoupling capacitor with values as small as 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and REFGND pins.

POWER SUPPLY

The AD7985 uses 4 power supply pins: an analog supply (AVDD), a buffer supply (BVDD), a digital supply (DVDD), and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 2.7 V. To reduce the number of supplies needed, VIO, DVDD, and AVDD can be tied together. The AD7985 is independent of power supply sequencing between all of its supplies. Additionally, it is very insensitive to power supply variations over a wide frequency range.

DIGITAL INTERFACE

Although the AD7985 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7985 is compatible with SPI, MICROWIRE™, QSPI™, and digital hosts. In this mode, the AD7985 can use either a 3-wire or a 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7985 provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register. Chain mode is only available Normal mode (Turbo=Low).

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In Normal mode operation, the AD7985 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must timeout the maximum conversion time prior to readback.

The busy indicator feature is enabled

- In the $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 13 and Figure 17).
- Turbo must be kept low for both digital interfaces.

When CNV is low, reading can occur during conversion, acquisition, and split across acquisition and conversion, as detailed in the following sections.

A discontinuous SCK is recommended because the part is selected with CNV low, and SCK activity begins to clock out data.

Note that in the following sections, the timing diagrams indicate digital activity (SCK, CNV, SDI, and SDO) during the conversion. However, due to the possibility of performance degradation, digital activity should occur only prior to the safe data reading time, t_{DATA}, because the AD7985 provide error correction circuitry that can correct for an incorrect bit decision during this time. From t_{DATA} to t_{CONV}, there is no error correction and conversion results may be corrupted. Similarly, t_{quiet} , the time from the last falling edge to the rising edge of CNV, must remain free of digital activity. The user should configure the AD7985 and initiate the busy indicator (if desired in normal mode) prior to t_{DATA}. It is also possible to corrupt the sample by having SCK near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 20 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

DATA READING OPTIONS

There 3 different data reading options for the AD7985. There is the option to read during conversion, to split the read across acquisition and conversion (see Figures 14 & 18), and in normal mode, to read during acquisition. The desired SCK frequency will largely determine which reading option to pursue.

Reading During Conversion, Fast Hosts (Turbo or Normal Mode)

When reading during conversion (n), conversion results are for the previous (n – 1) conversion. Reading should only occur up to t_{DATA} and, because this time is limited, the host must use a fast SCK.

The required SCK frequency is calculated by

$$f_{SCK} \geq \frac{Number\_SCK\_Edges}{t_{DATA}}$$

To determine the SCK frequency, let's follow these examples to read data from conversion (n-1).

Turbo Mode (2.5Msps):

Number_SCK_Edges = 16; t_{DATA} =180ns

f_{SCK} = 16/180ns = 88.9MHz

Normal Mode (2.0Msps):

Number_SCK_Edges = 16; t_{DATA} =280ns

f_{SCK} = 16/280ns = 57.14MHz

The time between t_{DATA} and t_{CONV} is an I/O quiet time where digital activity should not occur, or sensitive bit decisions may be corrupt.

Split-Reading , Any Speed Host (Turbo or Normal Mode)

To allow for slower SCK, there is the option of a split read where data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n – 1) conversion.

Similar to reading during conversion, reading should only occur up to t_{DATA}. For the maximum throughput, the only time restriction is that reading take place during the t_{ACQ} (min) + t_{DATA} – t_{QUIET} time. The time between the falling edge of SCK and CNV rising is an acquisition quiet time, t_{QUIET} .

To determine how to split the read for a particular SCK frequency, let's follow these examples to read data from conversion (n-1).

Turbo Mode (2.5Msps):

f_{SCK} = 80MHz; t_{DATA} =180ns

Number_SCK_Edges = 85MHz * 180ns = 14.40

14 bits are read during conversion (n), and 2 bits are read during acquisition (n).

Normal Mode (2.5Msps):

f_{SCK} = 45MHz; t_{DATA} =280ns

Number_SCK_Edges = 50MHz * 280ns = 12.6

12 bits are read during conversion (n), and 4 bits are read during acquisition (n).

For slow throughputs, the time restriction is dictated by the user's required throughput, and the host is free to run at any speed. Similar to the reading during acquisition, for slow hosts, the data access must take place during the acquisition phase with additional time into the conversion.

Note that data access spanning conversion requires the CNV to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Thus, the host must perform two bursts of data access when using this method.

Reading During Acquisition, Any Speed Hosts, (Turbo or Normal Mode)

When reading during acquisition (n), conversion results are for the previous (n – 1) conversion. Maximum thoughput is achievable in Normal mode (2.0Msps), however in Turbo mode, 2.5Msps throughput is not achievable..

For the maximum throughput, the only time restriction is that the reading take place during the t_{ACQ} (min) time. For slow throughputs, the time restriction is dictated by throughput required by the user, and the host is free to run at any speed. Thus for slow hosts, data access must take place during the acquisition phase.

$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 10, and the corresponding timing is given in Figure 11.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues until completion irrespective of the state of CNV. This can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7985 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

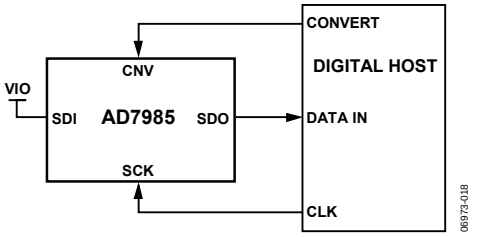

Figure 10. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Connection Diagram (SDI High)

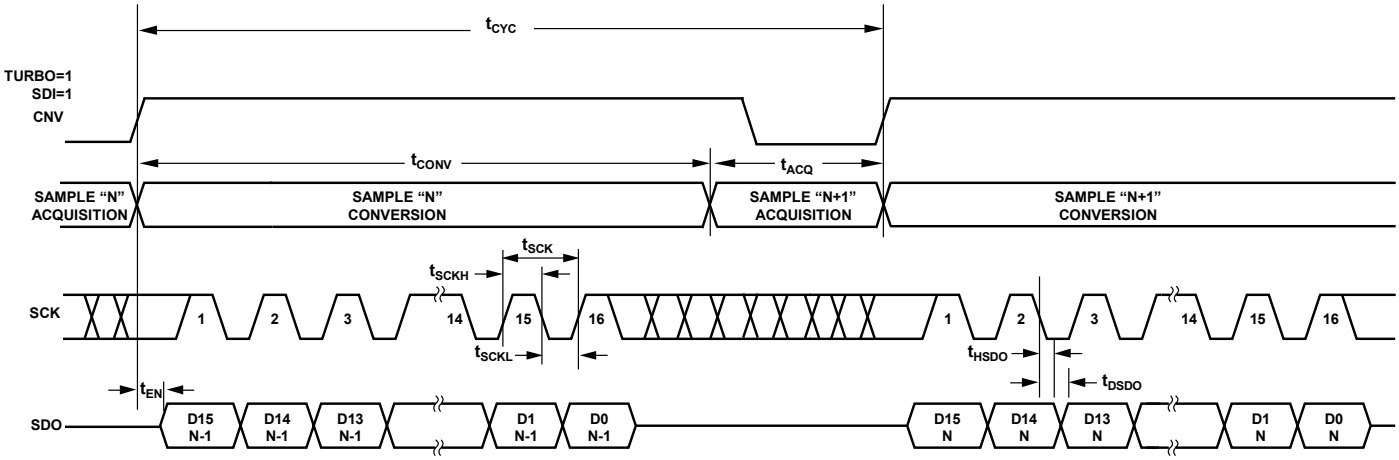

Figure 11. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host having an interrupt input. It is only available in Normal conversion mode (Turbo=low).

The connection diagram is shown in Figure 12, and the corresponding timing is given in Figure 13.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge, SDO returns to high impedance.

If multiple AD7985s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

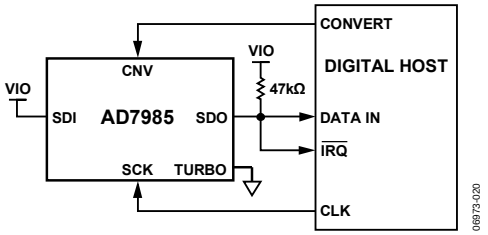

Figure 12. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Connection Diagram (SDI High)

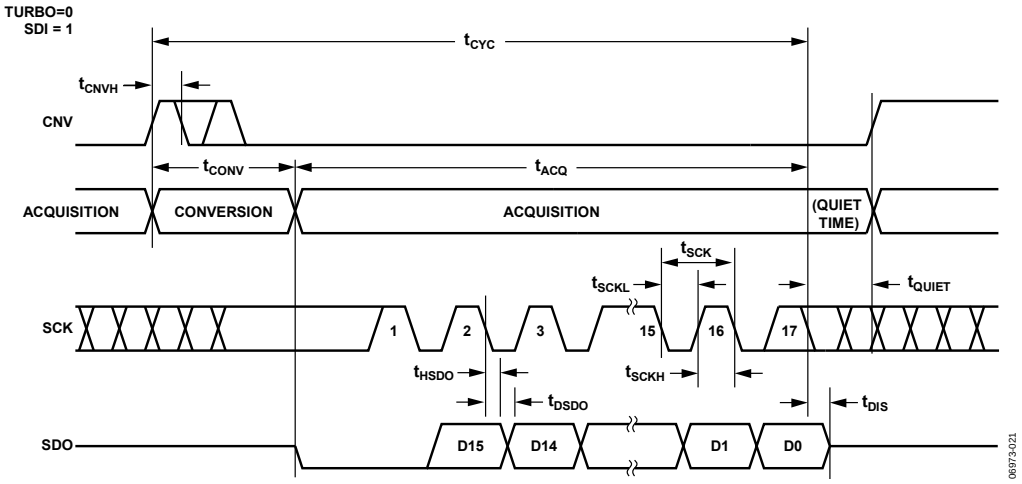

Figure 13. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7985s are connected to an SPI-compatible digital host.

A connection diagram example using two AD7985s is shown in Figure 14, and the corresponding timing is given in Figure 15.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7985 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge, SDO returns to high impedance and another AD7985 can be read.

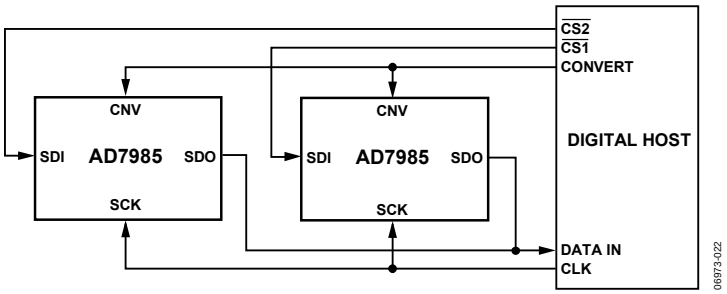

Figure 14. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

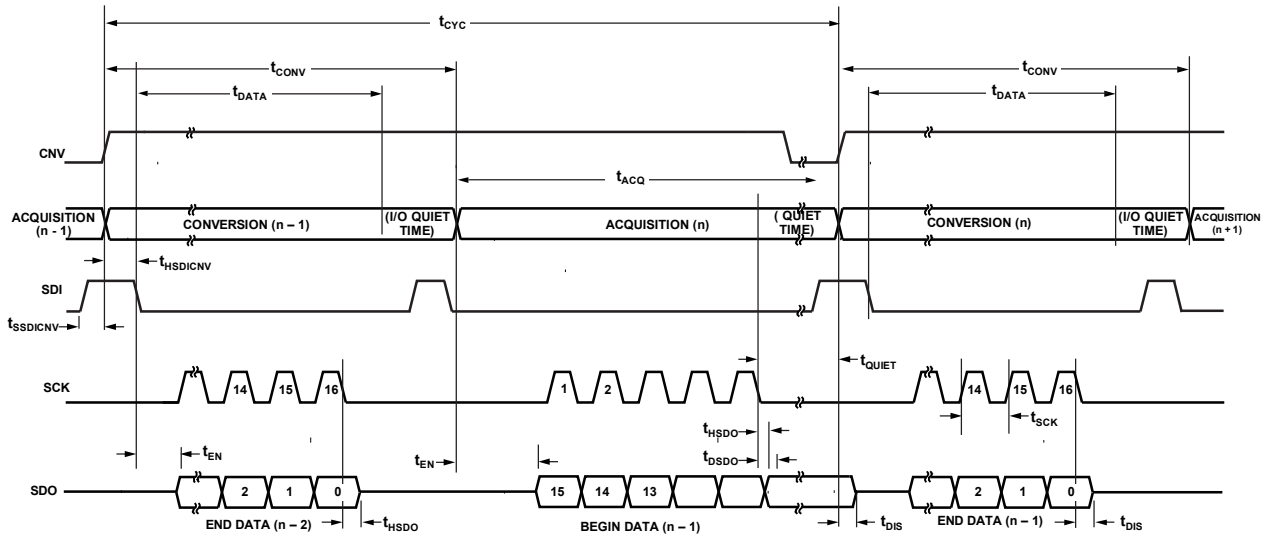

Figure 15. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7985 is connected to an SPI-compatible digital host with an interrupt input and when it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired. This mode is only available in Normal conversion mode (Turbo=low).

The connection diagram is shown in Figure 16, and the corresponding timing is given in Figure 17.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or SDI going high (whichever occurs first), SDO returns to high impedance.

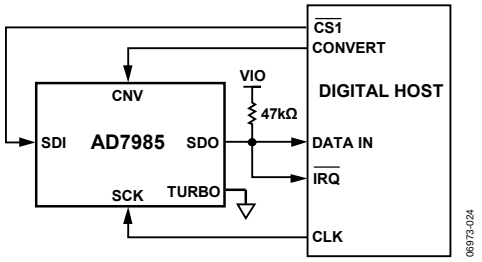

Figure 16. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Connection Diagram

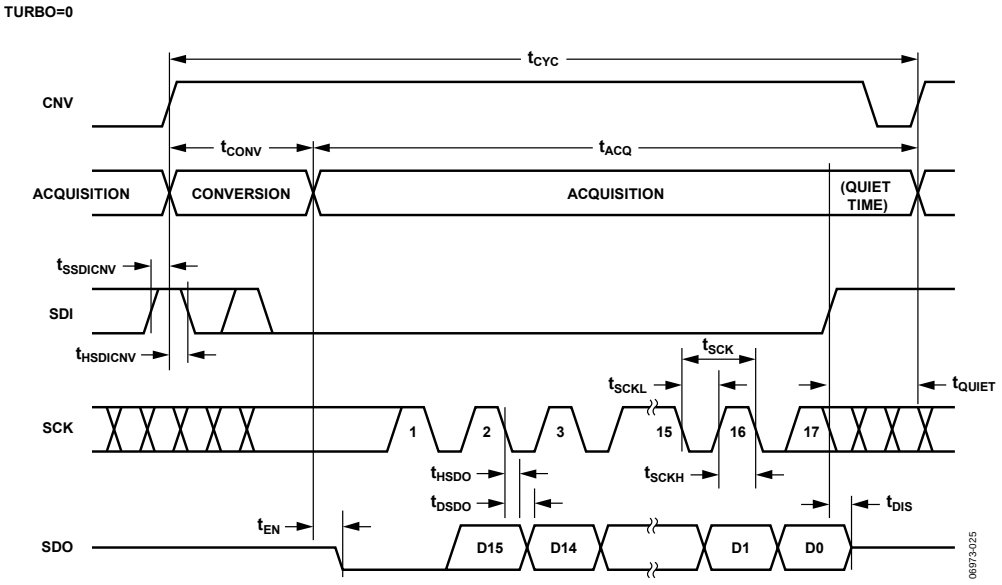

Figure 17. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7985s on a 3-wire serial interface. It is only available in Normal conversion mode (Turbo=low). This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7985s is shown in Figure 18, and the corresponding timing is given in Figure 19.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7985 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7985s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

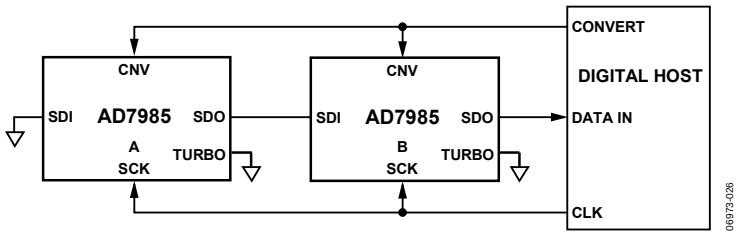

Figure 18. Chain Mode Without Busy Indicator Connection Diagram

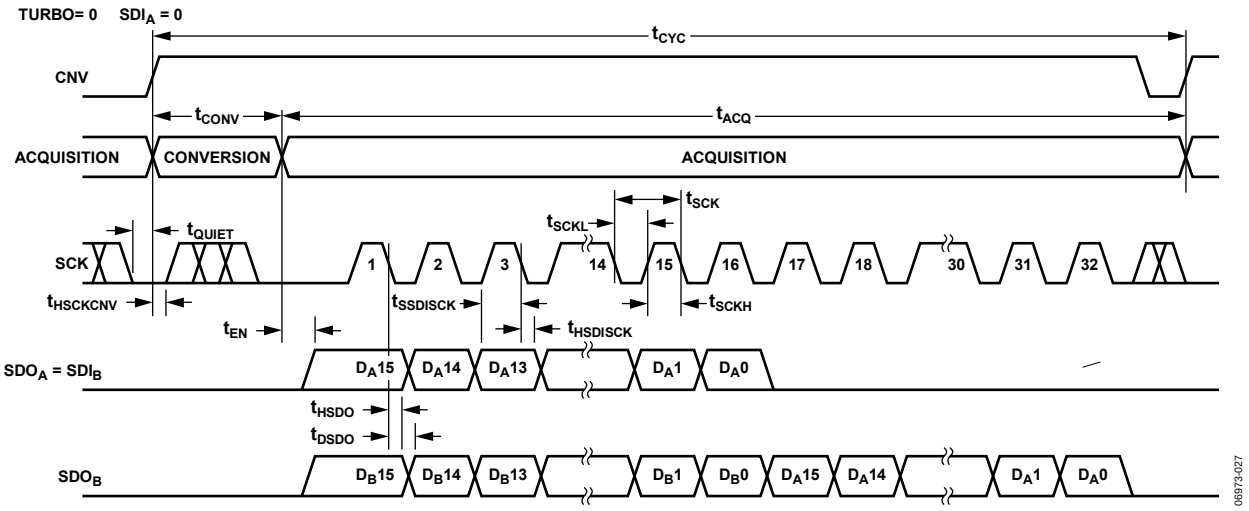

Figure 19. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7985s on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.A connection diagram example using three AD7985s is shown in Figure 20, and the corresponding timing is given in

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7985 ADC labeled C in Figure 20) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7985 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to read back the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7985s in the chain, provided the digital host has an acceptable hold time.

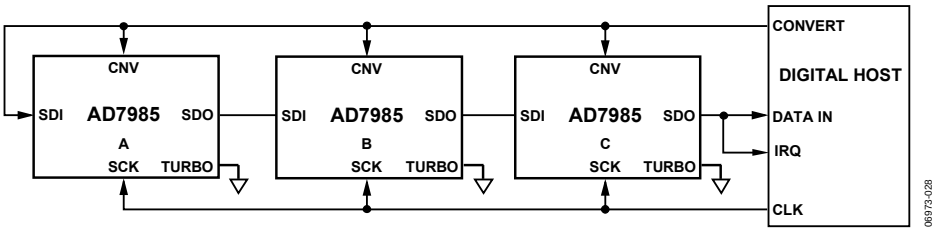

Figure 20. Chain Mode with Busy Indicator Connection Diagram

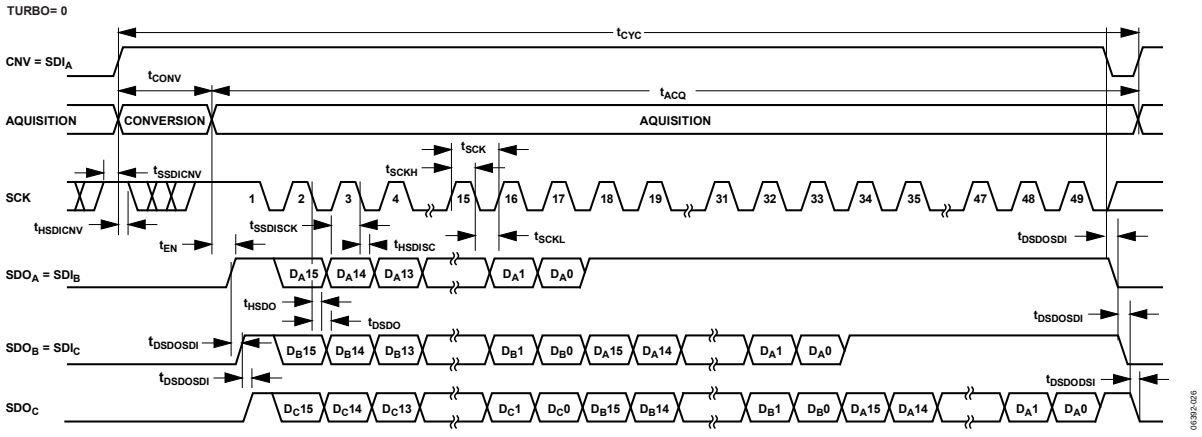

Figure 21. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board (PCB) that houses the AD7985 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7985, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7985 is used as a shield. Fast switching signals, such as CNV or clocks, should not run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7985s.

The AD7985 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7985 should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7985 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

EVALUATING THE AD7985 PERFORMANCE

Other recommended layouts for the AD7985 are outlined in the documentation of the evaluation board for the AD7985 (EVAL-AD7985CB). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-CONTROL BRD3.

OUTLINE DIMENSIONS

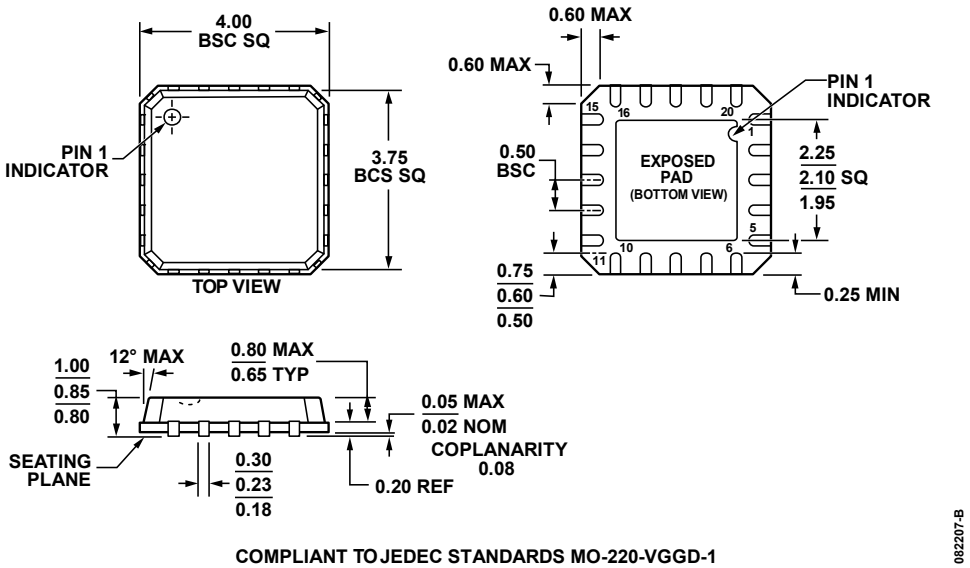

Figure 22. 20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
4 mm x4mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown inmillimeters.