Triple Skew-Compensating Video Delay Line with Analog and Digital Control

Preliminary Technical Data

AD8120

FEATURES

Corrects for Unshielded Twisted Pair (UTP) cable delay skew
Broadband delay up to a total of 50 nsec per channel
- **152 MHz BW @ V_O = 2 V_{P-P} & 0ns delay**
- **106 MHz BW @ V_O = 2 V_{P-P} & 50ns delay**

Channel-to-channel output matching within ±4%
- **Low output offset**
- **No external circuitry required to correct for offsets**

Independent Red, Green and Blue delay controls
Digital or analog delay control
- **Six-bit digital control over standard SPI bus**
- **I^2C control**
- **Analog voltage control with on-chip MUXed ADC**

Fixed overall gain of 2
Low Noise
Large differential input impedance: 10 MΩ
32-lead 5 mm × 5 mm LFCSP package

APPLICATIONS

Keyboard-video mouse (KVM)
Digital Signage
RGB video over UTP cable
Professional video projection and distribution
HD Video
Security video
General Broadband Delay Lines

GENERAL DESCRIPTION

The AD8120 is a triple broadband skew delay compensation IC that corrects for time mismatch of video signals incurred by transmission in unshielded twisted pairs of Category-5 and Category-6 type cables. Skew between the individual pairs exists in most types of multi-pair UTP cables due to the different twist-rates used for each pair in order to minimize crosstalk among the pairs. Some pairs are therefore longer than others, and in long cables, the difference in propagation time between two pairs can be well into the tens of nanoseconds.

The AD8120 contains three delay paths which provide broadband delays up to 50 nanoseconds, in 0.8 ns increments, using 64 digital control steps or analog control adjustment. The delay technique used in the AD8120 minimizes noise and offset at the outputs. It has a broad bandwidth that ranges between 106MHz and 152 MHz, depending upon the delay setting. This high output bandwidth capability makes AD8120 ideal in applications that receive high-resolution video over UTP cables.

The logic circuitry inside the AD8120 provides for individual delay control of each path. The three delay times can be independently set using a standard four-wire SPI bus, standard I^2C bus or by applying three analog control voltages to the V_{CR}, V_{CG}, and V_{CB} pins. Analog control offers a simple solution for systems that do not have digital control available, the simplest being potentiometer control.

The AD8120 is designed to be used with the AD8123 triple UTP equalizer in video-over-UTP applications, but can be used in other applications where similar controllable broadband delays are required.

FUNCTIONAL BLOCK DIAGRAM

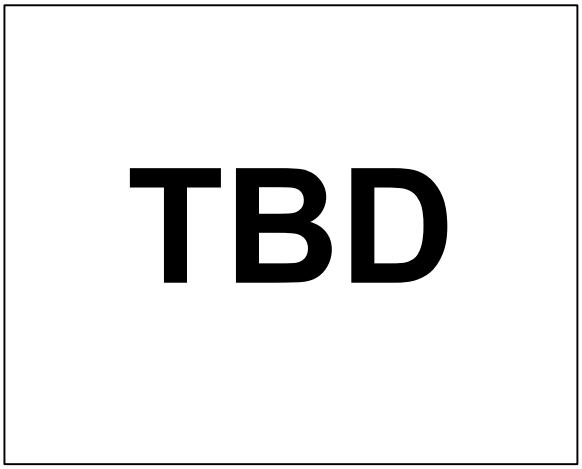

Figure 1.

The AD8120 is available in a 5 mm × 5 mm 32-lead LFCSP package and is rated to operate over the industrial temperature range of -40°C to +85°C.

Rev. PrA

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REVISION HISTORY

Revision PrA: Initial Version

SPECIFICATIONS

T_A = 25°C, Vs = ±5V, R_L=150 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
DELAY CHARACTERISTICS					
Total Adjustable Delay Range	Delay Code 63 – Delay Code 0		50		ns
Delay Resolution	Monotonic, 1 LSB		0.8		ns
Propagation Delay	Delay at 0 ns setting		5.9		ns
Channel to Channel Delay Error	At maximum delay		0.7		%
Delay Differential Nonlinearity (DNL)	See Applications Section for Details				LSB
Delay Integral Nonlinearity (INL)	See Applications Section for Details				LSB
DYNAMIC PERFORMANCE					
-3dB Large Signal Bandwidth	V_{OUT} = 2 V_{P-P}, delay at 0 ns		152		MHz
	V_{OUT} = 2 V_{P-P}, delay at 50 ns		106		MHz
-3dB Video Signal Bandwidth	V_{OUT} = 1.4 V_{P-P}, delay at 0 ns				MHz
	V_{OUT} = 1.4 V_{P-P}, delay at 50 ns				MHz
-3dB Small Signal Bandwidth	V_{OUT} = 0.2 V_{P-P}, delay at 0 ns				MHz
	V_{OUT} = 0.2 V_{P-P}, delay at 50 ns				MHz
0.1 dB Video Signal Flatness	V_{OUT} = 1.4 V_{P-P}, delay at 0 ns				MHz
	V_{OUT} = 1.4 V_{P-P}, delay at 50 ns				MHz
10% to 90% Rise/Fall Time	V_{OUT} = 1.4 V step, delay at 0 ns		3.5		ns
	V_{OUT} = 1.4 V step, delay at 50 ns		4.5		ns
Settling Time to 1%	V_{OUT} = 1.4 V step, delay at 0 ns		5		ns
	V_{OUT} = 1.4 V step, delay at 50 ns		12		ns
Slew Rate	V_{OUT} = 1.4 V step, delay at 0 ns		500		V/µs
	V_{OUT} = 1.4 V step, delay at 50 ns		400		V/µs
Overshoot	V_{OUT} = 1.4 V step, delay at 0 ns		5	10	%
	V_{OUT} = 1.4 V step, delay at 50 ns				%
Gain	Over All Codes				V/V
Channel-to-Channel Gain Matching	Over All Codes, Among All Channels				%
Hostile Crosstalk	Measured R-to-B at 1MHz, V_{OUT}=1.4 V_{P-P}		-80		dB
Settling Time, Delay Setting Change	Time to settle to 1% after last clock edge				ns
VIDEO INPUT CHARACTERISTICS					
Input Bias Current	R_{IN}, G_{IN}, B_{IN}		1	5	µA
Input Voltage Range	R_{IN}, G_{IN}, B_{IN}		-1/1		V
Input Resistance	R_{IN}, G_{IN}, B_{IN}		10		M Ω
VIDEO OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_{OUT}, G_{OUT}, B_{OUT}				V
Output Current	R_{OUT}, G_{OUT}, B_{OUT}		20		mA
Integrated Output Noise	R_{OUT}, G_{OUT}, B_{OUT}		2.5		mV_{rms}
Output Offset Voltage	R_{OUT}, G_{OUT}, B_{OUT}, Over All Delay Settings	-30	0	30	mV
Channel-to-Channel Output Offset Voltage Matching	Over All Codes, Among All Channels				mV
Output Impedence	R_{OUT}, G_{OUT}, B_{OUT}, $\overline{PD}$ high		4		Ω
	R_{OUT}, G_{OUT}, B_{OUT}, $\overline{PD}$ low		1		M Ω
ANALOG CONTROL INPUT CHARACTERISTICS					
Input Bias Current	V_{CR}, V_{CG}, V_{CB}				µA
Recommend Operating Range	V_{CR}, V_{CG}, V_{CB}		0 to 2		V
Input Offset Voltage	V_{CR}, V_{CG}, V_{CB} Required To Move First Delay Step				V
Maximum Delay Saturation Voltage	V_{CR}, V_{CG}, V_{CB} at Which Maximum Delay is Reached				V
Delay Voltage Step Size in Linear Range	ΔV_{CR}, ΔV_{CG}, ΔV_{CB} to Move one Delay LSB				mV
DIGITAL CONTROL INPUT CHARACTERISTICS					

Parameter	Conditions/Comments	Min	Typ	Max	Unit
Input Bias Current	SDO/SDA, SCK/SCL, SDI, $\overline{CS}$, SER_SEL, MODE				µA
Input High Voltage	SDO/SDA, SCK/SCL, SDI, $\overline{CS}$, SER_SEL, MODE				V
Input Low Voltage	SDO/SDA, SCK/SCL, SDI, $\overline{CS}$, SER_SEL, MODE				V
Output High Voltage	SDO/SDA, SCK/SCL, SDI, $\overline{CS}$, SER_SEL, MODE				V
Output Low Voltage	SDO/SDA, SCK/SCL, SDI, $\overline{CS}$, SER_SEL, MODE				V
Minimum Input Slew Rate	SCK/SCL				V/µs
Setup Time	SDI to SCK, SDA (in) to SCL				
Hold Time	SDI to SCK, SDA (in) to SCL				
Clock Frequency	SCK/SCL				
Clock Pulse Width	SCK/SCL				
POWER DOWN ($\overline{PD}$)					
Input Bias Current	Powered Down				
	Enabled				
Input Voltage	Powered Down				
	Enabled				
Assert Time					
De-Assert Time					
POWER SUPPLY					
Positive Supply Range		4.5		5.5	V
Negative Supply Range		-5.5		-4.5	V
Quiescent Positive Supply Current	Delay = 0 ns				mA
	Delay = 50 ns				mA
	Powered Down, $\overline{PD}$ = Low				
Quiescent Negative Supply Current	Delay = 0 ns				mA
	Delay = 50 ns				mA
	Powered Down, $\overline{PD}$ = Low				
Supply Current Drift	T_{MIN} to T_{MAX}				mA/°C
+PSRR	R_L = 150 Ω				dB
-PSRR	R_L = 150 Ω				dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
Power Dissipation	See Figure 3
Common-Mode Input Voltage	VEE – 0.5 V to VCC + 0.5 V
Differential Input Voltage	1.8 V
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Figure 2

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
5 mm × 5 mm, 32-Lead LFCSP	TBD	TBD	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4410-6 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4410-6. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Power dissipated due to load drive depends upon the particular application. It is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow will increase heat dissipation effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

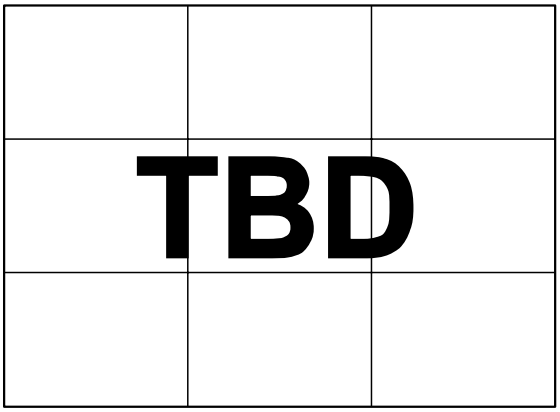

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

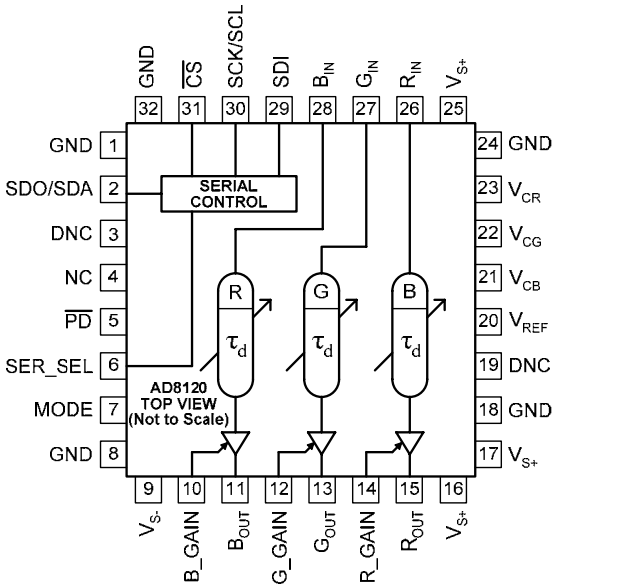

Figure 4. 32-Lead LFCSP Pin Configuration, Top View

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground
2	SDO/SDA	Serial Data Output for SPI Bus/Bi-Directional Serial Data Line for I^2C Bus
3	DNC	Do Not Connect
4	NC	No Internal Connection
5	$\overline{PD}$	Power Down
6	SER_SEL	Selection Between SPI and I^2C Serial Buses. I^2C=0, SPI=1
7	MODE	Selection Between Analog and Digital Control Modes. Digital=0, Analog=1
8, 18, 24	GND	Ground
9	V_{S-}	Negative Power Supply. Connect to -5V
10	B_GAIN	Blue Channel Gain of 2 if tied to GND or 1 if NC
11	B_{OUT}	Blue Channel Video Output
12	G_GAIN	Green Channel Gain of 2 if tied to GND or 1 if NC
13	G_{OUT}	Green Channel Video Output
14	R_GAIN	Red Channel Gain of 2 if tied to GND or 1 if NC
15	R_{OUT}	Red Channel Video Output
16, 17, 25	V_{S+}	Positive Power Supply. Connect to +5V
19	DNC	Do Not Connect
20	V_{REF}	Internal Reference Bypass
21	V_{CB}	Analog Delay Control, Blue Channel
22	V_{CG}	Analog Delay Control, Green Channel
23	V_{CR}	Analog Delay Control, Red Channel
26	R_{IN}	Red Channel Video Input
27	G_{IN}	Green Channel Video Input
28	B_{IN}	Blue Channel Video Input
29	SDI	Serial Data Input for SPI Bus
30	SCK/SCL	Serial Clock for SPI Bus/Serial Clock for I^2C Bus
31	$\overline{CS}$	Chip Select for SPI Bus
32	TEST1	Test Pin. Connect to Ground
Exposed Underside Pad		Thermal Plane Connection. Connect to any PCB plane with voltage between V_{S+} and V_{S-}

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, Vs = ±5V, R_L=150 Ω, unless otherwise noted.

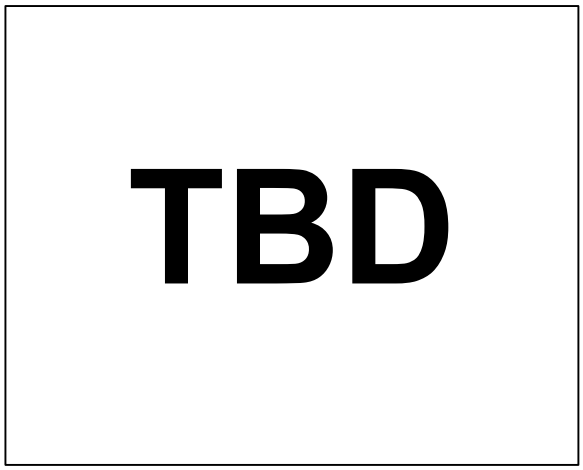

Figure 5. Small Signal Frequency Response for Various Delay Settings

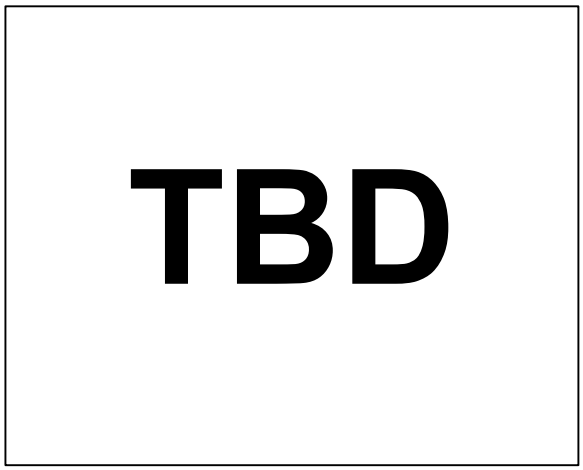

Figure 6. Small Signal Pulse Response for Various Delay Settings

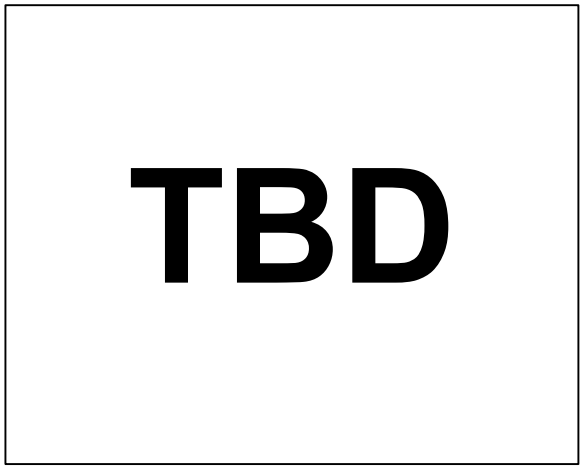

Figure 7. Digital Delay Code vs. Delay

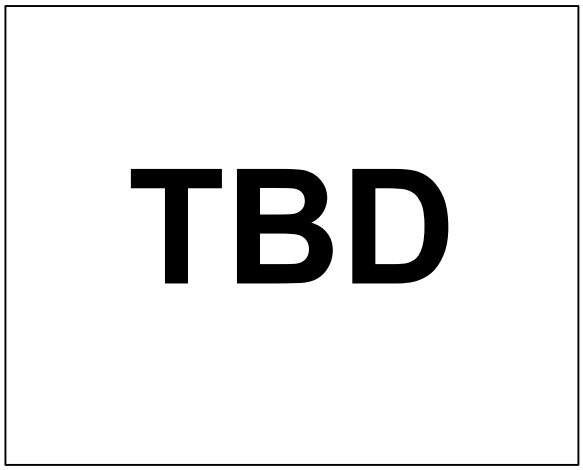

Figure 8. Video Signal Frequency Response for Various Delay Settings

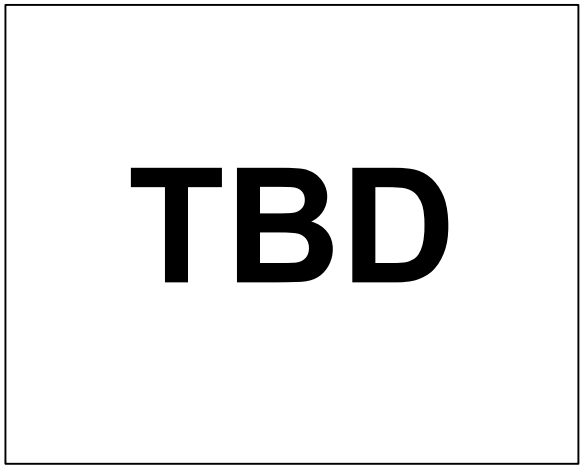

Figure 9. Large Signal Pulse Response for Various Delay Settings

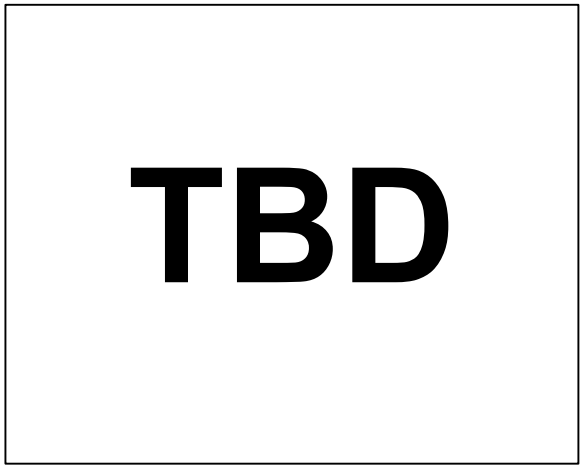

Figure 10. Analog Voltage vs. Delay

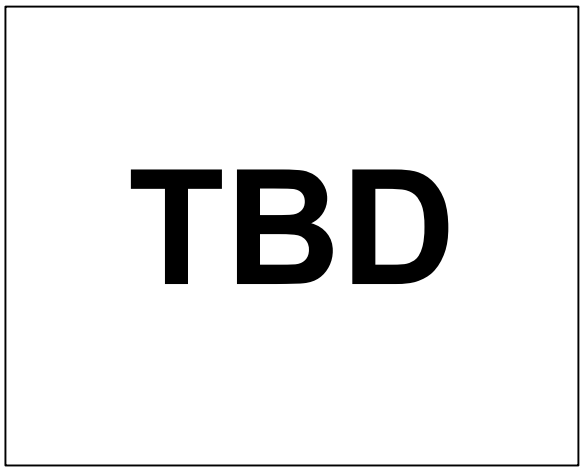

Figure 11. Delay DNL for Digital Control

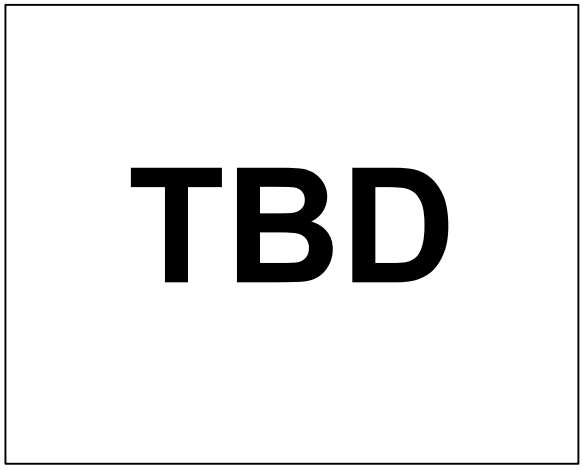

Figure 12. Integrated Output Noise vs. Delay

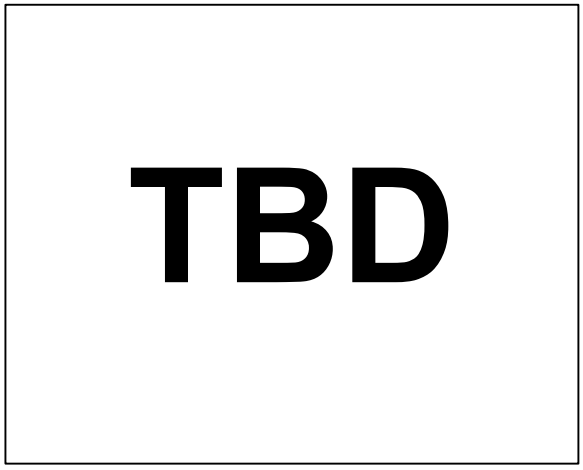

Figure 13. Small Signal Frequency Response for Various Temperatures

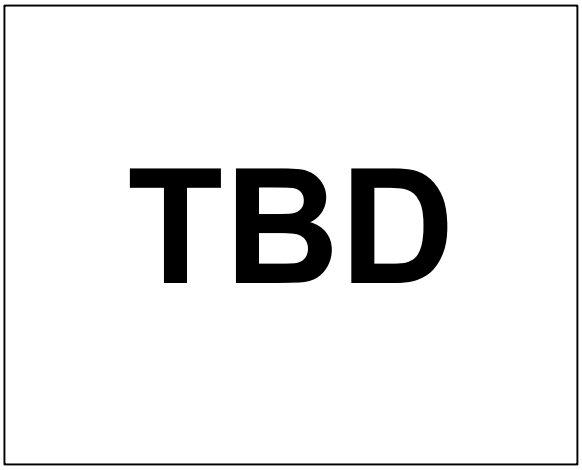

Figure 14. Delay INL for Digital Control

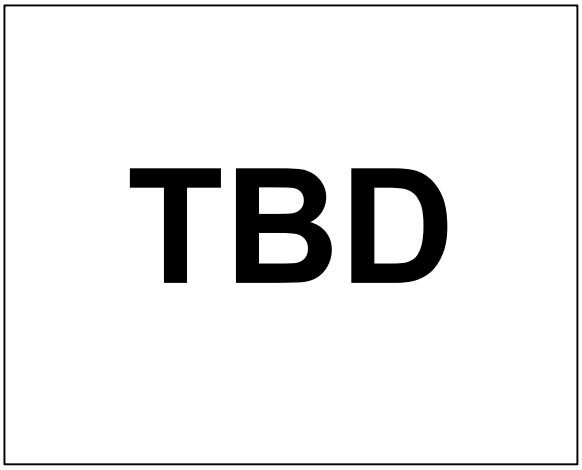

Figure 15. Worst-case Crostalk vs.Frequency

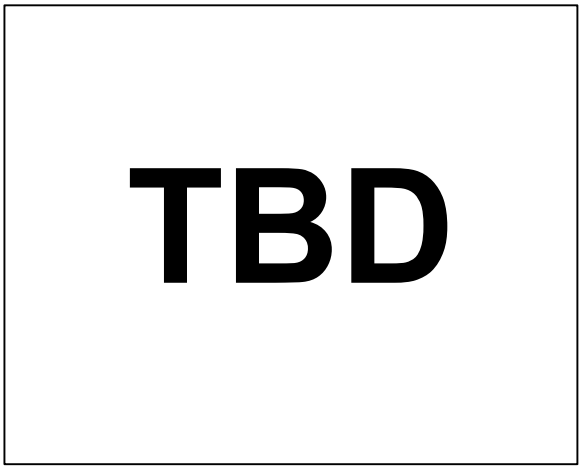

Figure 16. Large Signal Frequency Response for Various Temperatures

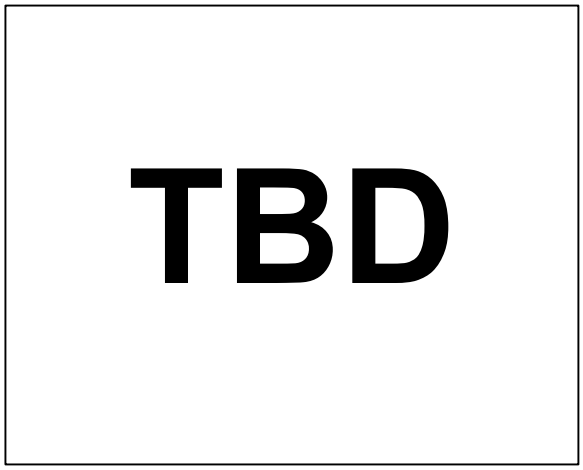

Figure 17. DC Gain Error vs. Delay

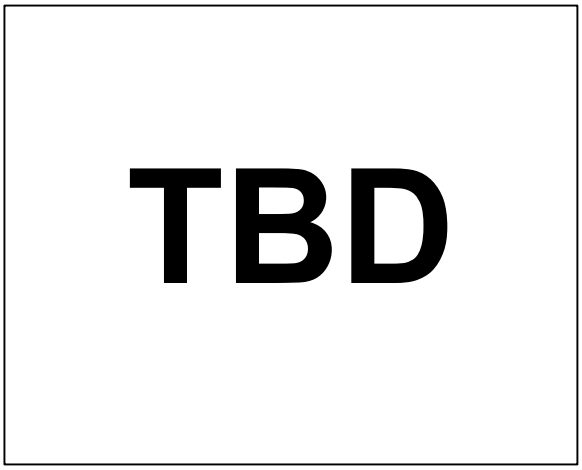

Figure 20. Output Offset vs. Delay

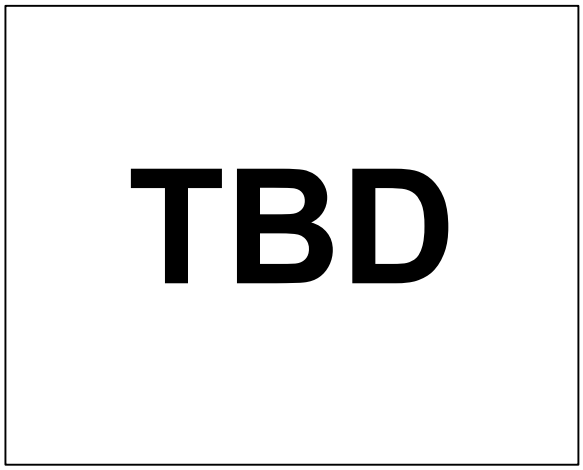

Figure 18. Positive Supply PSRR vs. Frequency

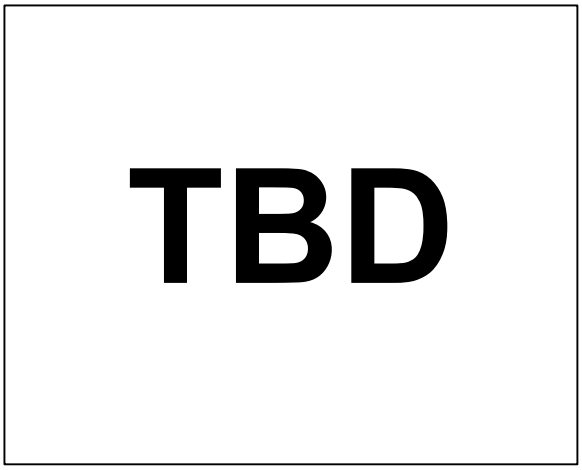

Figure 21. Negative Supply PSRR vs. Frequency

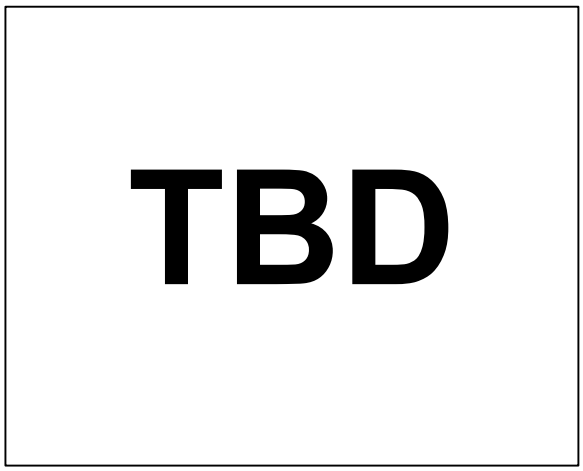

Figure 19. Positive Supply Current vs. Delay

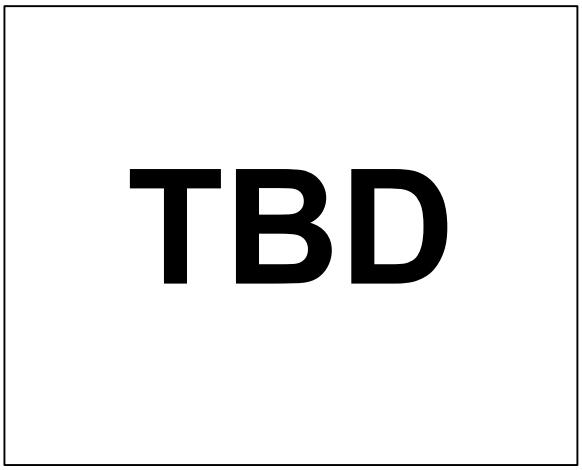

Figure 22. Negative Supply Current vs. Delay

TEST CIRCUITS

THEORY OF OPERATION

APPLICATIONS