8-Bit, 200 MSPS ADC

AD9054A

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/AD9054A

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD9054-703J44	8-Bit, 200 MSPS ADC

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
J44	J	44-Lead ceramic JLCC

3.0 Terminal Connections:

Pin Number	Mnemonic	Pin Number	Mnemonic
1	AIN	23	GND
2	GND	24	VDD
3	VDD	25	DB_0
4	$\overline{DEMUX}$	26	DB_1
5	$\overline{DS}$	27	DB_2
6	DS	28	DB_3
7	ENCODE	29	DB_4
8	$\overline{ENCODE}$	30	DB_5
9	VDD	31	DB_6
10	GND	32	DB_7
11	VDD	33	GND
12	GND	34	VDD
13	DA_7	35	GND
14	DA_6	36	VDD
15	DA_5	37	VDD
16	DA_4	38	GND
17	DA_3	39	VREF OUT
18	DA_2	40	VREF IN
19	DA_1	41	GND
20	DA_0	42	VDD
21	VDD	43	GND
22	GND	44	$\overline{AIN}$

Figure 1 - Terminal connections.

4.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{DD}…….....6V
Analog Inputs.....V_{DD} to 0.0V
Digital Inputs.....V_{DD} to 0.0V
VREF IN, VREF OUT.....V_{DD} to 0.0V
Digital Output Current.....20mA
Operating Temperature.....-55°C to +125°C
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature.....+150°C
Maximum Case Temperature .....+150°C

NOTES

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

4.1 Thermal Characteristics:

Thermal Resistance, 44-lead JLCC Package

Junction-to-Case (Θ_{JC}) = 10°C/W Max
Junction-to-Ambient (Θ_{JA}) = 49°C/W Max

4.2 Electrical Table:

Table I

Parameter See notes at end of table	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
DC Accuracy						
Differential Nonlinearity	DNL		1 2,3	-1 -1	+1.5 +2.0	LSB
Integral Nonlinearity	INL		1 2,3		±1.5 ±2.0	LSB
No Missing Codes		Guaranteed				
Gain Error	A_e	2/ 8/	1 2,3		±7.0 ±9.0	% FS
Analog Input						
Input Offset Voltage	V_{os}		1 2,3		±16 ±23	mV
Input Resistance	R_{in}	 8/	1 2,3	36 23		kΩ
Input Bias Current	I_b		1 2,3		50 75	µA
Reference Output						
Output Voltage	V_{REF}	8/	1,2,3	2.4	2.6	V

Switching Performance						
Maximum Conversion Rate	F_s		1,2,3	200		MSPS
Output Valid Time	t_v	3/, 9/	7	2.7		ns
Output Propagation Delay	t_{PD}	3/, 9/	7		7.9	ns
Digital Inputs						
HIGH Level Current	I_{IH}	4/, 8/	1,2,3		625	µA
LOW Level Current	I_{IL}	4/, 8/	1,2,3		625	µA
Digital Outputs						
HIGH Output Voltage	V_{OH}	9/	1,2,3	2.4		V
LOW Output Voltage	V_{OL}	9/	1,2,3		0.4	V
Power Supply						
V_{DD} Supply Current	I_{DD}	8/	1,2,3		156	mA
Power Dissipation	P_D	5/	1		781	mW
Power Supply Sensitivity	P_{SS}	6/	1		15	mV/V
Dynamic Performance		7/				
Signal-to-Noise Ratio (Without Harmonics)	SNR	f_{IN} = 49.7MHZ f_{IN} = 70.1MHZ	9 9	42 42		dB
Signal-to-Noise Ratio (With Harmonics)	SINAD	f_{IN} = 49.7MHZ f_{IN} = 70.1MHZ	9 9	40 39		dB
Effective Number of Bits	ENOB	f_{IN} = 49.7MHZ f_{IN} = 70.1MHZ	9 9	6.35 6.18		Bits
2^{nd} Harmonic Distortion	2HD	f_{IN} = 49.7MHZ f_{IN} = 70.1MHZ	9 9	54 49		dBc
3^{rd} Harmonic Distortion	3HD	f_{IN} = 49.7MHZ f_{IN} = 70.1MHZ	9 9	48 43		dBc

TABLE I NOTES:

1/ V_{DD} = 5 V, external reference, f_s = max unless otherwise noted.

2/ Gain error and gain temperature coefficient are based on the ADC only (with a fixed 2.5 V external reference)

3/ t_v and t_{PD} are measured from the threshold crossing of the ENCODE input to valid TTL levels of the digital outputs. The output ac load during test is 5 pF.

4/ I_{IH} and I_{IL} are valid for differential input voltages of less than 1.5V. At higher differential voltages, the input current will increase to a maximum of 1.5 mA at 25°C and 2.0 mA @ -55°C and 125°C

5/ Power dissipation is measured under the following conditions: analog input is -1 dBFS at 19.7 MHz.

6/ A change in input offset voltage with respect to a change in V_{DD}.

7/ SNR/harmonics based on an analog input voltage of -1.0 dBFS referenced to a 1.024 V full-scale input range.

8/ 100% production tested at 25°C; guaranteed by design and characterization testing for full mil temperature range.

9/ Go/No-Go parameter only, no read and record data available.

4.3 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 7, 9 1/ 2/ 3/
Group A Test Requirements	1, 2, 3, 7, 9 3/
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1

1/ PDA applies to subgroup 1 only. Delta's excluded from PDA.
2/ See Table III for delta parameters. See Table I for test conditions.
3/ Table I parameters with Note 8/ are 100% production tested at 25°C; guaranteed by design and characterization testing for full mil temperature range.

4.4 Table III - Life Test Endpoint and Delta Parameter (Product is tested in accordance with Table I with the following exceptions)

Parameter	Symbol	Sub-groups	Post Burn In Limit	Burn In Delta	Post Life Test Limit	Life Test Delta	Units
			Max		Max		
V_{DD} Supply Current	I_{DD}	1	156	-	171.6	±15.6	mA
Input Offset Voltage	V_{os}	1	±23	±7	±30	±7	mV
Gain Error	A_e	1	±9	±2	±13	±4	%FS

5.0 MIL-STD-38535 QMLV exceptions:

5.1 Full WLA per MIL-STD-883 TM 5007 is not available for this product fabricated in a QMLQ wafer process facility. SEM Inspection only is available per MIL-STD-883, TM2018.

Rev	Description of Change	Date
A	Initiate	10/18/2004
B	Typical values for Dynamic Performance for subgroup 10 & 11 deleted	06/15/2005
C	Clarify SEM vs. WLA availability for QMLQ fab process	11/12/2007