



Dual, Low Power, Wideband, Low Noise, Rail-to-Rail Output Operational Amplifier

ADA4692-2

FEATURES

Low power: 200 μ A typical, 250 μ A maximum
Low distortion: 0.003% THD + N
Low noise: 16 nV/ $\sqrt{\text{Hz}}$ typical
3.9 MHz bandwidth
Slew rate: 1.4 V/ μ s typical
Offset voltage: 500 μ V typical
Low offset voltage drift: 4 μ V/ $^{\circ}$ C maximum
Very low input bias currents: 0.5 pA typical
2.7 V to 5 V single supply or $\pm$ 1.35 V to $\pm$ 2.5 V dual supply

APPLICATIONS

Portable audio: MP3, PDA, smart phone, notebook
Portable instrumentation
Portable medical devices
Photodiode amplifier
Sensor amplifier
Low-side current sense
ADC driver
Active filter
Sample-and-hold
Automotive sensors

GENERAL DESCRIPTION

The ADA4692-2 is a dual, rail-to-rail output, single-supply amplifier featuring low power, wide bandwidth, and low noise ideal for a wide variety of applications. Audio preamps, filters, IR/photodiode amplifiers, charge amps, and high impedance sensors all benefit from this combination of performance features.

Applications for these amplifiers include consumer audio personal players with low noise and low distortion that provide

PIN CONFIGURATION

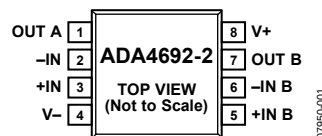


Figure 1. 8-Lead SOIC_N (R-8)

enough gain and slew rate response over the audio band at low power. Industrial applications with high impedance sensors, such as pyroelectric sensors and other IR sensors, benefit from the high impedance input, low offset drift, and enough bandwidth and response for low gain applications.

The ADA4692-2 is specified over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$). The ADA4692-2 is a dual op amp available in an 8-lead SOIC package.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Fax: 781.461.3113
www.analog.com
©2009 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	6
Applications.....	1	Thermal Resistance.....	6
Pin Configuration.....	1	ESD Caution.....	6
Revision History	2	Typical Performance Characteristics	7
Specifications.....	3	Outline Dimensions	15
Electrical Characteristics—2.7 V Operation.....	3	Ordering Guide	15
Electrical Characteristics—5 V Operation.....	4		

REVISION HISTORY

3/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

$V_{SY} = 2.7\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	2.5 3.5	mV mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5 325	pA pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	5 225	pA pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+1.6	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	70	90		dB dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to }2.2\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	90	100		dB dB dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$R_L = 600\ \Omega$, $V_{OUT} = 0.5\text{ V to }2.2\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	85	95		dB dB
Input Capacitance	C_{IN}			0.6	3	$\mu\text{V}/^\circ\text{C}$
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65 2.6	2.67		V V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.55 2.5	2.59		V V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ to V_{SY} $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		24	30	mV mV
		$R_L = 600\ \Omega$ to V_{SY} $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		78	95	mV mV
Short-Circuit Current	I_{SC}	$V_{OUT} = V_{SY}$ or GND		± 15	125	mV mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_v = -100$		372		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80 75	90		dB dB
Supply Current Per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		165	200 225	μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 600\ \Omega$, $C_L = 20\text{ pF}$, $A_v = +1$		1.1		V/ μs
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $C_L = 20\text{ pF}$, $A_v = +1$		1.4		V/ μs
Settling Time to 0.1%	t_s	Step = 0.5 V, $R_L = 2\text{ k}\Omega$, 600 Ω		1		μs
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_v = +1$		3.9		MHz
Phase Margin	Φ_M	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_v = +1$		49		Degrees

ADA4692-2

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Distortion	THD + N	$A_V = -1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.15\text{ V rms}$		0.008		%
		$A_V = -1$, $R_L = 600\text{ }\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.15\text{ V rms}$		0.01		%
		$A_V = +1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.15\text{ V rms}$		0.004		%
		$A_V = +1$, $R_L = 600\text{ }\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.15\text{ V rms}$		0.005		%
Voltage Noise	e_n p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$		3.1		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		13		$\text{nV}/\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3\text{ V to }+3.9\text{ V}$		0.5	2.5	mV
		$V_{CM} = -0.1\text{ V to }+3.9\text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			3.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5	pA
					360	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	5	pA
					260	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+3.9	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\text{ V to }+3.9\text{ V}$	75	98		dB
		$V_{CM} = -0.1\text{ V to }+3.9\text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$, $V_{CM} = 0\text{ V}$	95	110		dB
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	90			dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80			dB
		$R_L = 600\text{ }\Omega$, $V_O = 0.5\text{ V to }4.5\text{ V}$, $V_{CM} = 0\text{ V}$	90	100		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4	$\mu\text{V}/^\circ\text{C}$
Input Capacitance						
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$	4.95	4.97		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.9			V
		$R_L = 600\text{ }\Omega$ to GND	4.85	4.88		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.8			V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$		28	35	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			45	mV
		$R_L = 600\text{ }\Omega$		90	110	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			140	mV
Short-Circuit Limit	I_{SC}	$V_{OUT} = V_{SY}$ or GND		± 55		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = -100$		344		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }5.5\text{ V}$	80	90		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	75			dB
Supply Current per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$		175	225	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			250	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $600\text{ }\Omega$, $C_L = 20\text{ pF}$, $A_V = +1$		1.3		V/ μ s
Settling Time to 0.1%	t_s	$V_{IN} = 2\text{ V}$ step, $R_L = 2\text{ k}\Omega$, $600\text{ }\Omega$		1.5		μ s
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_V = +1$		3.6		MHz
Phase Margin	Φ_M	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_V = +1$		52		Degrees
NOISE PERFORMANCE						
Distortion	THD + N	$A_V = -1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.008		%
		$A_V = -1$, $R_L = 600\text{ }\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.006		%
		$A_V = +1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.003		%
		$A_V = +1$, $R_L = 600\text{ }\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.001		%
Voltage Noise	e_n p-p	$f = 0.1\text{ Hz}$ to 10 Hz		3.2		μ V p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		16		nV/ $\sqrt{\text{Hz}}$
	e_n	$f = 10\text{ kHz}$		13		nV/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Input Current ¹	±10 mA
Differential Input Voltage ²	± V_{SY}
Output Short-Circuit Duration to GND	Indefinite
Temperature	
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

¹ Input pins have clamp diodes to the supply pins. Limit the input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.3 V.
² Differential input voltage is limited to 5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages and measured using a standard 2-layer board, unless otherwise specified.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	158	43	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

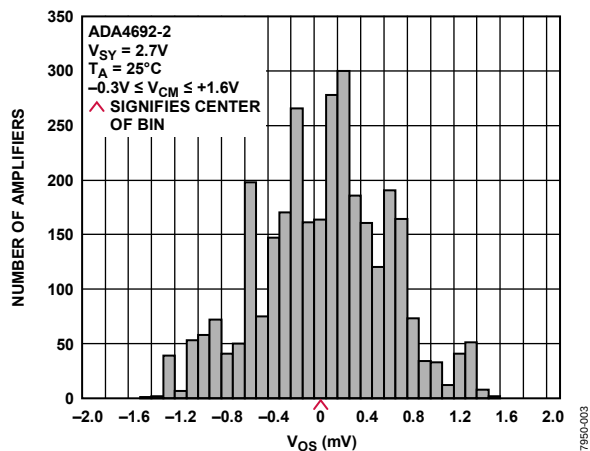


Figure 2. Input Offset Voltage Distribution

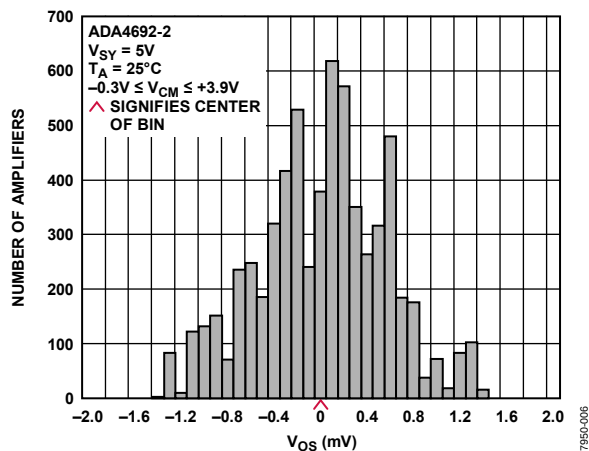


Figure 5. Input Offset Voltage Distribution

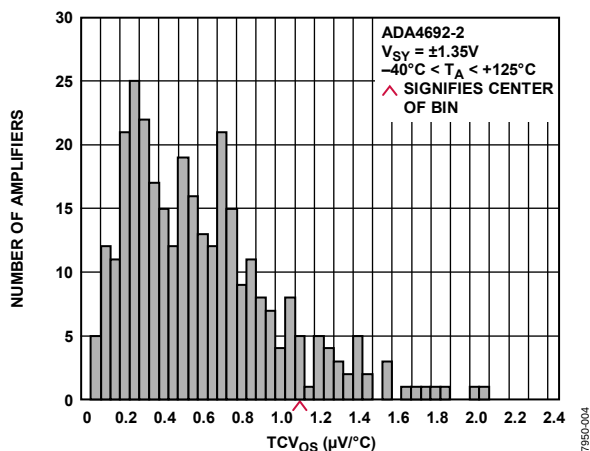


Figure 3. Input Offset Voltage Drift Distribution

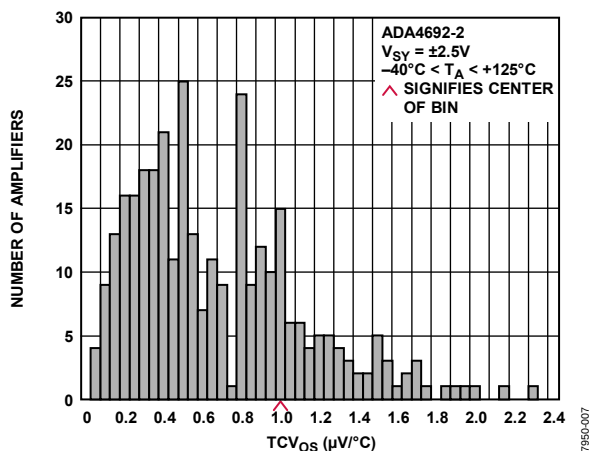


Figure 6. Input Offset Voltage Drift Distribution

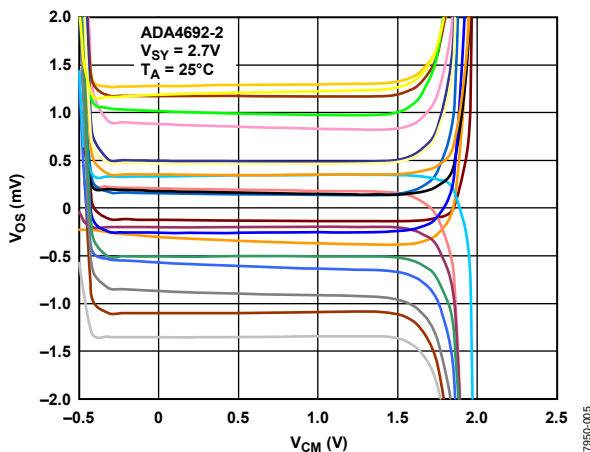


Figure 4. Input Offset Voltage vs. Common-Mode Voltage

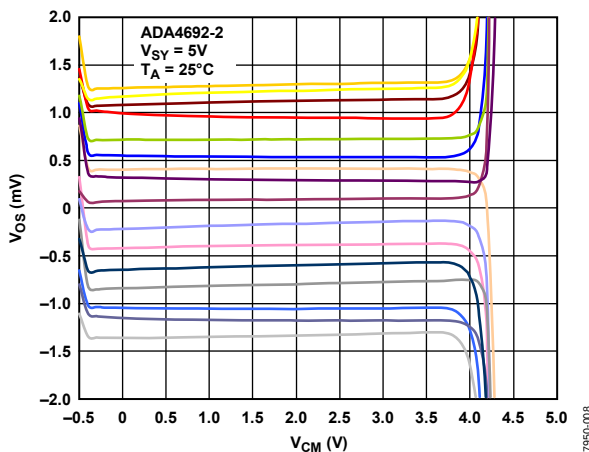


Figure 7. Input Offset Voltage vs. Common-Mode Voltage

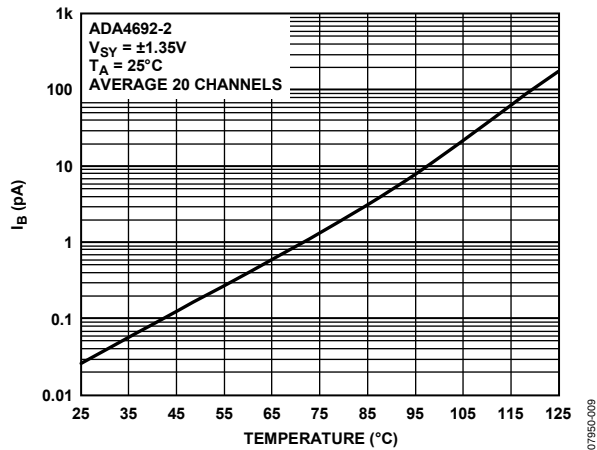


Figure 8. Input Bias Current vs. Temperature

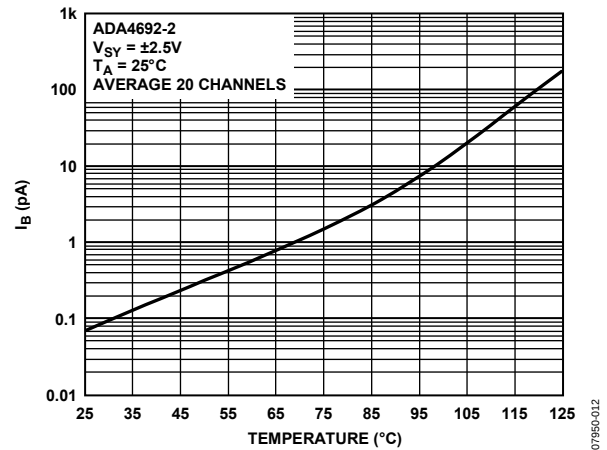


Figure 11. Input Bias Current vs. Temperature

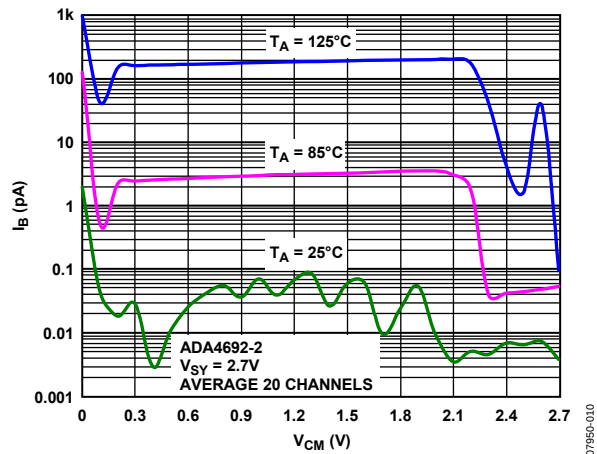


Figure 9. Input Bias Current vs. Common-Mode Voltage

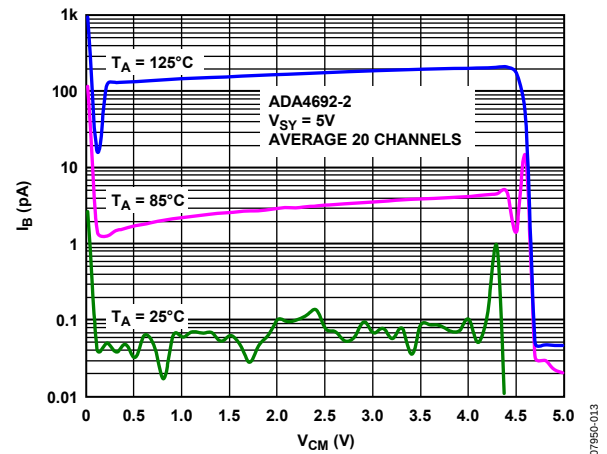


Figure 12. Input Bias Current vs. Common-Mode Voltage

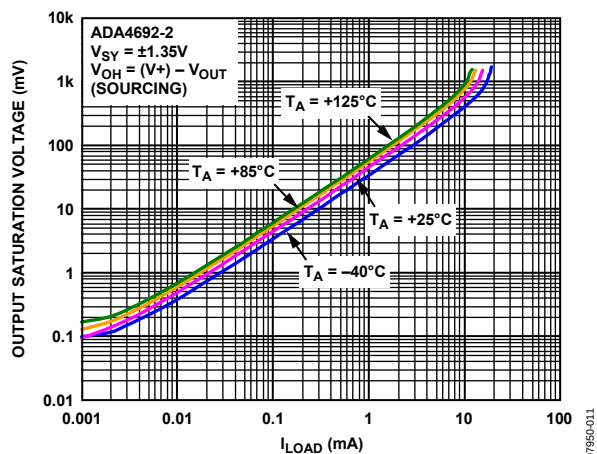


Figure 10. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

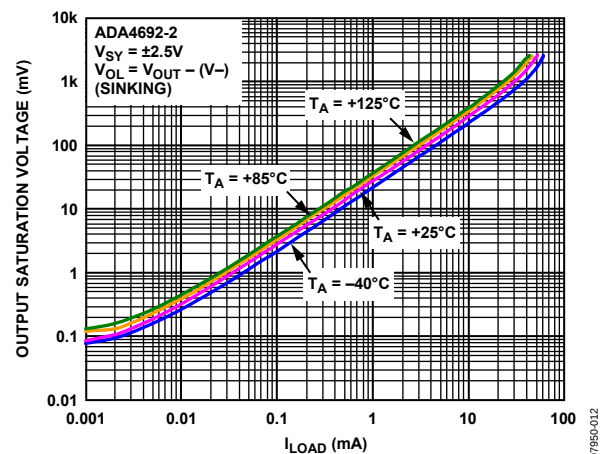


Figure 13. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

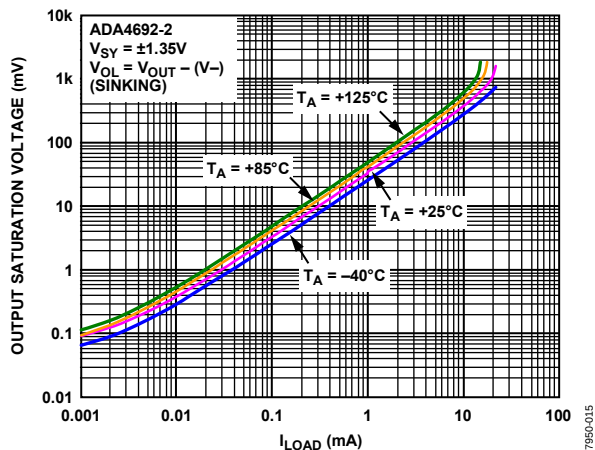


Figure 14. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

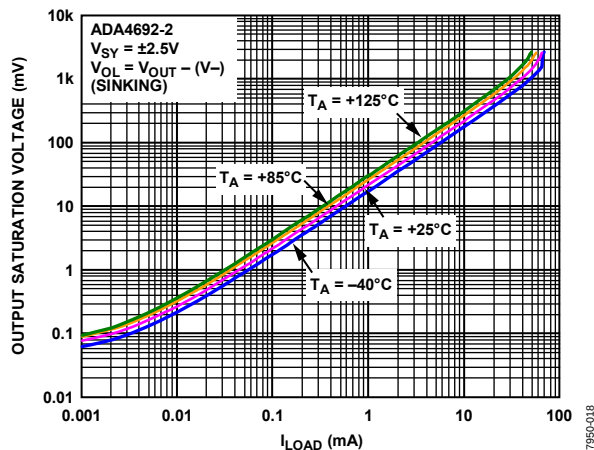


Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

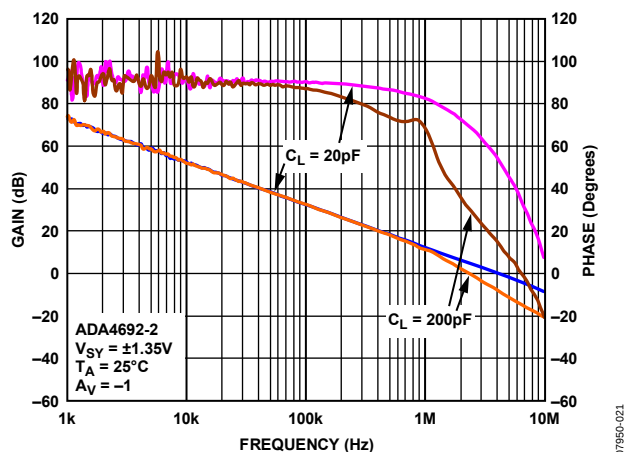


Figure 15. Open-Loop Gain and Phase vs. Frequency

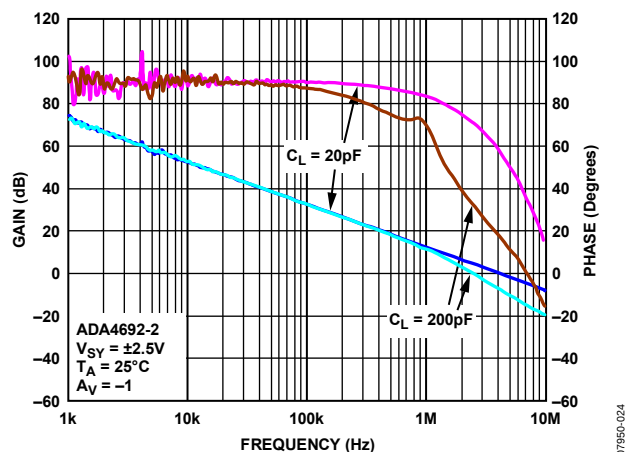


Figure 18. Open-Loop Gain and Phase vs. Frequency

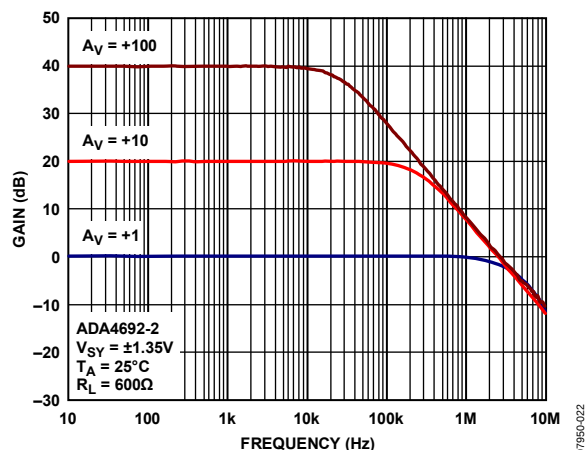


Figure 16. Closed-Loop Gain vs. Frequency

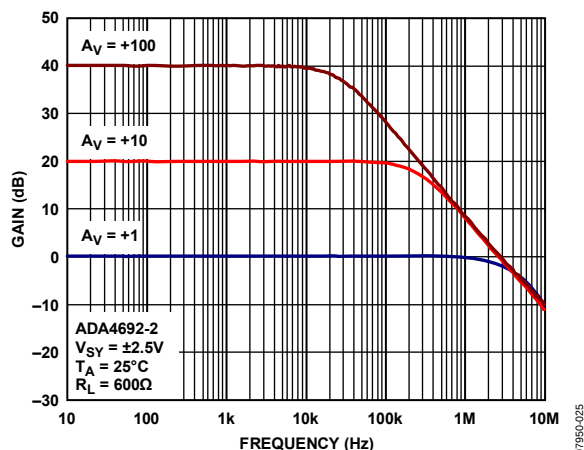


Figure 19. Closed-Loop Gain vs. Frequency

ADA4692-2

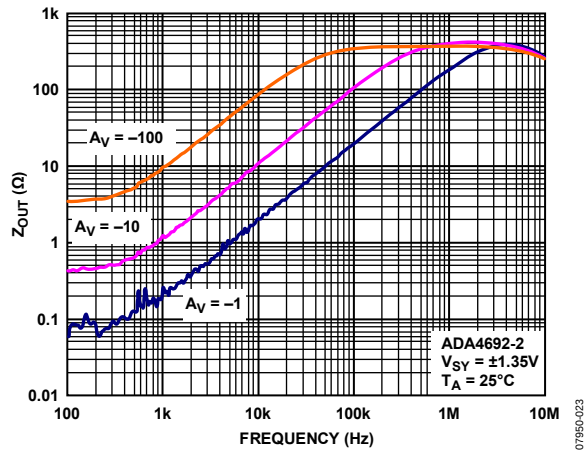


Figure 20. Output Impedance vs. Frequency

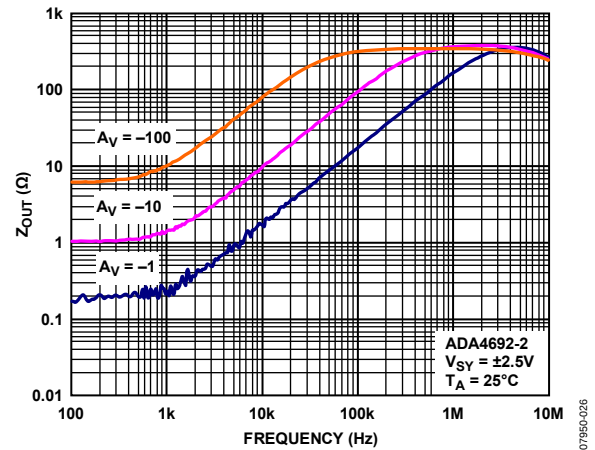


Figure 23. Output Impedance vs. Frequency

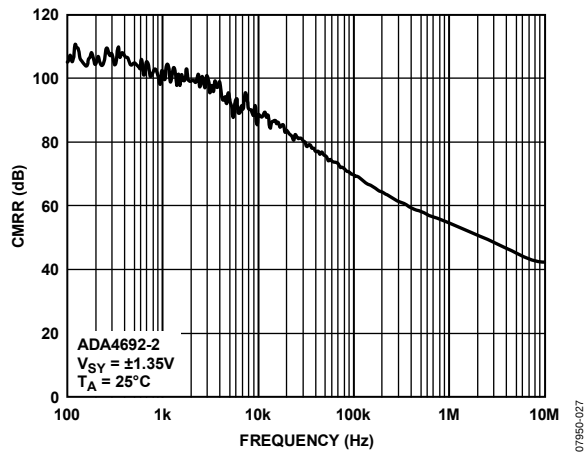


Figure 21. CMRR vs. Frequency

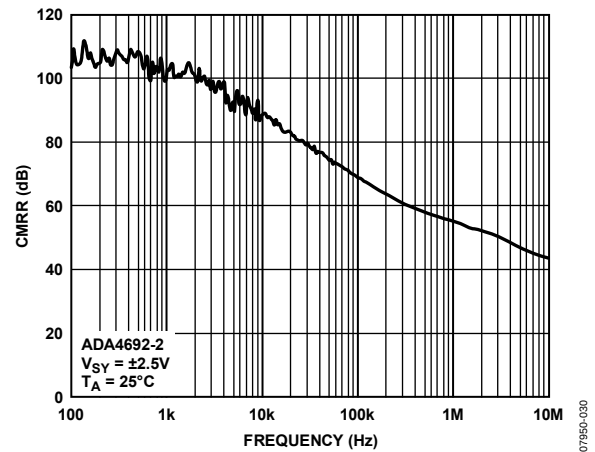


Figure 24. CMRR vs. Frequency

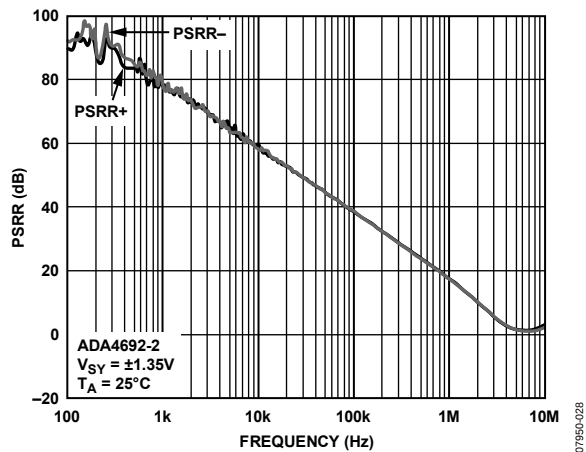


Figure 22. PSRR vs. Frequency

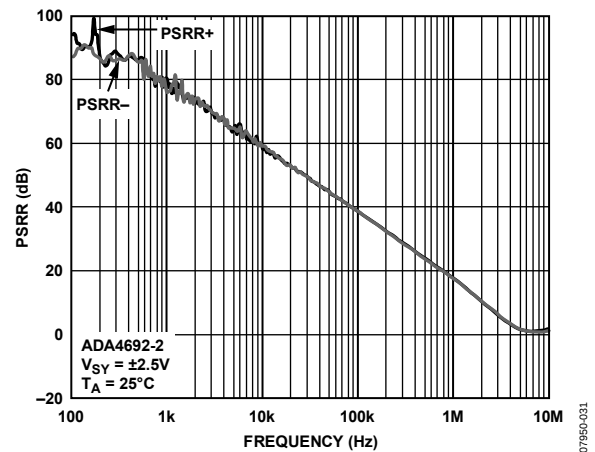


Figure 25. PSRR vs. Frequency

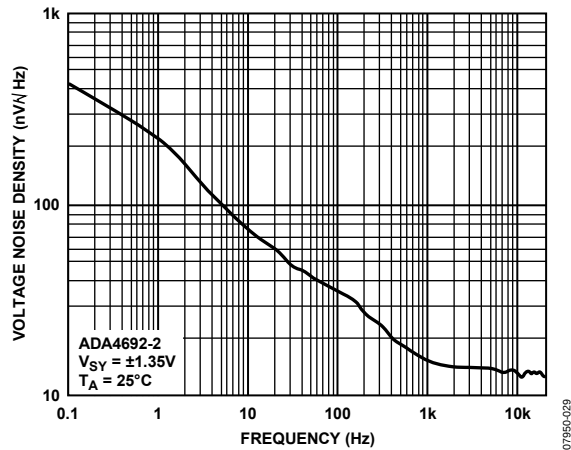


Figure 26. Voltage Noise Density vs. Frequency

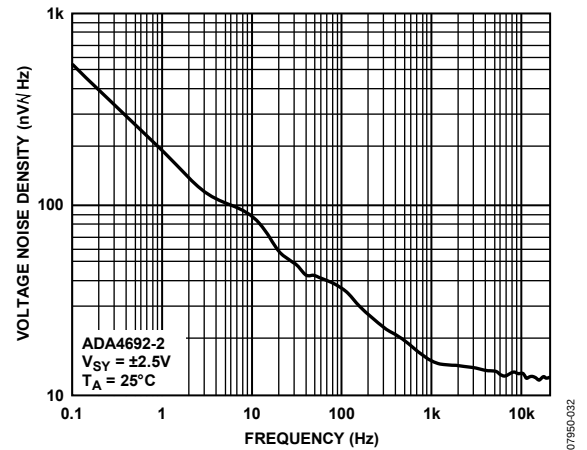


Figure 29. Voltage Noise Density vs. Frequency

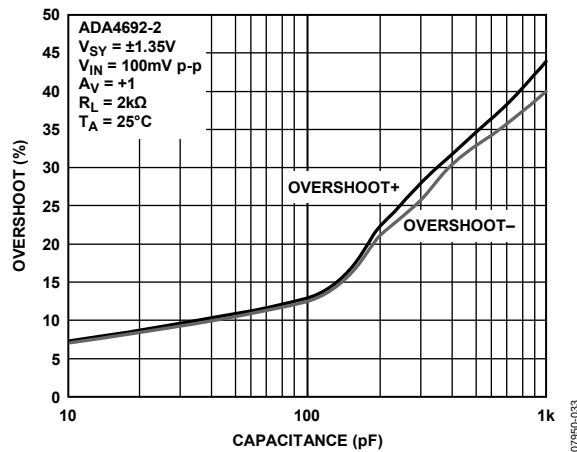


Figure 27. Small Signal Overshoot vs. Load Capacitance

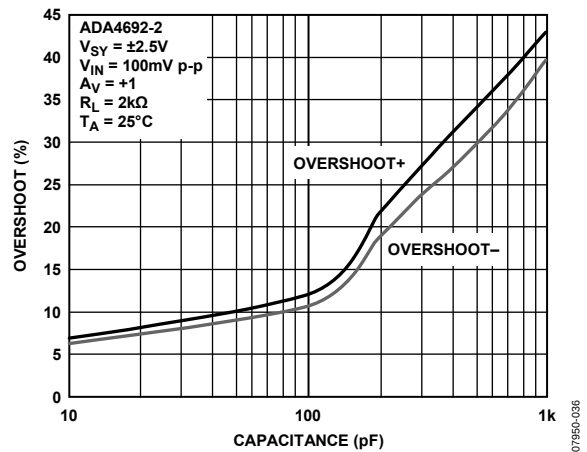


Figure 30. Small Signal Overshoot vs. Load Capacitance

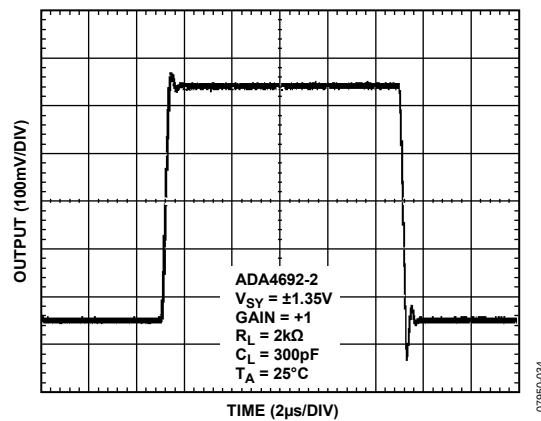


Figure 28. Large Signal Transient Response

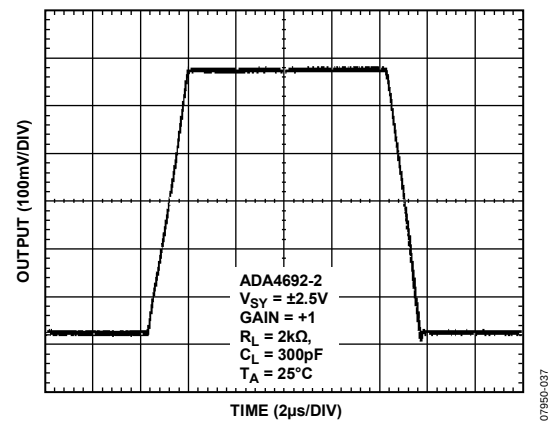


Figure 31. Large Signal Transient Response

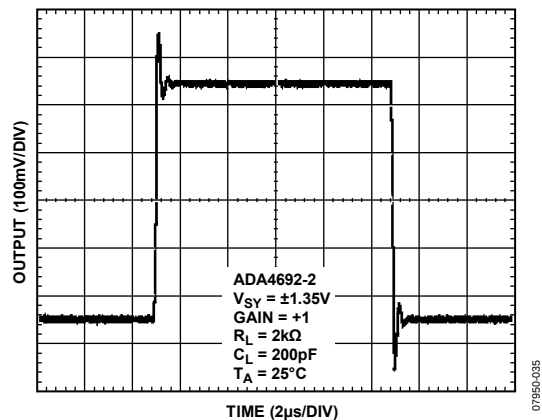


Figure 32. Small Signal Transient Response

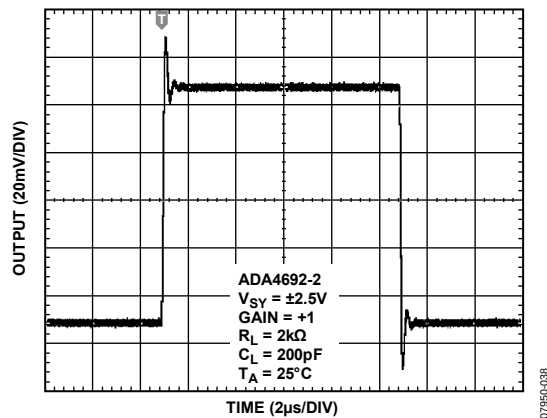


Figure 35. Small Signal Transient Response

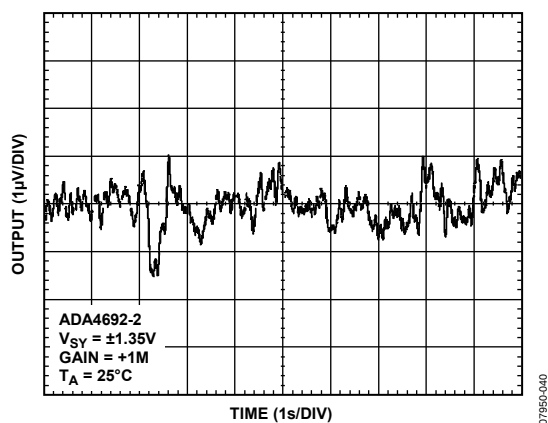


Figure 33. 0.1 Hz to 10 Hz Noise

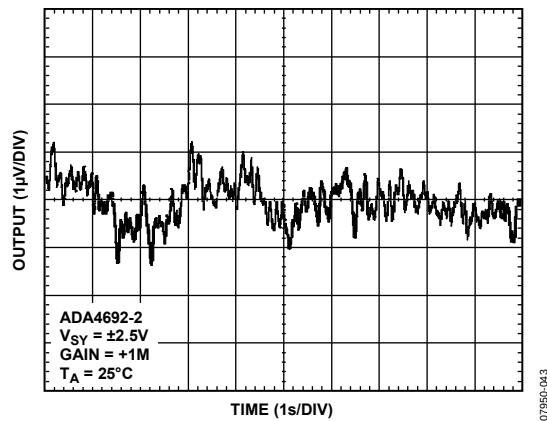


Figure 36. 0.1 Hz to 10 Hz Noise

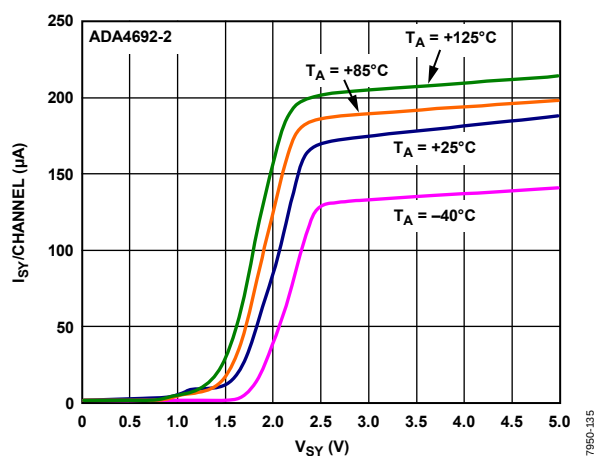


Figure 34. Supply Current per Amplifier vs. Supply Voltage

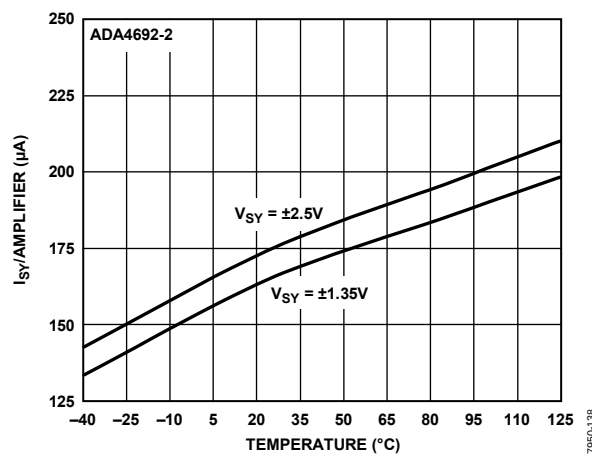


Figure 37. Supply Current per Channel vs. Temperature

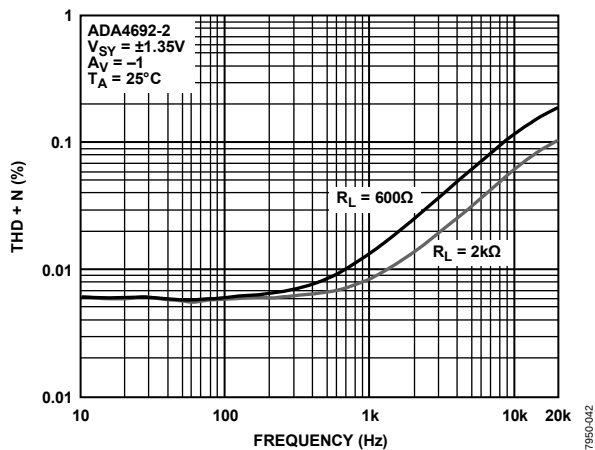


Figure 38. THD + Noise vs. Frequency

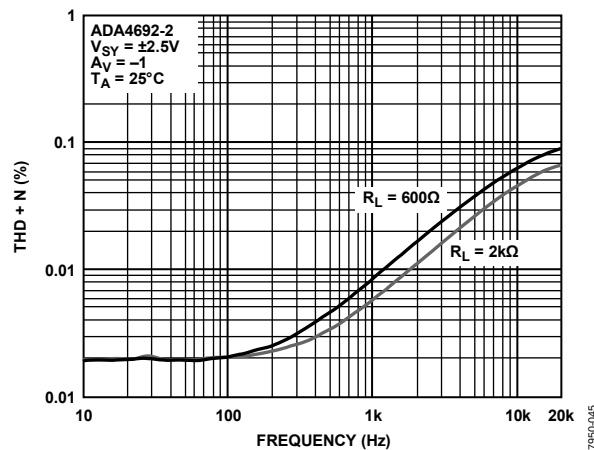


Figure 41. THD + Noise vs. Frequency

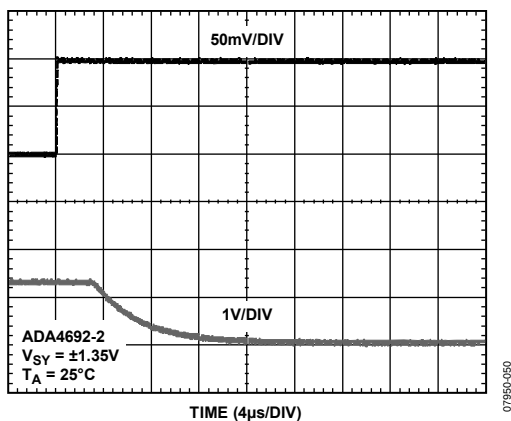


Figure 39. Negative Overload Recovery

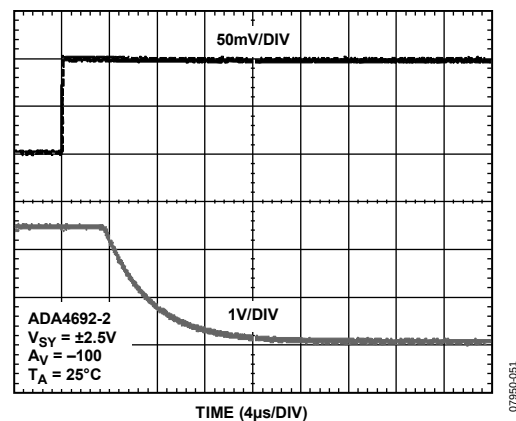


Figure 42. Negative Overload Recovery

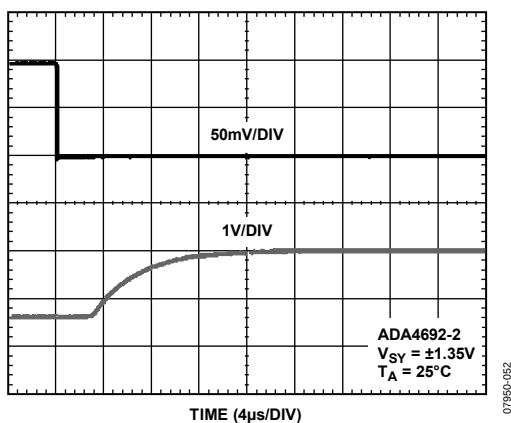


Figure 40. Positive Overload Recovery

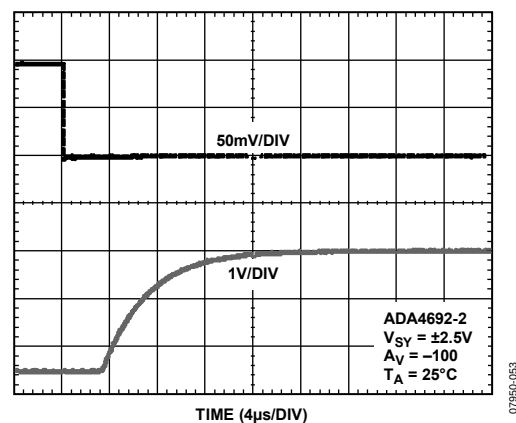
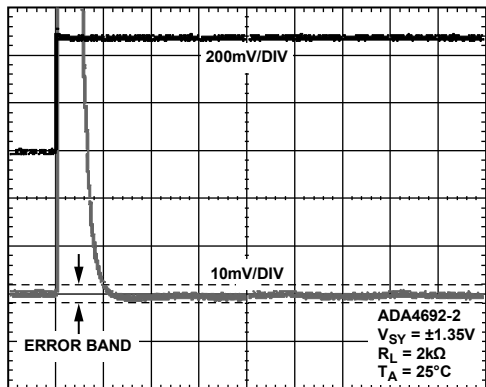
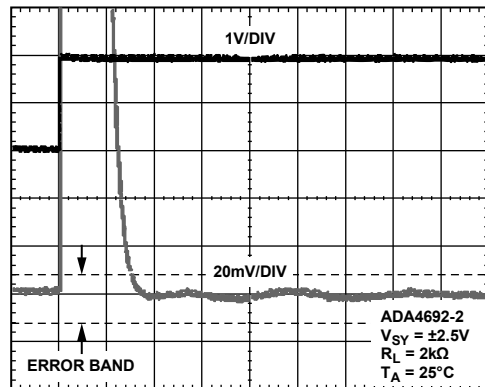


Figure 43. Positive Overload Recovery



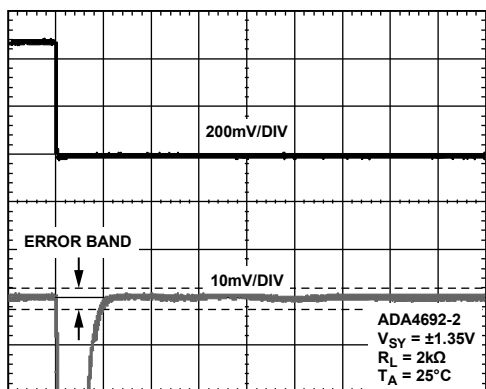
TIME (1μs/DIV)

Figure 44. Positive Settling Time to 0.1%



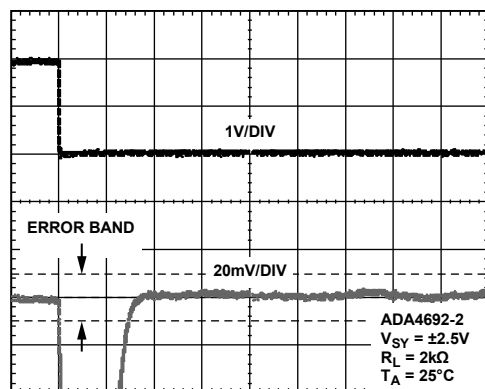
TIME (1μs/DIV)

Figure 47. Positive Settling Time to 0.1%



TIME (1μs/DIV)

Figure 45. Negative Settling Time to 0.1%



TIME (1μs/DIV)

Figure 48. Negative Settling Time to 0.1%

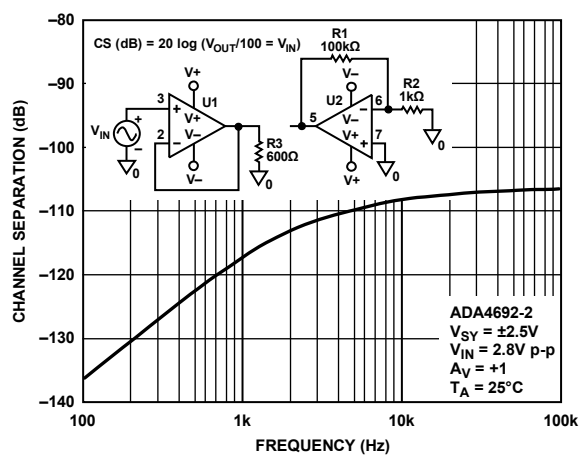
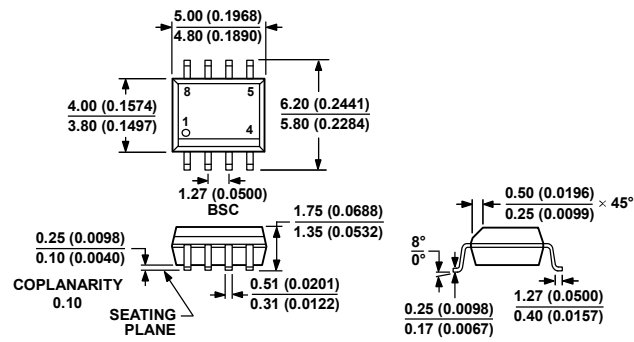


Figure 46. Channel Separation vs. Frequency

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 49. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4692-2ARZ ¹	−40°C to +125°C	8-Lead SOIC_N	R-8
ADA4692-2ARZ-R7 ¹	−40°C to +125°C	8-Lead SOIC_N	R-8
ADA4692-2ARZ-RL ¹	−40°C to +125°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

NOTES