0.5 Ω CMOS 1.65 V to 3.6 V Dual SPDT/2:1 Mux in Mini LFCSP Package

ADG824

FEATURES

0.5 Ω typical on resistance
0.7 Ω maximum on resistance at 85°C
1.65 V to 3.6 V operation
High current carrying capability: 300 mA continuous
Rail-to-rail switching operation
Fast switching times: <20 ns
Typical power consumption: (<0.1 μW)
1.3 mm × 1.6 mm mini LFCSP package

APPLICATIONS

Cellular phones
PDAs
MP3 players
Power routing
Battery-powered systems
PCMCIA cards
Modems
Audio and video signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM

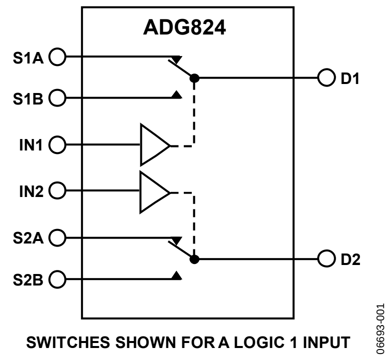

Figure 1.

GENERAL DESCRIPTION

The ADG824 is a low voltage CMOS device containing two independently selectable single-pole, double throw (SPDT) switches. This device offers ultralow on resistance of less than 0.7 Ω over the full temperature range. The ADG824 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG824 exhibits break-before-make switching action.

The low on resistance of the ADG824 makes this device ideal for audio switching. In addition, a data rate of 180 Mbps makes the device suitable for USB low speed (1.5 Mbps) and full speed (12 Mbps) data switching.

The ADG824 is available in a 1.3 mm × 1.6 mm, 10-lead mini LFCSP package.

PRODUCT HIGHLIGHTS

1. <0.7 Ω over the full temperature range of −40°C to +85°C.
2. Single 1.65 V to 3.6 V operation.
3. 1.8 V logic compatible.
4. High current carrying capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.06% typical).
6. 1.3 mm × 1.6 mm mini LFCSP package.

Rev. B

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7/08—Rev. 0 to Rev. A

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4/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.5		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA; see Figure 19
	0.65	0.7	Ω max	
On Resistance Match Between	0.003		Ω typ	V_{DD} = 2.7 V, V_S = 0.65 V, I_{DS} = 100 mA
Channels, ΔR_{ON}		0.02	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.13		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA
		0.2	Ω max	
LEAKAGE CURRENTS				V_{DD} = 3.6 V
Source Off Leakage, I_S (Off)	±0.2		nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; see Figure 20
Channel On Leakage, I_D, I_S (On)	±0.2		nA typ	V_S = V_D = 0.6 V or 3.3 V; see Figure 21
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.35	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	µA max	V_{IN} = V_{GND} or V_{DD}
Digital Input Capacitance, C_{IN}	2.7		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	7		ns typ	R_L = 50 Ω, C_L = 35 pF
	9.5	10.8	ns max	V_S = 2 V/0 V; see Figure 22
t_{OFF}	6		ns typ	R_L = 50 Ω, C_L = 35 pF
	7.7	8.6	ns max	V_S = 2 V; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	3.5		ns typ	R_L = 50 Ω, C_L = 35 pF
		2	ns min	V_{S1} = V_{S2} = 2 V; see Figure 23
Charge Injection, Q_{INJ}	27		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 24
Off Isolation	−71		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 25
Channel-to-Channel Crosstalk	−90		dB typ	S1A to S2A/S1B to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
	−67		dB typ	S1A to S1B/S2A to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion, THD + N	0.06		%	R_L = 33 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p
Insertion Loss	−0.05		dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
−3 dB Bandwidth	90		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
C_S (Off)	25		pF typ	
C_D, C_S (On)	58		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.6 V
I_{DD}	0.003		µA typ	Digital inputs = 0 V or 3.6 V
		1	µA max	

[1] Guaranteed by design; not subject to production test.

V_{DD} = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	0.65		Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA; see Figure 19
	0.78	0.83	Ω max	
On Resistance Match Between Channels, ΔR_{ON}	0.005		Ω typ	V_{DD} = 2.3 V, V_S = 0.7 V, I_{DS} = 100 mA
		0.01	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	0.2		Ω typ	V_{DD} = 2.3 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA
		0.3	Ω max	
LEAKAGE CURRENTS				V_{DD} = 2.7 V
Source Off Leakage, I_S (Off)	±0.2		nA typ	V_S = 0.6 V/2.4 V, V_D = 2.4 V/0.6 V; see Figure 20
Channel On Leakage, I_D, I_S (On)	±0.2		nA typ	V_S = V_D = 0.6 V or 2.4 V; see Figure 21
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.3	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	µA max	V_{IN} = V_{GND} or V_{DD}
Digital Input Capacitance, C_{IN}	2.7		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	9		ns typ	R_L = 50 Ω, C_L = 35 pF
	11.5	12.4	ns max	V_S = 1.5 V/0 V; see Figure 22
t_{OFF}	6		ns typ	R_L = 50 Ω, C_L = 35 pF
	7.4	8	ns max	V_S = 1.5 V; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	5		ns typ	R_L = 50 Ω, C_L = 35 pF
		3	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 23
Charge Injection, Q_{INJ}	21		pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 24
Off Isolation	−71		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 25
Channel-to-Channel Crosstalk	−90		dB typ	S1A to S2A/S1B to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
	−71		dB typ	S1A to S1B/S2A to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion, THD + N	0.1		%	R_L = 33 Ω, f = 20 Hz to 20 kHz, V_S = 1.5 V p-p
Insertion Loss	−0.065		dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
−3 dB Bandwidth	90		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
C_S (Off)	25		pF typ	
C_D, C_S (On)	60		pF typ	
POWER REQUIREMENTS				V_{DD} = 2.7 V
I_{DD}	0.003		µA typ	Digital inputs = 0 V or 2.7 V
		1	µA max	

[1] Guaranteed by design; not subject to production test.

V_{DD} = 1.65 V to 1.95 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance, R_{ON}	1.3		Ω typ	V_{DD} = 1.8 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA; see Figure 19
	1.7	2.1	Ω max	
	2.5	3	Ω max	V_{DD} = 1.65 V, V_S = 0 V to V_{DD}, I_{DS} = 100 mA; see Figure 19
On Resistance Match Between Channels, ΔR_{ON}	0.01		Ω typ	V_{DD} = 1.65 V, V_S = 0.7 V, I_{DS} = 100 mA
LEAKAGE CURRENTS				V_{DD} = 1.95 V
Source Off Leakage, I_S (Off)	±0.2		nA typ	V_S = 0.6 V/1.65 V, V_D = 1.65 V/0.6 V; see Figure 20
Channel On Leakage, I_D, I_S (On)	±0.2		nA typ	V_S = V_D = 0.6 V or 1.65 V; see Figure 21
DIGITAL INPUTS				
Input High Voltage, V_{INH}		0.65 V_{DD}	V min	
Input Low Voltage, V_{INL}		0.35 V_{DD}	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{GND} or V_{DD}
		±0.1	µA max	V_{IN} = V_{GND} or V_{DD}
Digital Input Capacitance, C_{IN}	2.7		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	13		ns typ	R_L = 50 Ω, C_L = 35 pF
	18.6	19.3	ns max	V_S = 1.2 V/0 V; see Figure 22
t_{OFF}	7		ns typ	R_L = 50 Ω, C_L = 35 pF
	9.8	10.2	ns max	V_S = 1.2 V; see Figure 22
Break-Before-Make Time Delay, t_{BBM}	7.5		ns typ	R_L = 50 Ω, C_L = 35 pF
		5	ns min	V_{S1} = V_{S2} = 1.2 V; see Figure 23
Charge Injection, Q_{INJ}	15		pC typ	V_S = 1 V, R_S = 0 Ω, C_L = 1 nF; see Figure 24
Off Isolation	−71		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 25
Channel-to-Channel Crosstalk	−90		dB typ	S1A to S2A/S1B to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
	−71		dB typ	S1A to S1B/S2A to S2B, R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion, THD + N	0.4		%	R_L = 33 Ω, f = 20 Hz to 20 kHz, V_S = 1.2 V p-p
Insertion Loss	−0.1		dB typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
−3 dB Bandwidth	90		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
C_S (Off)	26		pF typ	
C_D, C_S (On)	61		pF typ	
POWER REQUIREMENTS				V_{DD} = 1.95 V
I_{DD}	0.003		µA typ	Digital inputs = 0 V or 1.95 V
		1	µA max	

[1] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4.6 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to +4.6 V or 10 mA, whichever occurs first
Peak Current, Sx or Dx Pins	Pulsed at 1 ms, 10% duty cycle max
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA
Continuous Current, Sx or Dx Pins	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Mini LFCSP Package	
θ_{JA} Thermal Impedance (4-Layer Board)	131.6°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at the INx, Sx, or Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

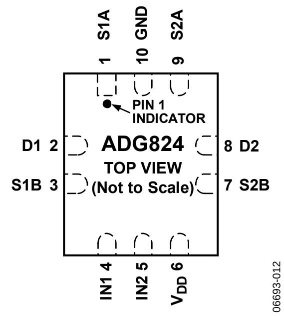

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1A	Source Terminal. This pin can be an input or an output.
2	D1	Drain Terminal. This pin can be an input or an output.
3	S1B	Source Terminal. This pin can be an input or an output.
4	IN1	Logic Control Input. This pin controls Switch S1A and Switch S1B to D1.
5	IN2	Logic Control Input. This pin controls Switch S2A and Switch S2B to D2.
6	V_{DD}	Most Positive Power Supply Potential.
7	S2B	Source Terminal. This pin can be an input or an output.
8	D2	Drain Terminal. This pin can be an input or an output.
9	S2A	Source Terminal. This pin can be an input or an output.
10	GND	Ground (0 V) Reference.

Table 6. ADG824 Truth Table

Logic (IN1/IN2)	Switch A (S1A or S2A)	Switch B (S1B or S2B)
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

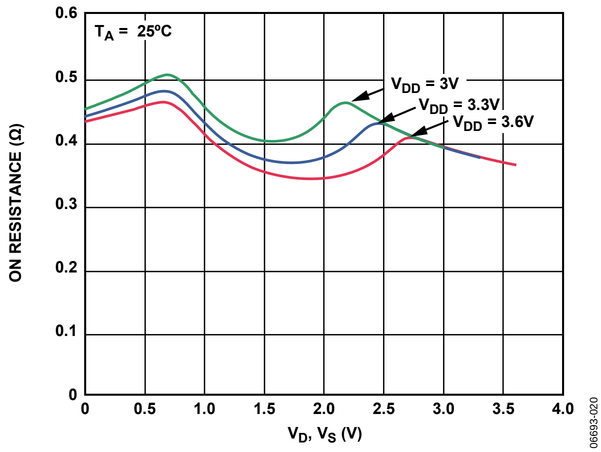

Figure 3. On Resistance vs. V_D (V_S), V_{DD} = 3.3 V ± 0.3 V

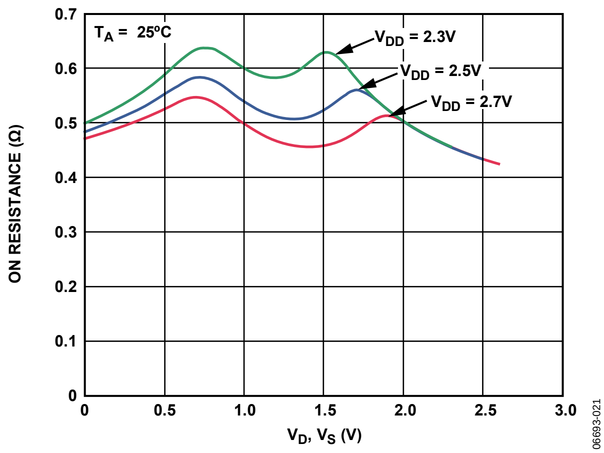

Figure 4. On Resistance vs. V_D (V_S), V_{DD} = 2.5 V ± 0.2 V

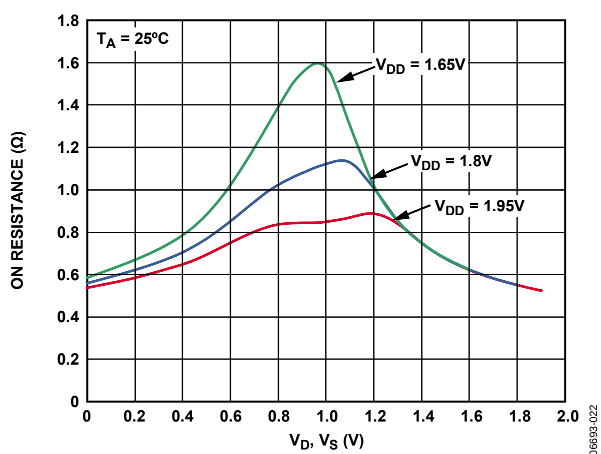

Figure 5. On Resistance vs. V_D (V_S), V_{DD} = 1.8 V ± 0.15 V

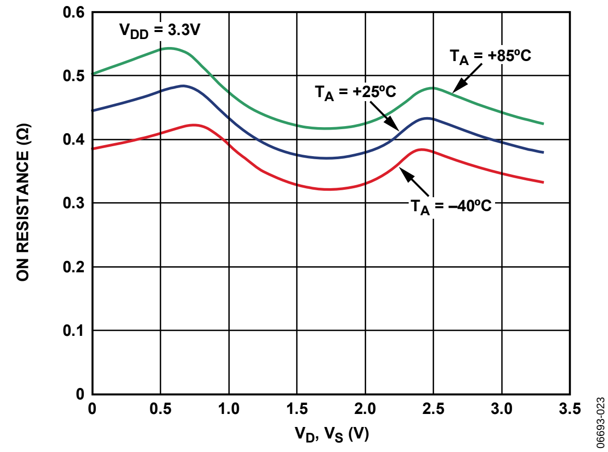

Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 3.3 V

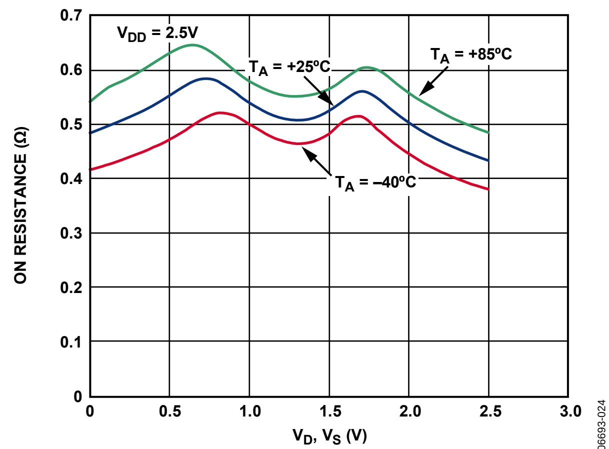

Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 2.5 V

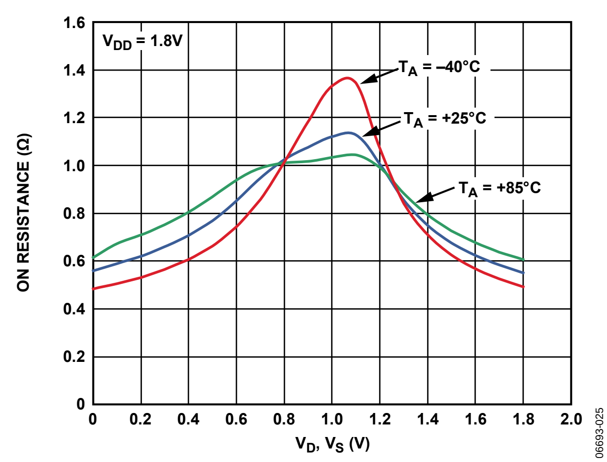

Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, V_{DD} = 1.8 V

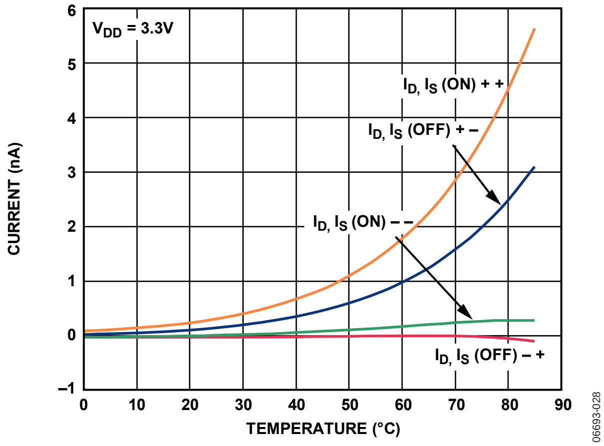

Figure 9. Leakage Current vs. Temperature, V_{DD} = 3.3 V

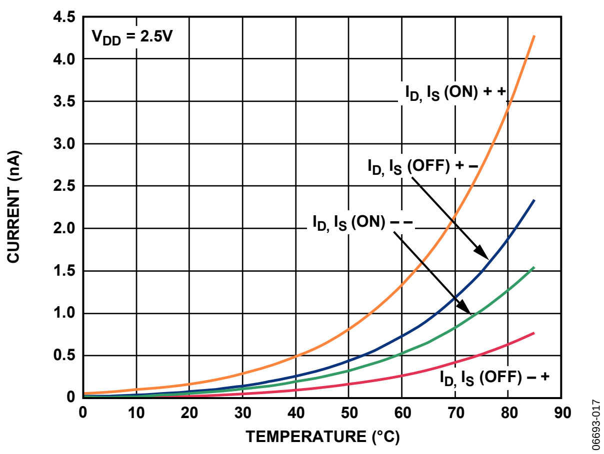

Figure 10. Leakage Current vs. Temperature, V_{DD} = 2.5 V

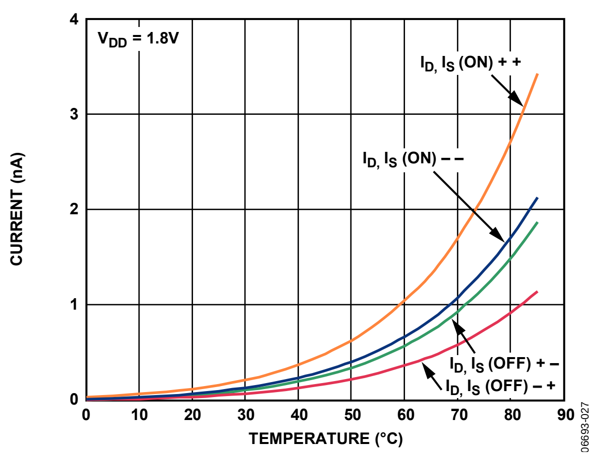

Figure 11. Leakage Current vs. Temperature, V_{DD} = 1.8 V

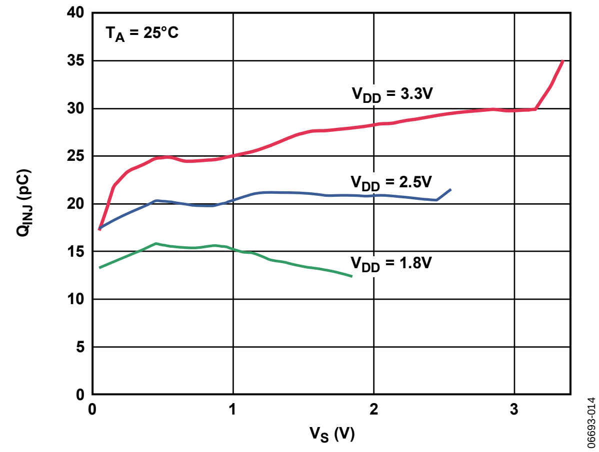

Figure 12. Charge Injection vs. Source Voltage

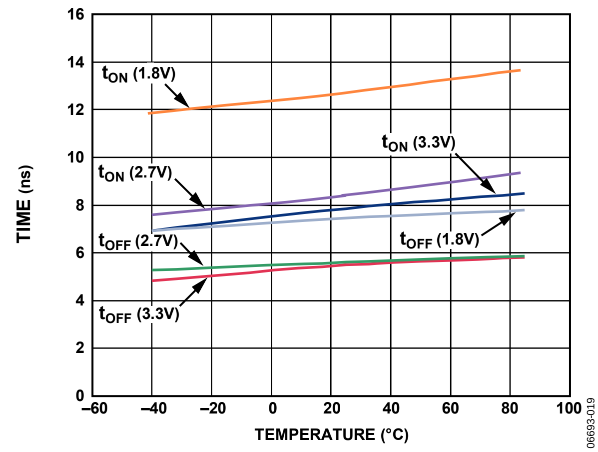

Figure 13. t_{ON}/t_{OFF} Times vs. Temperature

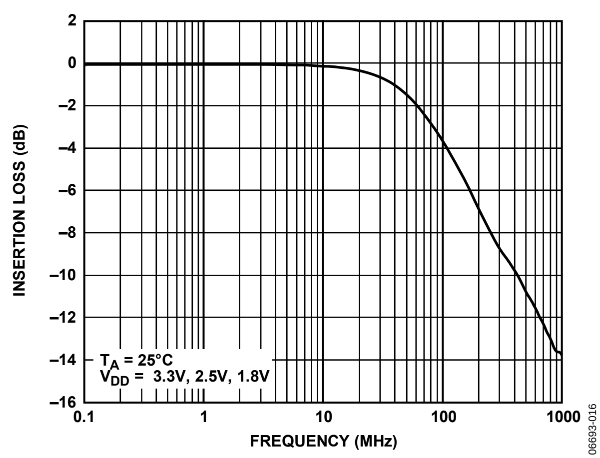

Figure 14. Bandwidth

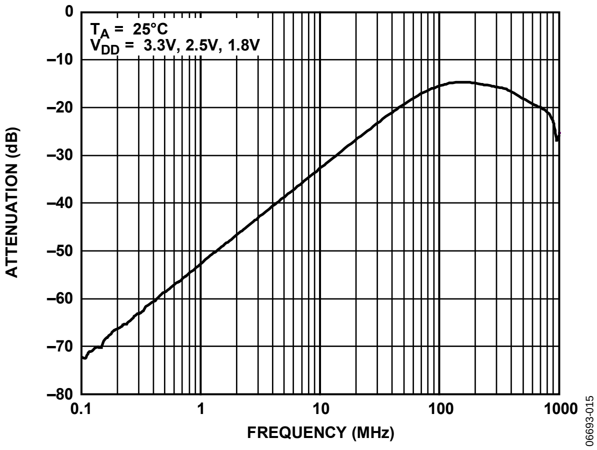

Figure 15. Off Isolation vs. Frequency

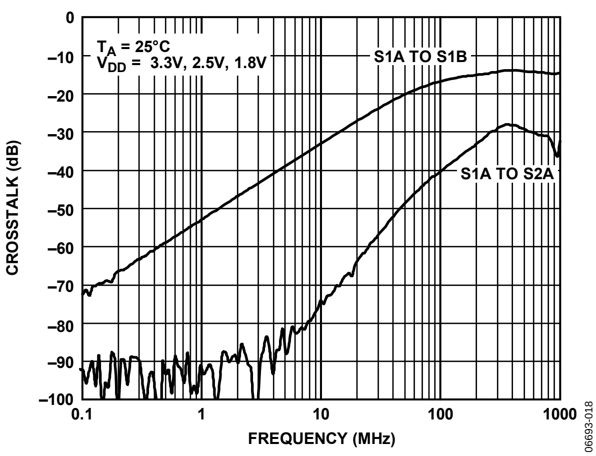

Figure 16. Crosstalk vs. Frequency

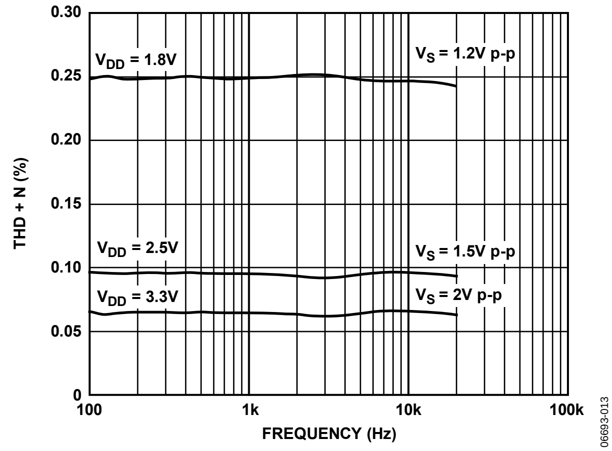

Figure 17. Total Harmonic Distortion + Noise vs. Frequency

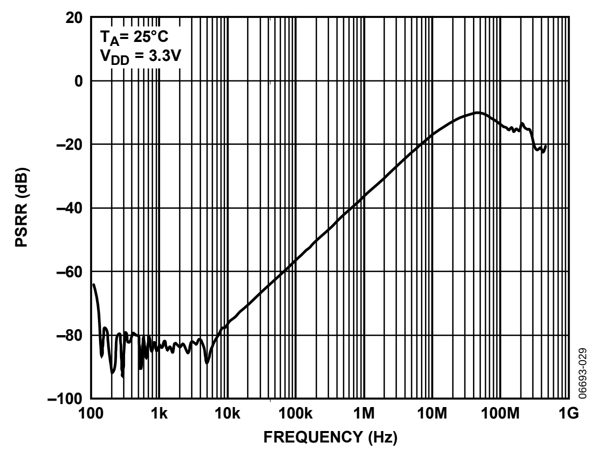

Figure 18. PSRR vs. Frequency

TEST CIRCUITS

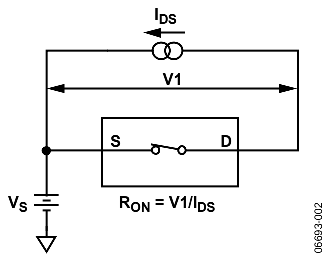

Figure 19. On Resistance

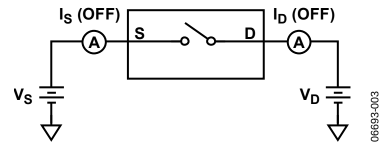

Figure 20. Off Leakage

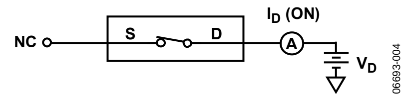

Figure 21. On Leakage

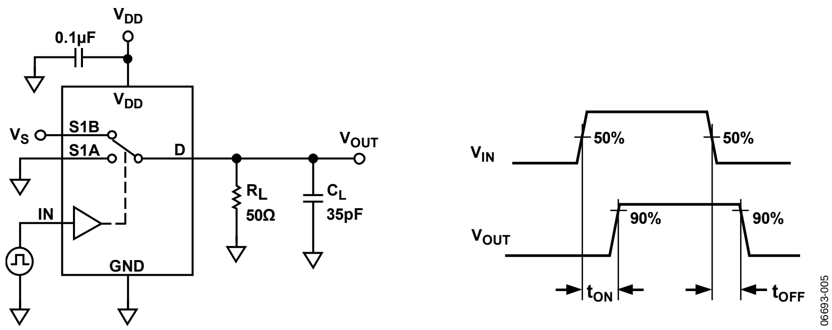

Figure 22. Switching Times, t_{ON}, t_{OFF}

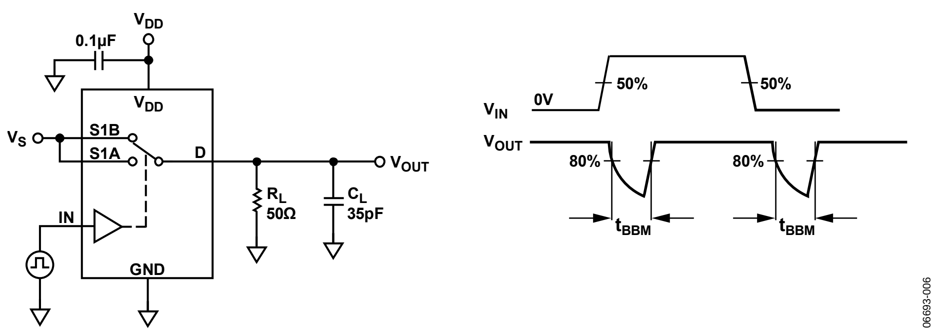

Figure 23. Break-Before-Make Time Delay, t_{BBM}

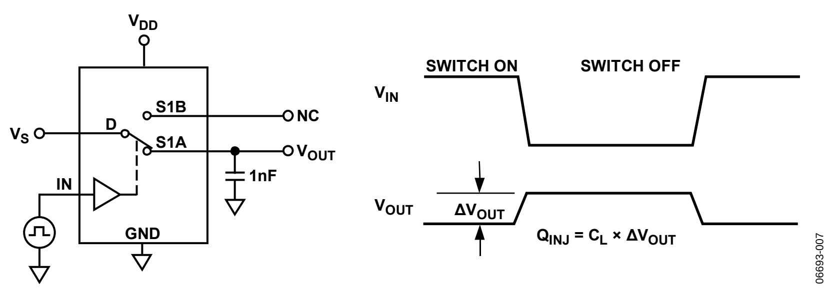

Figure 24. Charge Injection

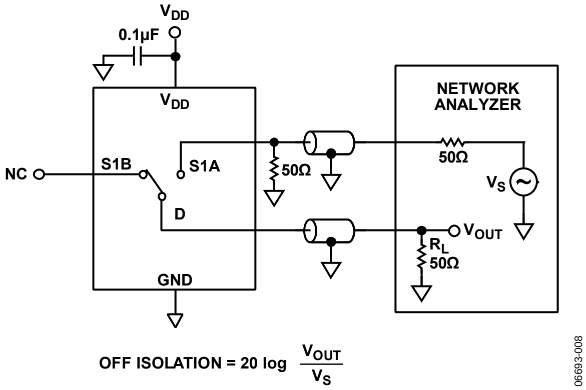

Figure 25. Off Isolation

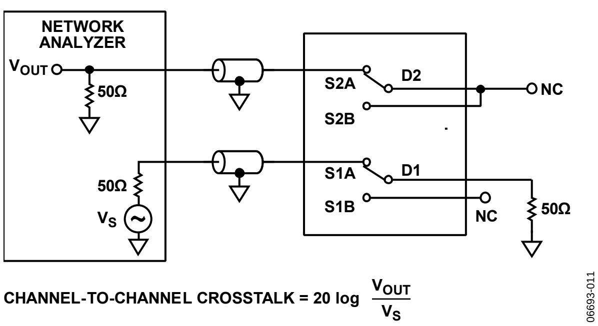

Figure 26. Channel-to-Channel Crosstalk (S1A to S2A/S1B to S2B)

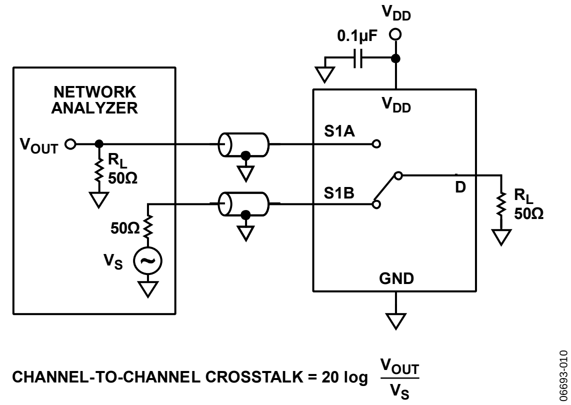

Figure 27. Channel-to-Channel Crosstalk (S1A to S1B/S2A to S2B)

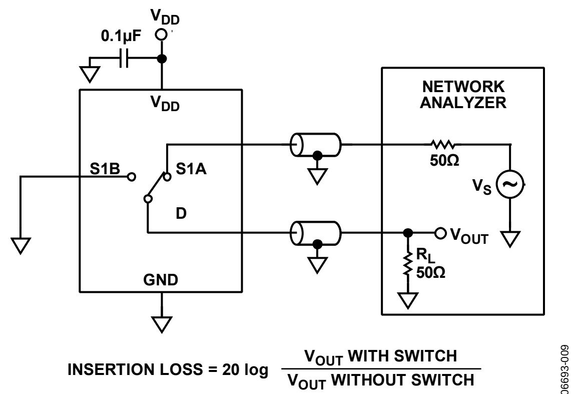

Figure 28. Bandwidth

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (On)

The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}

On resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

Measure of unwanted signal coupling through an off switch.

Crosstalk

Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth

Frequency at which the output is attenuated by 3 dB.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

OUTLINE DIMENSIONS

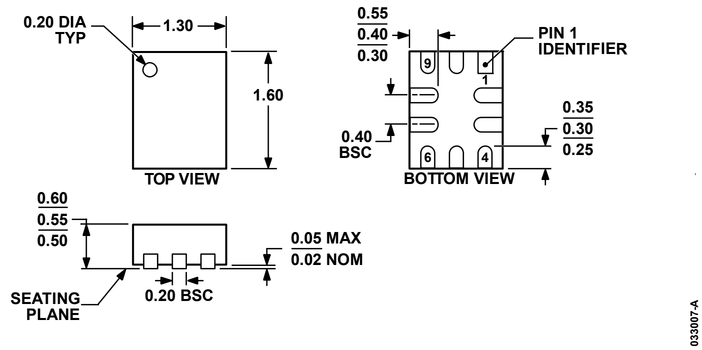

Figure 29. 10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)
1.3 mm × 1.6 mm Body, Ultra Thin Quad
(CP-10-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG824BCPZ-REEL[1]	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)	CP-10-10	A
ADG824BCPZ-REEL7[1]	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package (LFCSP_UQ)	CP-10-10	A
EVAL-ADG824EBZ[1]	−40°C to +85°C	Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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