Low IF Tuner IC for T-DMB/DAB/FM

Preliminary Technical Data

ADMTV300

FEATURES

Single-chip RF tuner for T-DMB, dual-band DAB, DAB+, and FM receiver

Low IF single-conversion architecture, which eliminates the need for SAW filters

Covers whole Band-III (168 MHz ~ 245 MHz), L-band (1450 MHz ~ 1492 MHz), and FM (88 MHz ~ 108 MHz)

High input sensitivity: −102 dBm

Very low power consumption: 70 mW at Band III

Supply: 1.2 V (core) / 1.8 V ~ 3.3 V (I/O)

On-chip fast switching fractional-N PLL

On-chip low phase noise and wide frequency range VCO

On-chip bandwidth-adjustable band-pass filter

Integrated IF programmable gain amplifier for direct connection to digital demodulators

Noise/linearity optimization through internal RF RSSI and AGC loop

Small 32-LFCSP (QFN) package (5 mm × 5 mm× 0.85 mm)

APPLICATIONS

Terrestrial DMB and DAB mobile phone

Low power portable TV, PDA, car A/V

FM radio applications

FUNCTIONAL BLOCK DIAGRAM

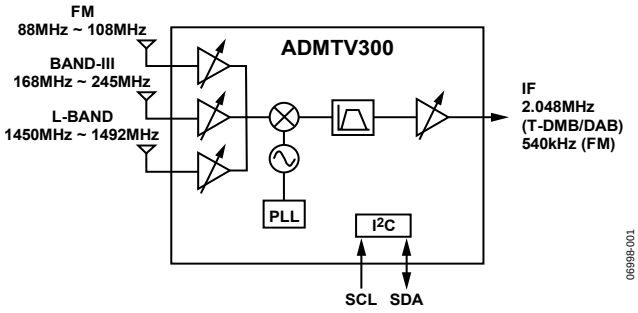

Figure 1.

GENERAL DESCRIPTION

The ADMTV300 is a highly integrated CMOS, single-chip, low IF single-conversion tuner IC for mobile application like terrestrial digital multimedia broadcasting (DMB), dual-band digital audio broadcasting (DAB), and FM. It includes three LNAs, a RF PGA, a down conversion mixer, a bandwidth-adjustable image rejection band-pass filter, an IF programmable gain amplifier, a VCO, and a fractional-N PLL. On-chip low phase noise VCO along with high-resolution fractional-N frequency synthesizer makes in-band phase noise lower than that of any other conventional tuner. The ADMTV300 uses single 1.2 V power supply. It has an industry-standard I^2C serial bus interface.

The ADMTV300 exhibits very low power consumption, such as 70 mW. With a small 5 mm × 5 mm 32-lead LFCSP (QFN) package, the ADMTV300 is the best solution for highly integrated multituner system applications and portable applications, where low power consumption is required critically.

PRODUCT HIGHLIGHTS

1. Single-chip RF tuner for terrestrial DMB, dual-band DAB, and FM
2. Low IF single-conversion architecture, which eliminates the need for SAW filters.
3. Very low power consumption: 70 mW.

Rev. PrD

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SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS					
1.2 V Supply Voltage (VDD12RF1, VDD12RF2, VDD12IF, VDD12VCO, VDD12PLL, VDD12CP, VDD12CORE)	V_{DD12}	1.1	1.2	1.3	V
2.8 V Supply Voltage(VDDIO)	V_{DDIO}	1.7	2.8	3.6	V
Operating Ambient Temperature	T_{OP}	−40		+85	°C
1.2 V Current Consumption (BAND-III)	I_{DD12B3}		60	70	mA
2.8 V I/O Current Consumption (BAND -III)	I_{DD3B3}		1	2	mA
1.2 V Current Consumption (L- BAND)	I_{DD12L}		65	77	mA
2.8 V I/O Current Consumption (L- BAND)	I_{DD3L}		1	2	mA
1.2 V Current Consumption (FM)	I_{DD12FM}		60	70	mA
2.8 V I/O Current Consumption (FM)	I_{DDIOFM}		1	2	mA
DIGITAL INPUT/OUTPUT PINS					
Analog/Digital Core Supply Voltage	V_{DD12}	1.1	1.2	1.3	V
I/O Supply Voltage	V_{DD3}	1.7	2.8	3.6	V
Maximum Low Input Voltage	V_{IL}			$0.3 \times V_{DD3}$	V
Minimum High Input Voltage	V_{IH}	$0.7 \times V_{DD3}$			V
Maximum Low Output Voltage	V_{OL}			$0.25 \times V_{DD3}$	V
Minimum High Output Voltage	V_{OH}	$0.75 \times V_{DD3}$			V
High Level Input Current (VIN = V_{DD3})	I_{IH}	−10		+10	µA
Low Level Input Current (VIN = GND)	I_{IL}	−10		+10	µA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD12} supplies = 1.2V. V_{DDIO} supplies = 2.8 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
BAND-III CHARACTERISTICS					
RF Frequency Range	$f_{BAND-III}$	168		245	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
IF Center Frequency	f_{IFB3}		2.048		MHz
Typical Dynamic Range	P_{IN}	−108		10	dBm
Noise Figure at Maximum Gain	NF		2.5	5	dB
In-Band Two-Tone IMD_3[1] (U/D)	IMD_{3I}		−50	−40	dBc
Out-Band Two-Tone IMD_3[2] (U/D)	IMD_{3O}		−40	−20	dBc
3 dB Cutoff Frequency Offset	f_{3dB}		±0.768		MHz
Stop-Band Attenuation at ±1.57 MHz	SBA		−55	−45	dBc
Image Rejection Ratio	IRR		−50	−40	dBc
Output SNR[3]	SNR	30	40		dB
LO Phase Noise (SSB at 100 kHz Offset)	PN		−110	−90	dBc/Hz
IF Output Amplitude V_{p-p}, Single	V_{OUTAC}	300	500	700	mV
IFAGC Input Voltage	V_{AGC}	0		1.2	V
Maximum Load at IF Output Pins, Differential	Z_{MAX}	2		10	kΩ pF

Parameter	Symbol	Min	Typ	Max	Unit
Output DC Voltage at IF Output Pins	V_{OUTDC}	0.5	0.6	0.7	V
L-BAND CHARACTERISTICS					
RF Frequency Range	f_{LBAND}	1450		1492	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
IF Center Frequency	f_{IFLB}		2.048		MHz
Typical Dynamic Range	P_{IN}	−105		10	dBm
Noise Figure at Maximum Gain	NF		3	6	dB
In-Band Two-Tone IMD_3[1] (U/D)	IMD_{3I}		−50	−40	dBc
Out-Band Two-Tone IMD_3[2] (U/D)	IMD_{3O}		−40	−20	dBc
3 dB Cutoff Frequency Offset	f_{3dB}		±0.768		MHz
Stop-Band Attenuation at ±1.57 MHz	SBA		−55	−45	dBc
Image Rejection Ratio	IRR		−50	−40	dBc
Output SNR[3]	SNR	30	40		dB
LO Phase Noise (SSB at 100 kHz Offset)	PN		−95	−90	dBc/Hz
IF Output Amplitude V p-p, Single	V_{OUTAC}	300	500	700	mV
IFAGC Input Voltage	V_{AGC}			1.2	V
Maximum Load at IF Output Pins, Differential	Z_{MAX}		2		kΩ
				10	pF
Output DC Voltage at IF Output Pins	V_{OUTDC}	0.5	0.6	0.7	V
FM CHARACTERISTICS					
RF frequency range	f_{FM}	88		108	MHz
RF input impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
IF Center Frequency	f_{IFFM}		0.54		MHz
Noise Figure	NF		5.5	8	dB
3 dB Cutoff Frequency Offset	f_{3dBFM}		±75		kHz
Stop-Band Attenuation at ±200 kHz	SBA_{FM}		−40	−30	dBc
Image Rejection Ratio	IRR		−40	−25	dBc

[1] For RF input power <−20 dBm.
[2] For RF input power <−90 dBm, two-tone interfere power is 40 dB higher than the wanted power.
[3] For DAB modulated signal with RF power higher than −70 dBm.

POWER SEQUENCE SPECIFICATIONS

Table 3.

Parameter	Symbol[1]	Min	Unit
Power Up Setup Margin for VDDIO	A	Don't care	µs
Power Up Setup Margin for VDDI2	B	10	µs
RESETB Setup Time for RESETB	C	100	µs
Setup Time for I²C Interface	D	100	µs

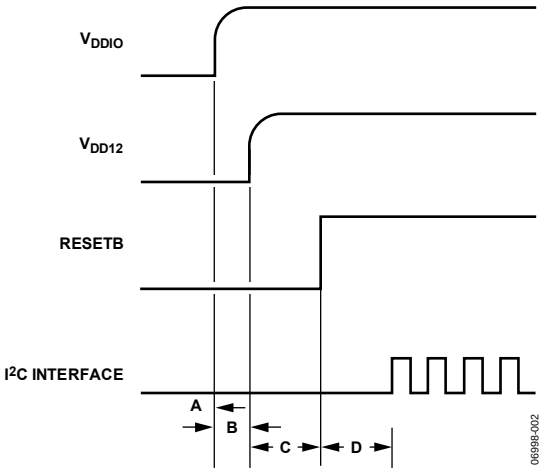


Figure 2. Power & Digital Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4. (T_A = 25°C, unless otherwise noted.)

Parameter	Rating
1.2 V Supply Voltage (VDD12RF1, VDD12RF2, VDD12IF, VDD12VCO, VDD12PLL, VDD12CP, VDD12CORE), V_{DD12}	−0.3 V to +1.4 V
2.8 V Supply Voltage (VDDIO), V_{DDIO}	−0.3 V to +4.6 V
Analog Input Voltage, V_{IA}	−0.3 V to V_{DD12} +0.3 V
Digital Input Voltage, V_{ID}	−0.3 V to V_{DD3} +0.3 V
Analog Output Voltage, V_{OA}	−0.3 V to V_{DD12} +0.3 V
Digital Output Voltage, V_{OD}	−0.3 V to V_{DD3} +0.3 V
Operating Temperature, T_{OP}	−40°C to +85°C
Storage Temperature Range, T_{STO}	−65°C to +150°C

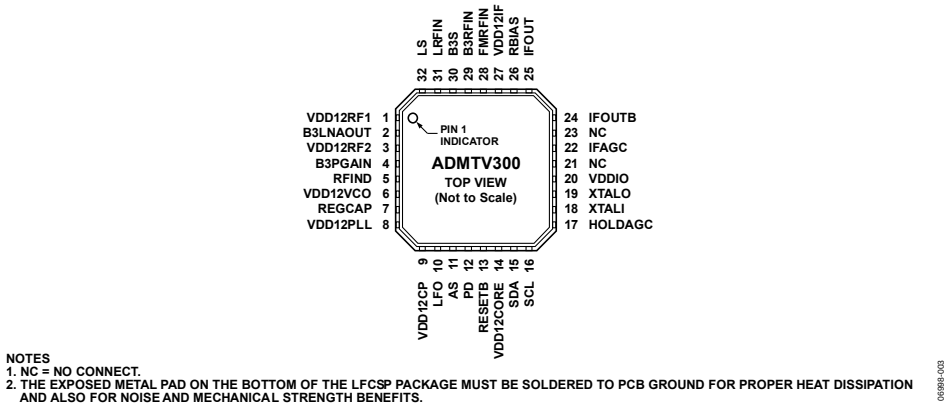
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED METAL PAD ON THE BOTTOM OF THE LFCSP PACKAGE MUST BE SOLDERED TO PCB GROUND FOR PROPER HEAT DISSIPATION AND ALSO FOR NOISE AND MECHANICAL STRENGTH BENEFITS.

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	I/O Type[1]	Function
1	VDD12RF1	P	RF Power V_{DD12}.
2	B3LNAOUT	AO	Band-III LNA Output.
3	VDD12RF2	P	RF Power V_{DD12}.
4	B3PGAIN	AI	Band-III RF PGA Input.
5	RFIND	AI	RF Inductor for Band-III and FM.
6	VDD12VCO	P	VCO Power V_{DD12}.
7	REGCAP	AO	VCO Regulator Output.
8	VDD12PLL	P	PLL Power V_{DD12}.
9	VDD12CP	P	Charge Pump Power V_{DD12}.
10	LFO	AO	Charge Pump Output.
11	AS	DI	Address Select Input.
12	PD	DI	Hardware Power-Down. 0 V for operation and V_{DDIO} for power-down.
13	RESETB	DI	Reset Input. 0 V for reset, V_{DDIO} for normal operation.
14	VDD12CORE	P	Digital Power V_{DD12}.
15	SDA	DB	I^2C Data. Bidirectional Pin. Open-drain output/5 V tolerant input.
16	SCL	DI	I^2C Clock.
17	HOLDAGC	DI	HOLDAGC Input. 0 V for AGC operation and V_{DDIO} for AGC hold.
18	XTALI	DI	Crystal Oscillator Input.
19	XTALO	DO	Crystal Oscillator Output.
20	VDDIO	P	Digital Power V_{DDIO}.
21	NC	NC	No connection
22	IFAGC	AI	External AGC Input or IF RSSI Output. Programmable.
23	NC	NC	No Connection
24	IFOUTB	AO	Negative IF Output.
25	IFOUT	AO	Positive IF Output.
26	RBIAS	AI	External Bias Resistor.
27	VDD12IF	P	IF Power V_{DD12}.
28	FMRFIN	AI	FM LNA Input.
29	B3RFIN	AI	Band-III LNA Input.
30	B3S	AO	Band-III LNA Source Inductor.
31	LRFIN	AI	L-band LNA Input.
32	LS	AO	L-band LNA Source.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DB = digital bidirectional, P = power supply, NC = no connection

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD12} = 1.2 V, V_{DDIO} = 2.8 V, unless otherwise noted.

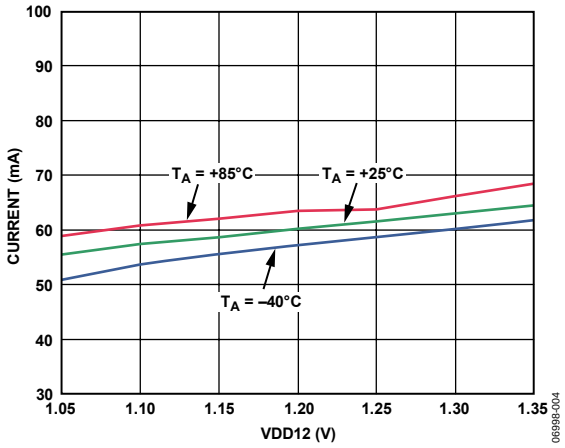


Figure 4. Band-III Receive Mode Supply Current vs. Supply Voltage

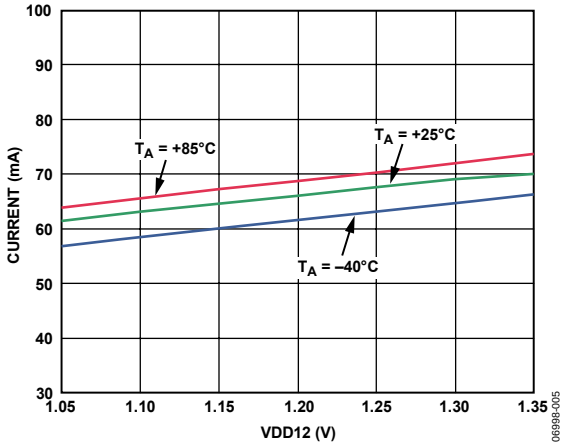


Figure 5. L-Band Receive Mode Supply Current vs. Supply Voltage

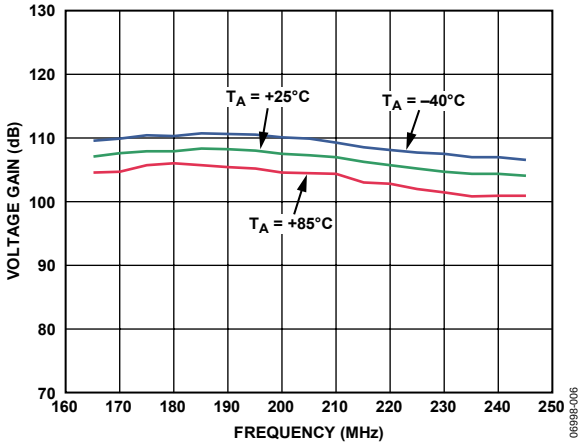


Figure 6. Band-III Voltage Gain vs. Frequency

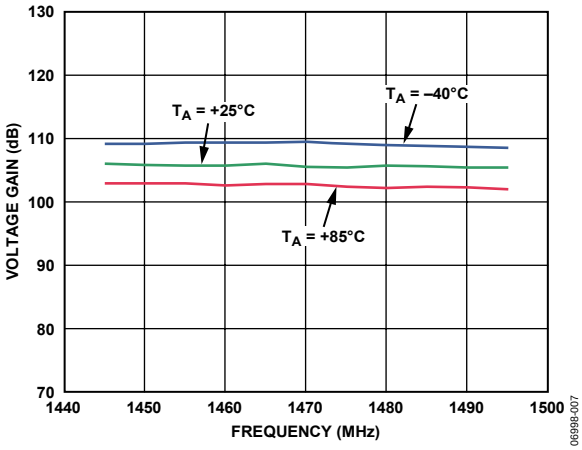


Figure 7. L-Band Voltage Gain vs. Frequency

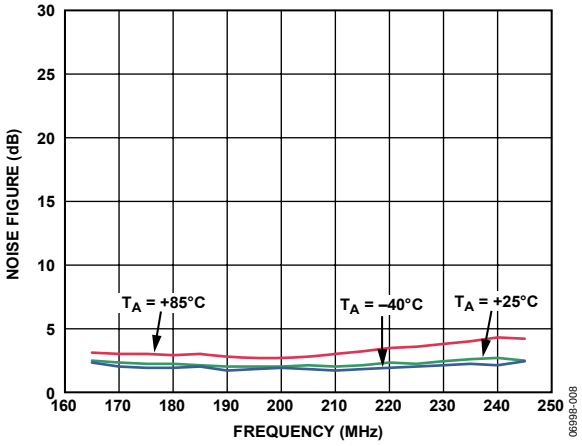


Figure 8. Band-III Noise Figure vs. Frequency

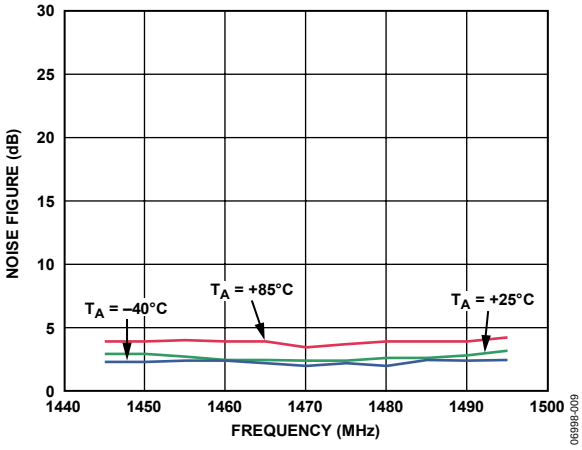


Figure 9. L-Band Noise Figure vs. Frequency

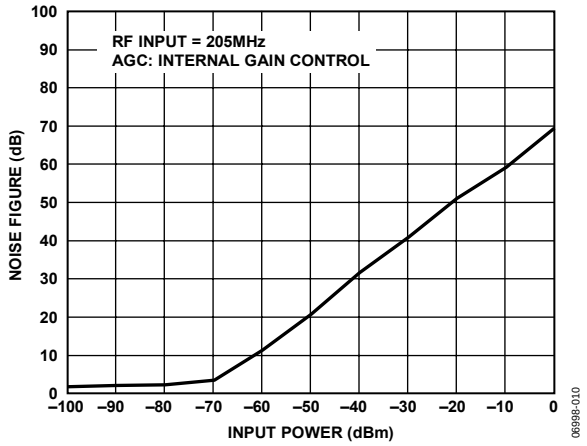


Figure 10. Band-III Noise Figure vs. Input Power

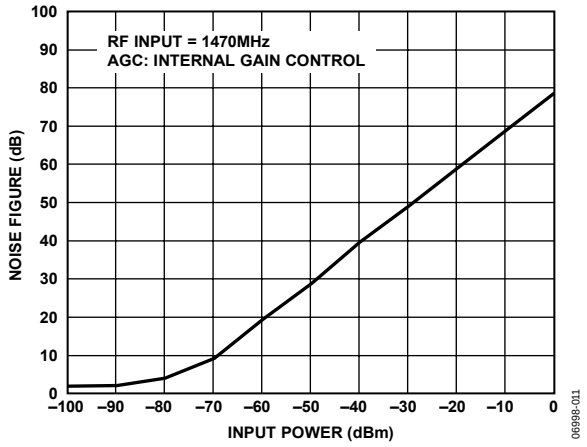


Figure 11. L-Band Noise Figure vs. Input Power

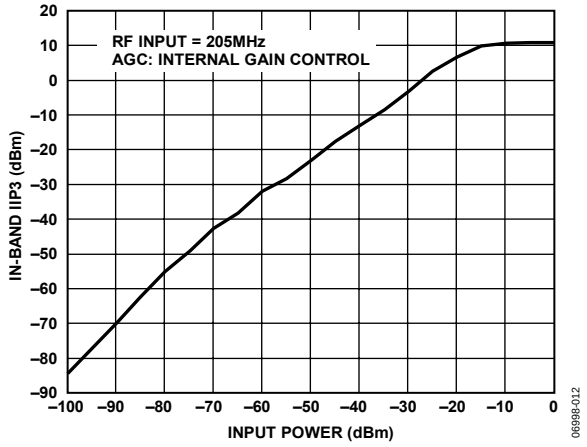


Figure 12. Band-III In-Band IIP3 vs. Input Power

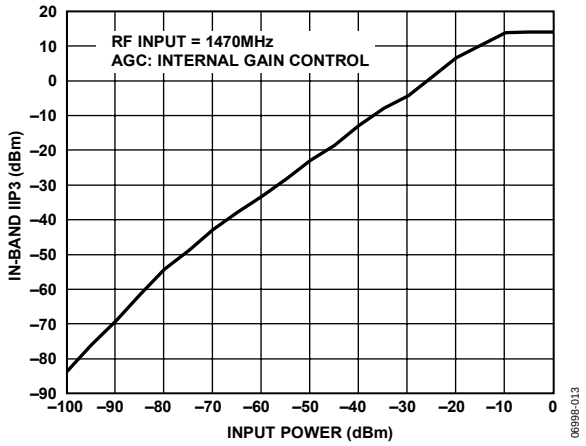


Figure 13. L-Band In-Band IIP3 vs. Input Power

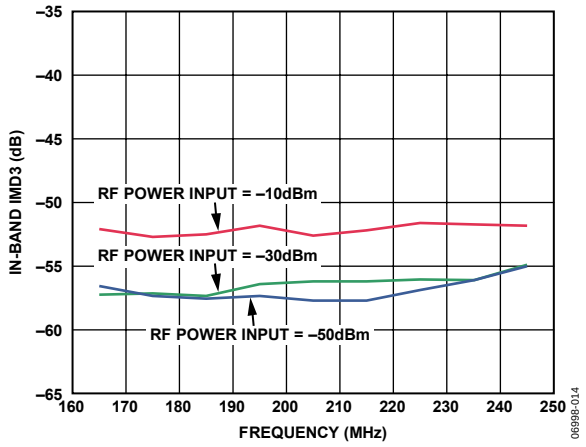


Figure 14. Band-III IMD3 vs. Frequency

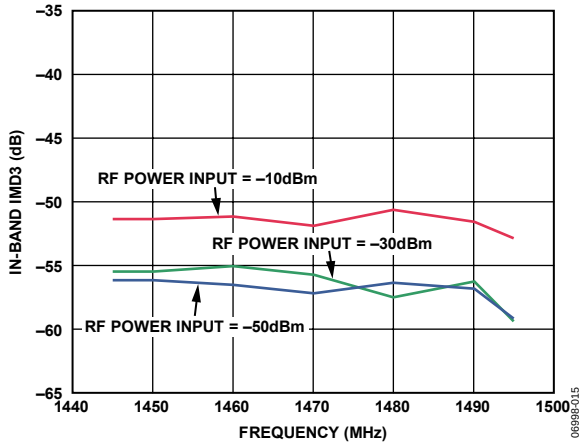


Figure 15. L-Band IMD3 vs. Frequency

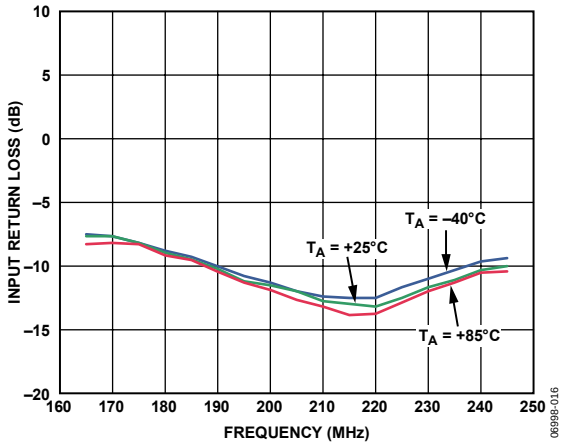


Figure 16. Band-III Input Return Loss vs. Frequency (LNA Gain Mode: High)

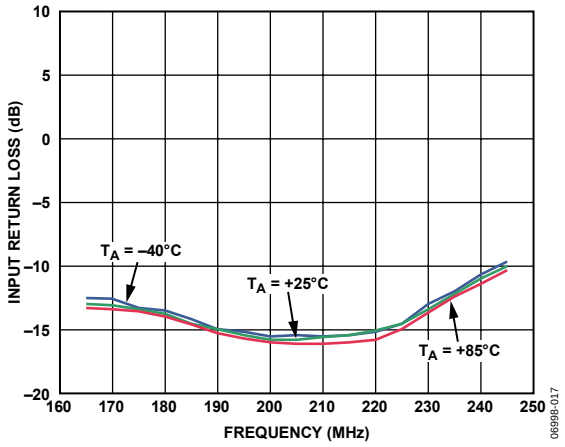


Figure 17. Band-III Input Return Loss vs. Frequency (LNA Gain Mode: Low)

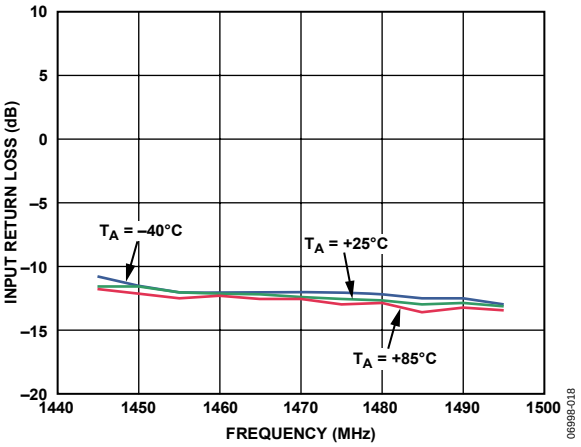


Figure 18. L- Band Input Return Loss vs. Frequency (LNA Gain Mode: High)

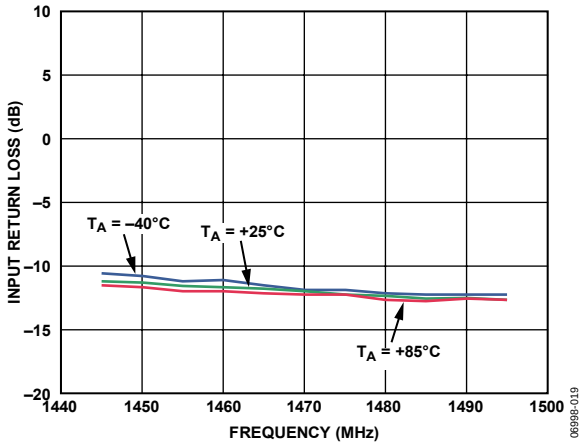


Figure 19. L- Band Input Return Loss vs. Frequency (LNA Gain Mode: Low)

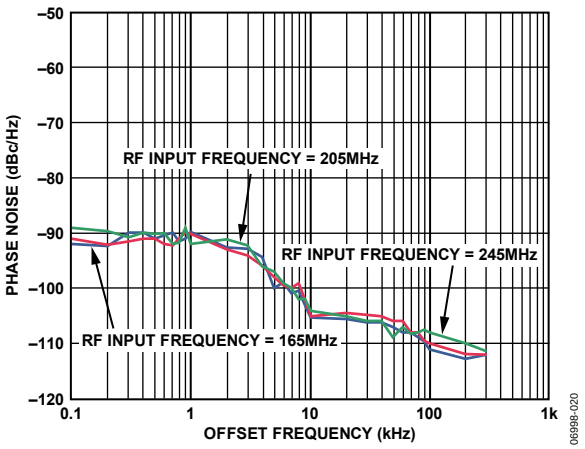


Figure 20. Band-III Phase Noise vs. Offset Frequency

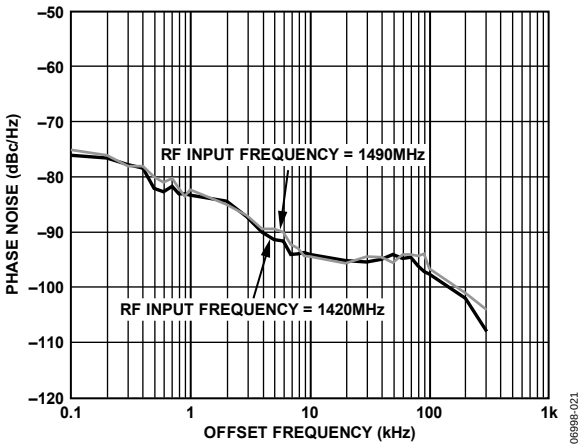


Figure 21. L-band Phase Noise vs. Offset Frequency

TERMINOLOGY

Input Third-Order Intercept (IIP3)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at the specified frequencies relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities, producing IMD components at (2 × f1) − f2 and (2 × f2) − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when it is plotted in decibels.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa, nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

Noise Figure (NF)
The degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Voltage Standing-Wave Ratio (VSWR)
The ratio of the amplitude of the elective field at a voltage maximum to that at an adjacent voltage minimum.

THEORY OF OPERATION

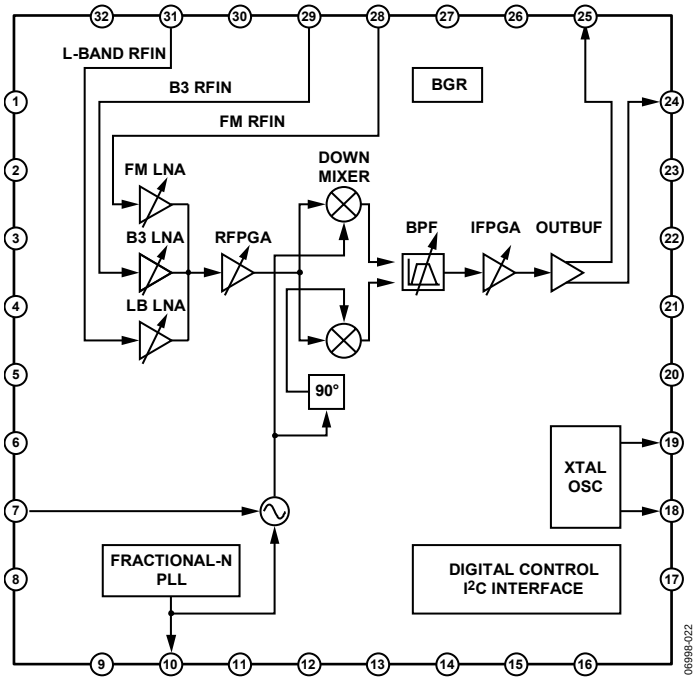


Figure 22. ADMTV300 Block Diagram

RF LNA, PGA, AND DOWNCONVERTER

RF LNA, programmable gain amplifier (PGA), and downconverter amplify in-coming RF signals and downconvert them to low IF frequency. LNA has three gain modes, which are high, mid, and low gain with 18 dB gain step. The LNA gain state can be read from the LNAGAIN register (0: low gain; 1, 2: mid gain; 3: high gain). RFPGA has around 30 dB gain dynamic range. RFPGA gain is controlled by digital gain code, which can be read from the RFAGC[7:0] register. RFPGA gain is from 0x00 (minimum gain) to 0xff (maximum gain). Gain step is around 0.35 dB. The downconversion mixer downconverts the signal from the RFPGA output.

LOCAL OSCILLATOR

The ADMTV300 includes an on-chip VCO, which eliminates the need for an external LC tank. The VCO in ADMTV300 uses only 1.2 V. The internal VCO covers whole Band-III, L-Band, and FM, which are 168 MHz ~ 245 MHz, 1450 MHz ~ 1492 MHz, and 88 MHz ~ 108 MHz, respectively. Along with fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of T-DMB, DAB, and FM signals.

PLL

The ADMTV300 local oscillator consists of a ∑-Δ fractional-N frequency synthesizer and a VCO. The integrated VCO covers the full Band-III, L-band, and FM frequency range. The VCO in ADMTV300 uses only 1.2 V.

The synthesizer uses fractional-N type architecture with a high performance 20-bit ∑-Δ modulator to attain high resolution and fast switching time, as well as good phase noise. The charge pump is programmed by a 6-bit digital control, and its current range is from 20 μA to 1280 μA.

Unlike the integer-N type synthesizer used in other silicon tuners, a ∑-Δ modulated frequency synthesizer provides fast switching time, ultra high frequency resolution, and good phase noise due to its wide bandwidth.

The switching time is less than 30 μs for the worst case of power-up sequence. Using a 16.384 MHz oscillator, the 20-bit ∑-Δ modulated fractional-N phase-locked loop exhibits very fine frequency resolution of 16 Hz. It can compensate for the frequency offset induced in part by the reference crystal frequency error and the temperature drift of crystal. The LO frequency, f_{LO}, is calculated as follows:

$$LO\ Frequency = \{Clock\ Frequency \times (PLLN + PLLF \div 2^{20})\}$$

where *PLLN* is the N-counter divide value, and *PLLF* is the fractional value.

IF BPF AND PGA

The IF block contains BPF and PGA. The RF signal is reduced to low IF through the RF downconverter. The IF BPF selects the signal of interest from the output of the downconverter and eliminates the image signal. The cutoff frequency of BPF is about 1.28 MHz and 2.82 MHz for T-DMB and DAB, 465 kHz and 615 kHz for FM. To compensate for the variation of cutoff frequency in the BPF, the automatic cutoff-tuning circuit is included. This circuit guarantees the cutoff frequency accuracy.

The IF PGA controls the input level of the ADC in the demodulator. The gain of the IF PGA is controlled by an 8-bit gain control register. The PGA gain setting can be read from the GVBB register. GVBB[7:0] ranges from 0x00 to 0xc3. The digital gain step is around 0.25 dB. The IF PGA gain setting can be programmed for ADMTV300 test mode by using the I²C GVBBI2C[7:0] register. The EXTGVBB[1:0] register setting allows for three gain setting modes: IF internal AGC using analog IF RSSI, manual gain setting using GVBBI2C, and gain setting from the PWM output of the demodulator.

AUTOMATIC GAIN CONTROL

In ADMTV300, there are two AGC loops: RFAGC and IFAGC. LNA has a three-step gain control, and the gain difference is 18 dB. RFPGA has around a 30 dB gain dynamic range and BPF has around a 14 dB gain dynamic range controlled by the RFAGC[7:0] register. The register value is from 0x00 (minimum gain) to 0xff (maximum gain). The RFAGC consists of these two blocks. RFAGC dynamic range is around 80 dB.

IFAGC has a programmable gain amplifier with a gain step of 0.25 dB. The ADMTV300 IF gain is determined by the digital gain setting of the GVBB[7:0] register. The register value is from 0x00 (minimum gain) to 0xc3 (maximum gain). The IFAGC dynamic range is around 48 dB. With these two dynamic ranges (RF 80 dB and IF 48 dB), the ADMTV300 dynamic range is larger than 100 dB.

I²C INTERFACE AND CLOCK CONTROL

ADMTV300 uses an I²C (Inter IC) bus interface. Serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending on the function of the device.

HARDWARE/SOFTWARE POWER-DOWN

There is a hardware power-down pin (Pin 12). The ADMTV300 also has a software power-down mode controlled by the I²C PD register. If PD is high, ADMTV300 goes to power-down mode. To restart, PD should be low. But in software power-down mode, the digital part remains active.

APPLICATION INFORMATION

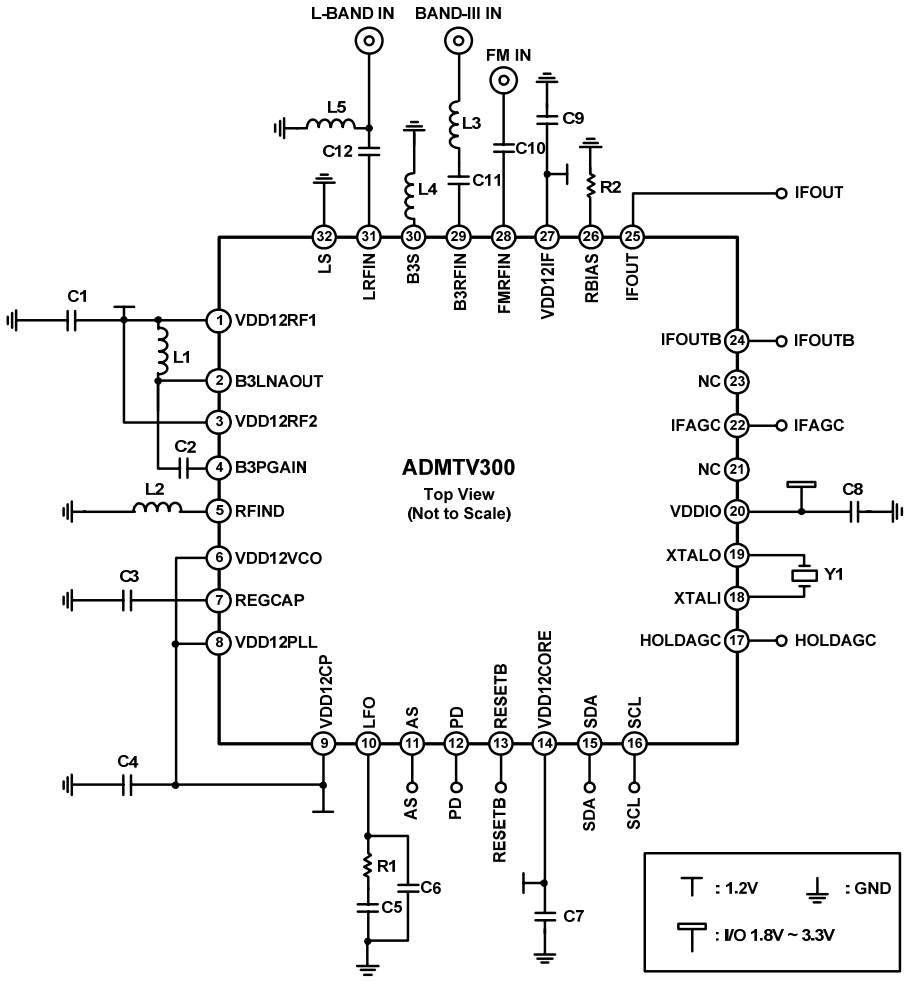


Figure 23. Typical Connection Diagram

RF INPUT STAGE

RF matching components should be located as close as possible to the chip.

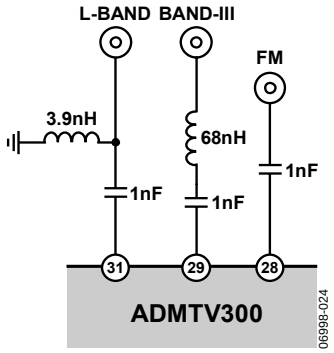


Figure 24. RF Input Stage

DIGITAL INTERFACE—I²C/RESET

ADMTV300 is controlled by the I²C communication protocol. The maximum operating frequency of the I²C SCL is about 400 kHz (2.5 µs). The I²C address can be determined by the AS pin. If AS is connected to ground, the ADMTV300 chip address is 0xC2; if AS is connected to VDDIO, the chip address is 0xC4. SCL/SDA switching noise can degrade VCO phase noise, and RC noise filter can help to reject this type of noise. ADMTV300 has a reset for I²C initialization and internal logic initialization. The reset pin is RESETB, which is active low. Therefore, if RESETB is low, the ADMTV300 is in the reset state; if RESETB is high, ADMTV300 is in normal operation. The voltage of logical high is VDDIO.

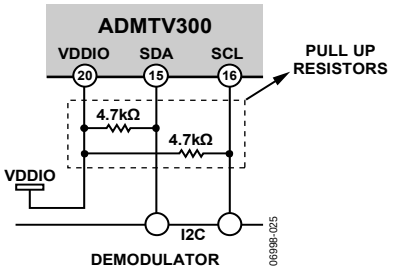


Figure 25. I²C Interface Between ADMTV300 and I²C Controller

IF AGC INTERCONNECTION

ADMTV300 supports internal and external IFAGC mode. To use external IFAGC mode,

1. EXTGVBB (Address 0x27) = 2.
2. SWPDIFRSSI (Address 0x2b) = 1.
3. Connect the IF AGC control voltage (0 V ~ 1.2 V) to Pin 22 via the proper low-pass filter.

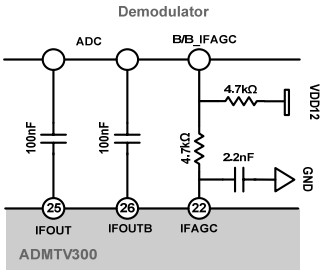


Figure 26. AGC Connection

1.2 V SUPPLY VOLTAGE APPLICATION

The ADMTV300 core supply voltage is 1.2 V, but a mobile phone has only 3.7 V battery supply. There are two methods to generate 1.2 V supply. One is through a linear regulator, and the other is by using a dc-to-dc converter. In mobile applications, using a dc-to-dc converter is recommended due to its power efficiency.

CRYSTAL SELECTION

ADMTV300 supports three crystal/TCXO frequencies: 16.384 MHz, 19.2 MHz, and 24.576 MHz. A feedback resistor and shunt capacitors (C_{p1}, C_{p2}: 8 pF) are also integrated on-chip.

CRYSTAL APPLICATION RECOMMENDATIONS

We strongly recommend that the crystal be located as close to the demodulator as possible, as shown in Figure 27, to reduce crystal harmonic spur.

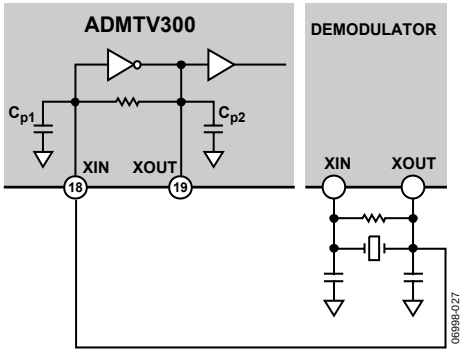


Figure 27. Clock Signal from Demodulator to Tuner

When the clock signal enters the tuner, the swing voltage level (sine wave or rectangular type) must be higher than 1 Vpp.

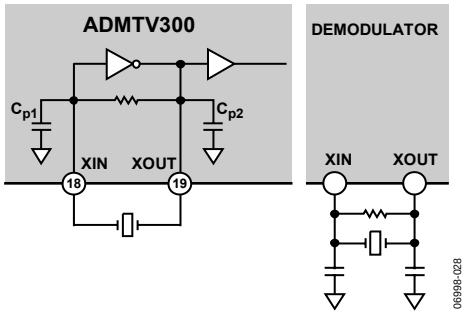


Figure 28. Two Crystals

When selecting a crystal, it is strongly recommended contacting the crystal vender to inquire about an optimized crystal application circuit that includes an external circuit.

RF AGC SETTING

In the ADMTV300, there are RF/IF dual AGC loops. Each loop can be controlled independently. RF gain is digitally controlled by the internal RF RSSI, which is located between the band-pass filter and the IF PGA. For test purposes, RF gain can also be set manually.

AUTOMATIC RF GAIN SETTING USING INTERNAL RF AGC (DEFAULT)

For take-over point, or TOP, (Address 0x20) values from 0x0 to 0x6, the internal RF AGC operates. When increasing the TOP (Address 0x20) value, TOP increases by 6 dB steps.

MANUAL RF GAIN SETTING

For RF manual gain setting, TOPI2C (Address 0x20) should be

set to 0x7. With this setting, the RFAGC (Address 0x04) value is loaded from RFAGCI2C (Address 0x5f). The RFAGC value should be between 0x00 and 0xff.

For example, to set the maximum RF gain manually,

TOP (Address 0x20) = 0x07,
RFAGCI2C[7:0] (Address 0x5f) = 0xff

IF AGC SETTING

ADMTV300 supports three IF AGC modes: internal IF AGC mode, external (from demodulator) IF AGC mode, and manual gain setting mode for test purposes.

INTERNAL IF AGC MODE (DEFAULT)

At default, ADMTV300 operates in the internal IF AGC mode. By changing IFPWR[1:0] (Address 0x25), the IF output level can be changed. The IF output amplitude can be increased by 6 dB as IFPWR is increased by 1.

EXTERNAL IF AGC MODE (AGC CONTROL FROM DEMODULATOR)

To use the AGC control signal from the demodulator,

1. EXTGVBB (Address 0x27) = 2.
2. SWPDIFRSSI (Address 0x2b) = 1.
3. Connect the IF AGC control voltage (0 V ~ 1.2 V) to Pin 22 via the proper low-pass filter.

MANUAL IF GAIN SETTING

To set the IF gain manually,

1. EXTGVBB (Address 0x27) = 1.
2. SWPDIFRSSI (Address 0x2b) = 1.
3. Set GVBBI2C (Address 0x64).

With these settings, the GVBB (Address 0x05) value is loaded from GVBBI2C (Address 0x64). The GVBB value should be between 0x00 and 0xc3.

I²C OPERATION

The ADMTV300 is controlled by an I²C data bus and is compatible with both standard and fast mode formats. The data and clock are fed on the SDA and SCL lines, respectively, as defined by the I²C bus format. The device can either accept data in the write mode or send data in the read mode. The LSB of the address byte sets the device into write mode if the AS pin is low and into read mode if the AS pin is high.

I²C READ/WRITE ADDRESS

Table 6. I²C Read/Write Address

	MSB	Address						LSB	
Address Select Pin	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
Read Mode									
AS									
Low	1	1	0	0	0	0	1	1	C3
High	1	1	0	0	0	1	0	1	C5
Write Mode									
AS									
Low	1	1	0	0	0	0	1	0	C2
High	1	1	0	0	0	1	0	0	C4

I²C BUS FORMAT

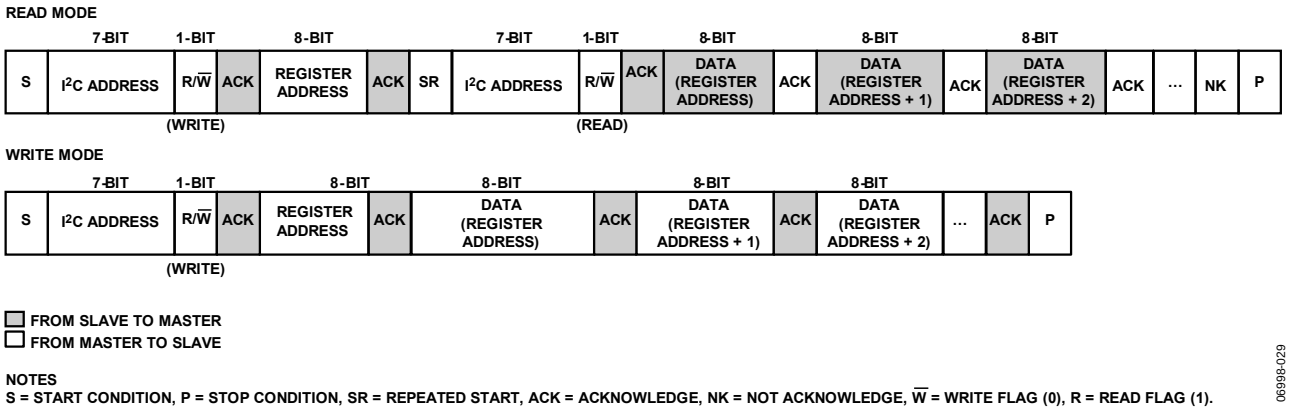


Figure 29. I²C Bus Format

I²C TIMING CHARACTERISTICS

According to standard I²C specification, the CLK frequency reaches its maximum 400 kHz in fast mode and reaches 100 kHz in standard mode. To communicate with the RF tuner, users need to comply with the conditions outlined in this section.

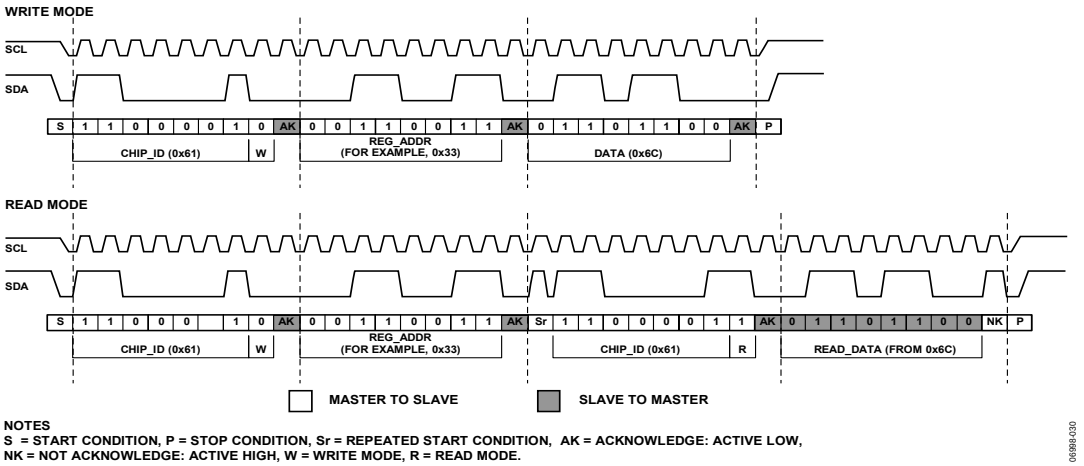


Figure 30. Serial Control Port Write Mode

Serial Control Port Timing

T_A = 25°C, V_{DDIO} = 2.8 V, GND = 0 V, unless otherwise noted.

Table 7. I²C Serial Control Timing

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Hold Time (Repeat) Start Condition[1]	t_{SHD}	4.0		0.6		µs
SCL Clock Period	t_{CLK}	0	100	0	400	kHz
High Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
Low Period of the SCL Clock	t_{LOW}	4.7		1.3		µs
Setup Time for Stop Condition	t_{PSU}	4.0		0.6		µs
Data Setup Time	t_{DSU}	250		100[2]		ns
Data Hold Time for I²C Bus Devices	t_{DHD}	0[3]	3.45[4]	0[3]	0.9[4]	µs

[1] After this period, the first clock pulse is generated.
[2] A fast mode I²C bus device can be used in a standard mode I²C bus system, but the $t_{DSU} \geq 250$ ns requirement must then be met. This automatically occurs if the device does not stretch the low period of the SCL signal (t_{LOW}).
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
[4] The maximum t_{DHD} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

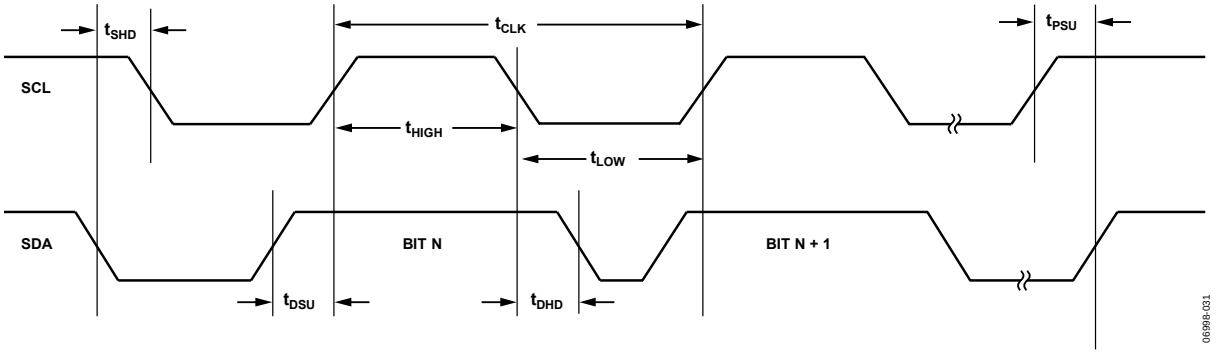


Figure 31. Serial Control Port Timing

I²C REGISTER MAP

Table 8. Read-Only Registers

Register Name	Type	MSB			Address			LSB
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD00	R	CHIPID1[7:0]							
RD01	R	CHIPID0[7:0]							
RD02	R	SPLITID[7:0]							
RD03	R	Blank		LNAGAIN[1:0]		GVBPF[1:0]		BIAS SHORT	LOCK
RD04	R	RFAGC[7:0]							
RD05	R	GVBB[7:0]							
RD06	R	Blank			CTUNE[4:0]				
RD07	R	Blank			CV[4:0]				
RD08	R	Blank			OFSCON[12:8]				
RD09	R	OFSCON[7:0]							
RD0A	R	Blank		VCORG[5:0]					
RD0B	R	Blank		VCOCON[5:0]					
RD0C	R	Blank			EICP_CALI[4:0]				
RD0D	R	Blank			MICP_CALO[4:0]				
RD0E	R	Blank		RTUNE[5:0]					
RD0F	R	Blank		RV[5:0]					
RD10	R	READEFUSE[31:24]							
RD11	R	READEFUSE[23:16]							
RD12	R	READEFUSE[15:8]							
RD13	R	READEFUSE[7:0]							
RD14	R	RFRSSID[7:0]							
RD15	R	ADJRSSID[7:0]							
RD16	R	RFPWRDETD[7:0]							
RD17	R	IFRSSID[7:0]							
RD18	R	BBAGCEXTD[7:0]							
RD19	R	TMPSNSD[7:0]							
RD1A	R	VTUNED[7:0]							
RD1B	R	Reserved							
RD1C	R	Reserved							

Table 9. Read/Write Registers

Register Name	Initial[1]	Type	MSB		Address					LSB
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR20	0x6b	R/W	BAND[1:0]		BPFBW	ADJ[1:0]		TOP[2:0]		
WR21	0x73	R/W	CONVCOBUF[2:0]			PDAAC	CLKSEL[2:0]			EXTCKOEN
WR22	0x20	R/W	DIVSEL[1:0]		ICP[5:0]					
WR23	0xb8	R/W	CTUNE_ ON	RTUNE_ ON	AAC_RN	RN_PLL	RN_CNT	Reserved	AAC_EN	VCO BIASSW
WR24	0x83	R/W	ICP_OFS[4:0]					ICP_EXT	PC4	DTHEN
WR25	0x40	R/W	IFPWR[1:0]		N[13:8]					
WR26	0x33	R/W	N[7:0]							
WR27	0x00	R/W	CAL_ON	PCAL_ON	EXTGVBB[1:0]		F[19:16]			
WR28	0xa0	R/W	F[15:8]							
WR29	0x00	R/W	F[7:0]							

Register Name	Initial[1]	Type	MSB	Address						LSB
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR2A	0x00	R/W	SWPD LNA	SWPD RFPGA	SWPD MIXER	SWPD BPF	SWPD CTUNE	SWPD BBPGA	SWPD OUTBUF	SWPD VCO
WR2B	0x00	R/W	SWPD PLL	SWPD PWDET	SWPD ADJRSSI	SWPD RFRSSI	SWPD IFRSSI	SWPD TMPSNS	SWPD RTUNE	SWPD ADC
WR2C	0x3f	R/W	SWPD LDO	SWPD BGR	TSPD LNA	TSPD RFPGA	TSPD MIXER	TSPD BPF	TSPD CTUNE	TSPD BBPGA
WR2D	0xff	R/W	TSPD OUTBUF	TSPD VCO	TSPD PLL	TSPD PWDET	TSPD ADJRSSI	TSPD RFRSSI	TSPD IFRSSI	TSPD TMPSNS
WR2E	0xf5	R/W	TSPD RTUNE	TSPD ADC	TSPD LDO	TSPD BGR	Reserved			
WR2F	0x42	R/W	Reserved							
WR30	0x45	R/W	Reserved							
WR31	0x22	R/W	Reserved							
WR32	0x24	R/W	Reserved							
WR33	0x8b	R/W	Reserved							
WR34	0x3f	R/W	Reserved							
WR35	0x3c	R/W	Reserved							
WR36	0xfc	R/W	Reserved							
WR37	0x6f	R/W	Reserved							
WR38	0x30	R/W	Reserved							
WR39	0xd8	R/W	Reserved							
WR3A	0x00	R/W	Reserved							
WR3B	0xbf	R/W	Reserved				CONBAND[3:0]			
WR3C	0x7c	R/W	Blank	Reserved						
WR3D	0x10	R/W	Reserved							
WR3E	0xf0	R/W	Reserved							
WR3F	0x33	R/W	Reserved							
WR40	0x04	R/W	Reserved							
WR41	0xf6	R/W	Reserved							
WR42	0x76	R/W	Reserved							
WR43	0x36	R/W	Reserved							
WR44	0x80	R/W	Reserved							
WR45	0x4b	R/W	Reserved							
WR46	0x40	R/W	Reserved							
WR47	0xc0	R/W	Reserved							
WR48	0x93	R/W	Reserved							
WR49	0x40	R/W	Reserved							
WR4A	0x8d	R/W	Reserved							
WR4B	0x72	R/W	Reserved							
WR4C	0xd7	R/W	Reserved							
WR4D	0x14	R/W	Reserved							
WR4E	0xf4	R/W	Reserved							
WR4F	0x24	R/W	Reserved							
WR50	0xe4	R/W	Reserved							
WR51	0x34	R/W	Reserved							
WR52	0xac	R/W	Reserved							
WR53	0x04	R/W	Reserved							
WR54	0x7c	R/W	Reserved							

Register Name	Initial[1]	Type	MSB	Address						LSB
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR55	0x78	R/W	Reserved							
WR56	0x5c	R/W	Reserved							
WR57	0x9c	R/W	Reserved							
WR58	0x6c	R/W	Reserved							
WR59	0x64	R/W	Reserved							
WR5A	0x7c	R/W	Reserved							
WR5B	0x34	R/W	Reserved							
WR5C	0x7c	R/W	Reserved							
WR5D	0xff	R/W	Reserved							
WR5E	0x00	R/W	Reserved							
WR5F	0xff	R/W	Reserved							
WR60	0x8d	R/W	Reserved							
WR61	0x72	R/W	Reserved							
WR62	0xc3	R/W	Reserved							
WR63	0x00	R/W	Reserved							
WR64	0xc3	R/W	Reserved							
WR65	0xd3	R/W	Reserved							
WR66	0x1a	R/W	Reserved							
WR67	0x2c	R/W	Reserved							
WR68	0x1f	R/W	Reserved							
WR69	0x50	R/W	Reserved							
WR6A	0x00	R/W	Reserved							
WR6B	0x80	R/W	Reserved							
WR6C	0x7a	R/W	Reserved				TSPDOSC1	SWPDOSC1	TSPDOSC2	SWPDOSC2
WR6D	0xff	R/W	Reserved							
WR6E	0x00	R/W	Reserved							
WR6F	0xdf	R/W	Reserved							
WR70	0x70	R/W	Reserved							
WR71	0x70	R/W	Reserved							
WR72	0x70	R/W	Reserved							
WR73	0x70	R/W	Reserved							
WR74	0x70	R/W	Reserved							
WR75	0x70	R/W	Reserved							
WR76	0x70	R/W	Reserved							
WR77	0x00	R/W	Blank			Reserved				
WR78	0x00	R/W	Blank				Reserved			
WR79	0x00	R/W	Reserved							
WR7A	0x00	R/W	Reserved							
WRF0	0x00	R/W	Reserved							
WRF1	0x14	R/W	Reserved							
WRF2	0x00	R/W	Reserved							

[1] Note that the initialization file overrides the initial value. Contact Analog Devices to receive the latest initialization file.

I²C REGISTER DESCRIPTIONS

Table 10. Register Descriptions

Address [Bits]	Type	Name	Description
LNA			
0x20[7:6]	R/W	BAND[1:0]	LNA band selection. 0: FM, 1: Band-III, 2: Band-III, 3: L-band.
0x03[1]	R	BIASSHORT	Mode change SW. 0: steady state, 1: mode control moment (for 50 µs).
BPF Digital Block			
0x20[5]	R/W	BPFBW	BPF mode selection. 0: FM, 1: T-DMB.
0x06[4:0]	R	CTUNE[4:0]	Cap bank tuning value from digital block.
CTUNE Digital Block			
0x23[7]	R/W	CTUNE_ON	CTUNE enable/disable. 0: disable, 1: enable. Main clock and CTUNE_ON make TUNEEN signals. TUNEEN signal toggles at falling edge of main clock.
0x21[3:1]	R/W	CLKSEL[2:0]	CTUNE CLK selection. 1: 16.384 MHz, 2: 19.2 MHz, 4: 24.576 MHz.
0x07[4:0]	R	CV[4:0]	Cap bank value by tuning.
VCO and Loop Filter			
0x21[4]	R/W	PDAAC	Power-down of automatic amplitude control circuit. 0: power on ACC (default), 1: power off AAC.
0x23[5]	R/W	AAC_RN	Reset of AAC.
0x23[1]	R/W	AAC_EN	0: AAC hold, 1: AAC enable.
0x22[7:6]	R/W	DIVSEL[1:0]	Band election. 00: L-band, 01: Band-III, 11: FM.
0x23[0]	R/W	VCOBIASSW	Enable when AAC_EN is 1.
0x3B[3:0]	R/W	CONBAND[3:0]	Load resistor control words. [0]: Band_3DIV; [1]: Band_4DIV; [2]: Band-DIVIII; [3]: Band_BUF; [2]: Band_DIVIII, L-band = 0, Band-III and FM = 1.
0x0A[5:0]	R	VCORG[5:0]	Externally supplied words for tank MIM capacitance in the VCO core. Write mode: VCORGSPI (The VCORGSPI register operates when EXTVCORG is 1.) 000000: minimum, 111111: maximum.
0x0B[5:0]	R	VCOCON[5:0]	AAC bias value.
0x1A[7:0]	R	VTUNED[7:0]	ADC output of VTUNE.
PLLA			
0x22[5:0]	R/W	ICP[5:0]	Charge-pump current setting value.
0x27[7]	R/W	CAL_ON	0: hold, 1: charge pump calibration enable.
0x27[6]	R/W	PCAL_ON	0: hold, 1: charge pump initial calibration enable.
0x24[7:3]	R/W	ICP_OFS[4:0]	EICP_CALI[4:0] setting offset value. See EICP_CALI[4:0] description.
0x24[2]	R/W	ICP_EXT	Manual EICP_CALI[4:0] setting enable. See EICP_CALI[4:0] description.
0x23[4]	R/W	RN_PLL	PLL reset. 1: operation, 0: PLL reset.
0x23[3]	R/W	RN_CNT	PLL counter reset. 1: operation, 0: PLL counter reset.
0x0C[4:0]	R	EICP_CALI[4:0]	Charge-pump UP/DN current calibration code. If ICP_EXT = 0 and ICP_OFS<4) = 0, EICP_CALI[4:0] = MICP_CALO[4:0] + ICP_OFS[3:0]. If ICP_EXT = 0 and ICP_OFS<4) = 1, EICP_CALI[4:0] = MICP_CALO[4:0] – ICP_OFS[3:0]. If ICP_EXT = 1, EICP_CALI[4:0] = ICP_OFS[4:0].
0x0D[4:0]	R	MICP_CALO[4:0]	Charge-pump UP/DN current calibration result code without offset. See EICP_CALI[4:0] description.

Address [Bits]	Type	Name	Description
PLLD			
0x24[1]	R/W	PC4	Prescaler divide ratio setting. 0: 8/9, 1: 4/5.
0x25[5:0]	R/W	N[13:8]	PLL feedback divider integer value.
0x26[7:0]		N[7:0]	
0x27[3:0]	R/W	F[19:16]	PLL feedback divider fractional value.
0x28[7:0]		F[15:8]	
0x29[7:0]		F[7:0]	
0x24[0]	R/W	DTHEN	∑-Δ modulator dithering control. 0: off, 1: on.
0x03[0]	R	LOCK	PLL lock status indicator. 0: unlock, 1: lock.
ADJRSSI			
0x20[4:3]	R/W	ADJ[1:0]	RSSI attenuator gain control. 00 ~ 11: 6 dB step (minimum = 0 dB, maximum = −18 dB), default = 01.
RFRSSI			
0x20[2:0]	R/W	TOP[2:0]	RSSI attenuator gain control. 000 ~ 110: 6 dB step (minimum = 0 dB, maximum = −36 dB), default = 011.
IFRSSI			
0x25[7:6]	R/W	IFPWR[1:0]	RSSI attenuator gain control. 00 ~ 11: 6 dB step (minimum = 0 dB, maximum = −18 dB), default = 01.
RTUNE			
0x23[6]	R/W	RTUNE_ON	RTUNE enable/disable. 0: disable, 1: enable. Main clock and RTUNE_ON make RTUNE_EN signals. RTUNE_EN signal toggles at falling edge of main clock.
0x0E[5:0]	R	RTUNE[5:0]	RTUNE value. If RTUNE_EXT = 0 and RTUNEOFS[5] = 0, RTUNE[5:0] = RV[5:0] + RTUNEOFS[4:0]. If RTUNE_EXT = 0 and RTUNEOFS[5] = 1, RTUNE[5:0] = RV[5:0] − RTUNEOFS[4:0]. If RTUNE_EXT = 1, RTUNE[5:0] = RTUNEOFS[5:0].
0x0F3[5:0]	R	RV[5:0]	Internal RTUNE setting value without offset
EFUSE			
0x6E[7:3]	R/W	FUSEADDR[4:0]	Select fuse bit to write/read.
0x6E[2]	R/W	FUSERDEN	Fuse read enable. 0: disable, 1: enable.
0x6E[1]	R/W	FUSEWREN	Fuse write enable. 0: disable, 1: enable.
0x10[7:0]	R	READEFUSE[31:0]	Read fuse programming data in read mode.
0x11[7:0]			
0x12[7:0]			
0x13[7:0]			
RFAGC Digital Block			
0x17[7:0]	R	RFRSSID[7:0]	RFRSSI detection value after ADC.
0x18[7:0]	R	ADJRSSID[7:0]	ADJRSSI detection value after ADC.
0x19[7:0]	R	RFPWRDETD[7:0]	RF power detector detection value after ADC.
0x03[5:4]	R	LNAGAIN[1:0]	LNA gain state value. 0: low gain; 1,2: mid gain; 3: high gain.
0x03[3:2]	R	GVBPF[1:0]	BPF gain state value. 0: low gain (1 dB), 1: mid gain (7 dB), 2: high gain (13 dB), 3: do not use.
0x04[7:0]	R	RFAGC[7:0]	RFAGC gain state value. 0x00 : lowest gain, 0xff : highest gain.
IFAGC Digital Block			
0x27[5:4]	R/W	EXTGVBB[1:0]	GVBB selection. 0: internal, 1: I^2C, 2: external, 3: not used.
0x17[7:0]	R	IFRSSID[7:0]	IFRSSI detection value after ADC.
0x18[7:0]	R	BBAGCEXTD[7:0]	External AGC voltage value after ADC.

Address [Bits]	Type	Name	Description
0x05[7:0]	R	GVBB[7:0]	Baseband gain value. 0x00 (minimum gain) ~ 0xc3 (maximum gain).
DCOC I2C			
0x08[12:8]	R	OFSCON[12:0]	DCOC value of OCA.
0x09[7:0]			
Software Power-Down			
0x2A[7]	R/W	SWPDLNA	LNA software power-down.
0x2A[6]	R/W	SWPDRFPGA	RFPGA software power-down.
0x2A[5]	R/W	SWPDMIXER	Mixer software power-down.
0x2A[4]	R/W	SWPDBPF	BPF software power-down.
0x2A[3]	R/W	SWPDCTUNE	CTUNE software power-down.
0x2A[2]	R/W	SWPDBBPGA	BBPGA software power-down.
0x2A[1]	R/W	SWPDOUTBUF	OUTBUF software power-down.
0x2A[0]	R/W	SWPDVCO	VCO software power-down.
0x2B[7]	R/W	SWPDPLL	PLL software power-down.
0x2B[6]	R/W	SWPDPWDET	PWDET software power-down.
0x2B[5]	R/W	SWPDADJRSSI	ADJRSSI software power-down.
0x2B[4]	R/W	SWPDRFRSSI	RFRSSI software power-down.
0x2B[3]	R/W	SWPDIFRSSI	IFRSSI software power-down.
0x2B[2]	R/W	SWPDTMPSNS	TMPSNS software power-down.
0x2B[1]	R/W	SWPDRTUNE	RTUNE software power-down.
0x2B[0]	R/W	SWPDDADC	ADC software power-down.
0x2C[7]	R/W	SWPDDLDO	LDO software power-down.
0x2C[6]	R/W	SWPDBGR	BGR software power-down.
0x6C[2]	R/W	SWPDOSC1	Xtal oscillator software Power-Down 1.
0x6C[0]	R/W	SWPDOSC2	Xtal oscillator software Power-Down 2.
Time-Slicing Power-Down			
0x2C[5]	R/W	TSPDLNA	LNA time-slicing power-down enable.
0x2C[4]	R/W	TSPDPGA	RFPGA time-slicing power-down enable.
0x2C[3]	R/W	TSPDMIXER	Mixer time-slicing power-down enable.
0x2C[2]	R/W	TSPDBPF	BPF time-slicing power-down enable.
0x2C[1]	R/W	TSPDCTUNE	CTUNE time-slicing power-down enable.
0x2C[0]	R/W	TSPDBBPGA	BBPGA time-slicing power-down enable.
0x2D[7]	R/W	TSPDOUTBUF	OUTBUF time-slicing power-down enable.
0x2D[6]	R/W	TSPDVCO	VCO time-slicing power-down enable.
0x2D[5]	R/W	TSPDPLL	PLL time-slicing power-down enable.
0x2D[4]	R/W	TSPDPWDET	PWDET time-slicing power-down enable.
0x2D[3]	R/W	TSPDADJRSSI	ADJRSSI time-slicing power-down enable.
0x2D[2]	R/W	TSPDRFRSSI	RFRSSI time-slicing power-down enable.
0x2D[1]	R/W	TSPDIFRSSI	IFRSSI time-slicing power-down enable.
0x2D[0]	R/W	TSPDTMPSNS	TMPSNS time-slicing power-down enable.
0x2E[7]	R/W	TSPDRTUNE	RTUNE time-slicing power-down enable.
0x2E[6]	R/W	TSPDADC	ADC time-slicing power-down enable.
0x2E[5]	R/W	TSPDLDO	LDO time-slicing power-down enable.
0x2E[4]	R/W	TSPDBGR	BGR time-slicing power-down enable.
0x6C[3]	R/W	TSPDOSC1	Xtal oscillator time-slicing Power-Down 1.
0x6C[1]	R/W	TSPDOSC2	Xtal oscillator time-slicing Power-Down 2.
Miscellaneous			
0x19[7:0]	R	TMPSNSD[7:0]	ADC output of temperature sensor.

OUTLINE DIMENSIONS

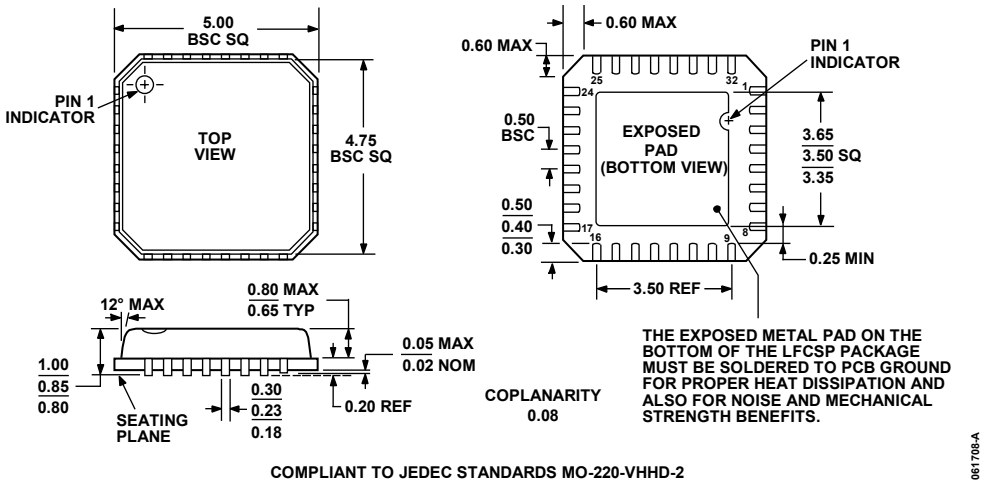


Figure 32. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Band	Temperature Range	Package Description	Package Option
ADMTV300ACPZRL[1]	Band-III	−40°C to + 85°C	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-4
ADMTV300BCPZRL[1]	Band-III, FM, L-Band	−40°C to + 85°C	32-Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-4
ADMTV300A-EBZ[1]	Band-III		Evaluation Board	
ADMTV300B-EBZ[1]	Band-III, FM, L-Band		Evaluation Board	

[1] Z = RoHS Compliant Part.

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