Mobile TV One-chip Receiver for T-DMB/DAB/FM

Preliminary Technical Data

ADMTV315

FEATURES

RF Tuner and Demodulator SoC for T-DMB/DAB/FM
Supports Triple-band: Band III, L-Band and FM
Wide Dynamic Range: –102dBm to +5dBm in 50Ω
Low Power Consumption
CSP_BGA Package: 75mW@TDMB_Video_544kbps
CSP Package: 65mW@TDMB_Video_544kbps
Reference Clock
CSP_BGA Package: 16.384/19.2MHz
CSP Package: 16.384MHz
1.2V Supply Voltage for Core and 1.8/2.8V Dual Supply Voltage selectable for I/O
Supports JTAG I/O Boundary Scan
Fully Compliant to T-DMB Standards in Korea and ETSI 300 401 Physical Layer Definition
Satisfied TTAS.KO-07.0024 Specification of the data Services for VHF Digital Multimedia Broadcasting
Supports ETSI EN 300 744 (204,188) Outer Coder
144-Ball Chip Scale Package Ball Grid Array (CSP_BGA) and 92-Ball Chip Scale Package (CSP)
CSP_BGA Package 7mm × 7mm × 1.0mm, 0.5mm pitch
CSP Package 5mm × 5mm × 0.75mm, 0.45mm pitch

FUNCTIONAL BLOCK DIAGRAM

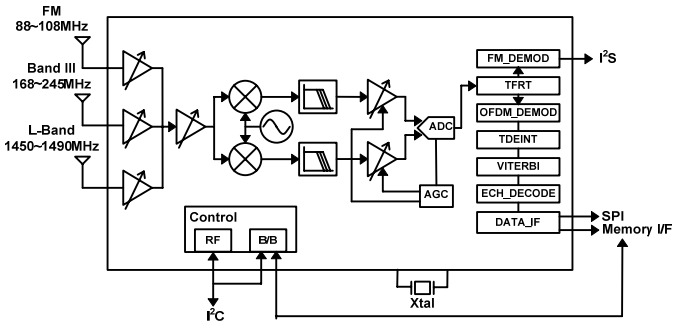

Figure 1. ADMTV315 Block diagram

GENERAL DESCRIPTION

ADMTV315 is a highly integrated SoC (System-on-Chip) T-DMB/DAB receiver, which supports triple bands (Band III, L-Band and FM). This device is composed of high performance RF front-end tuner and OFDM (Orthogonal Frequency Division Multiplex) demodulator in a small-size single package. The zero-IF down-conversion RF front-end includes LNA, RF PGA, mixer, high-resolution fractional-N PLL, on-chip low phase noise VCO, BB PGA, and automatic cutoff frequency-tuning LPF. The baseband of ADMTV315 includes 10bit ADC, OFDM demodulator and FEC/audio/data decoders. This device supports various serial interfaces such as I2C, I2S, and SPI to make interface with external devices more flexible. With good sensitivity and wide dynamic range, ADMTV315 is the best solution for T-DMB/DAB application. It is designed to comply with TTAS.KO-07.0024 specification of the data services for VHF Digital Multimedia Broadcasting (T-DMB) and ETSI EN 300 401 (European DAB).

The additional features of ADMTV315 are as follows:

- Supports transmission mode 1, 2, 3 and 4
- Supports digital frequency control and timing control
- Supports simultaneous channel reception
  - Maximum 64 sub-channels
  - 4 enhanced channels (TDMB/ESM/EPM)
- Supports various AP (HOST) interfaces
  - SRAM Base parallel interface (control + data)
  - Serial interface (control: I²C, data: SPI)
  - Single SPI interface at PIP mode
- Supports TII reception
- Supports FM reception
- Supports automatic setting with Multiplex Configuration Information decoder
  - CIF counter synchronization
  - Multiplex configuration & reconfiguration
  - Enhanced channel (TDMB/EPM)
- Supports full capacity channel decoding
- Minimized external components
  - No external system memory
  - Bit de-interleaver memory included

Rev. PrA

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REVISION HISTORY

SPECIFICATIONS

OPERATING CONDITIONS

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD} (1.2 V)	1.1		1.3	V
	V_{DD} (1.8 V)	1.65		1.95	V
	V_{DD} (2.8 V)	2.5		3.3	V
Input/Output Voltage	V_{IN}/V_{OUT}	1.65		1.95	V
		2.5		3.3	V
Operating Ambient Temperature	T_{opr}	−40		85	°C

ELECTRICAL CHARATERISTICS

T_A = 25°C, all 1.8 V supplies = 1.65 V to 1.95 V, unless otherwise noted.

Table 2. 1.8 V DC Electrical Characteristics

Parameter	Condition		Symbol	Min	Typ	Max	Unit
Input High Current	Normal	$V_{IN} = V_{DD}$	I_{IH}	−5		5	µA
	Down	Pull - Down		1		30	µA
Input Low Current	Normal	$V_{IN} = V_{SS}$	I_{IL}	−5		5	µA
	Up	Pull - Up		−30		−1	µA
Input High Voltage	CMOS		V_{IH}	0.65×V_{DD}			V
Input High Voltage	SCMOS		V_{T+}			0.7×V_{DD}	V
Input Low Voltage	CMOS		V_{IL}			0.35×V_{DD}	V
Input Low Voltage	SCMOS		V_{T-}	0.3×V_{DD}			V
Output High Voltage	I_{OH} = Drive Current		V_{OH}	V_{DD} − 0.45			V
Output Low Voltage	I_{OL} = Drive Current		V_{OL}			0.45	V
Tri-state Output Leakage Current	$V_{OUT} = V_{DD}$ of V_{SS}		I_{OZ}	−10		10	µA

T_A = 25°C, all 2.8 V supplies = 2.5 V to 3.1 V, unless otherwise noted.

Table 3. 2.8 V DC Electrical Characteristics

Parameter	Condition		Symbol	Min	Typ	Max	Unit
Input High Current	$V_{IN} = V_{DD}$	Normal	I_{IH}	−5		5	µA
	Pull - Down	Down		5		60	µA
Input Low Current	$V_{IN} = V_{SS}$	Normal	I_{IL}	−5		5	µA
	Pull - Up	Up		−60		−5	µA
Input High Voltage	CMOS		V_{IH}	0.65×V_{DD}			V
Input High Voltage	SCMOS		V_{T+}			0.7×V_{DD}	V
Input Low Voltage	CMOS		V_{IL}			0.35×V_{DD}	V
Input Low Voltage	SCMOS		V_{T-}	0.3×V_{DD}			V
Output High Voltage	I_{OH} = Drive Current		V_{OH}	V_{DD} − 0.45			V
Output Low Voltage	I_{OL} = Drive Current		V_{OL}			0.45	V
Tri-state Output Leakage Current	$V_{OUT} = V_{DD}$ of V_{SS}		I_{OZ}	−10		10	µA

T_A = 25°C, all 1.2 V supplies = 1.1 V to 1.3 V, 2.8 V supplies = 2.7 V to 2.9 V, unless otherwise noted.

Table 4. FM AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
FM RF frequency range	f_{FM}	88		108	MHz
RF input impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
Sensitivity	P_{MIN}		7		dBµV

T_A = 25°C, all 1.2 V supplies = 1.1 V to 1.3 V, 2.8 V supplies = 2.7 V to 2.9 V, unless otherwise noted.

Table 5. Band III AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Band-III RF frequency range	$f_{Band-III}$	168		245	MHz
RF input impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
Sensitivity @ BER	P_{MIN}		−102	−97	dBm
Max Input Power @ BER	P_{MAX}	+5			dBm
Digital Adjacent Chanel Rejection (n+1)	ACR_{DN+1}	33	38		dBc
Digital Adjacent Chanel Rejection (n−1)	ACR_{DN-1}	33	38		dBc
Far-off (+5 MHz)	FO_{+5MHz}	42	47		dBc
Far-off (−5 MHz)	FO_{-5MHz}	42	47		dBc

T_A = 25°C, all 1.2 V supplies = 1.1 V to 1.3 V, 2.8 V supplies = 2.7 V to 2.9 V, unless otherwise noted.

Table 6. L-Band AC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
L-Band RF frequency range	f_{L-Band}	1450		1492	MHz
RF input impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
Sensitivity	P_{MIN}		−101	−97	dBm
Max Input Power	P_{MAX}	0			dBm
Digital Adjacent Chanel Rejection (n+1)	ACR_{DN+1}	30	33		dBc
Digital Adjacent Chanel Rejection (n−1)	ACR_{DN-1}	30	33		dBc
Far-off (+5 MHz)	FO_{+5MHz}	40	47		dBc
Far-off (−5 MHz)	FO_{-5MHz}	40	47		dBc

DIGITAL TIMING CHARACTERISTICS

Table 7.

Characteristic	Symbol	Min	Unit
PD Set-up Margin	a	Don't Care	µs
Power up Set-up Margin for V_{DD18}	b	Don't Care	µs
Power up Set-up Margin for V_{DDIO}	c	Don't Care	µs
RESETB Set-up Time for RESETB	d	100	µs
Set-up Time for I^2C Interface	e	100	µs

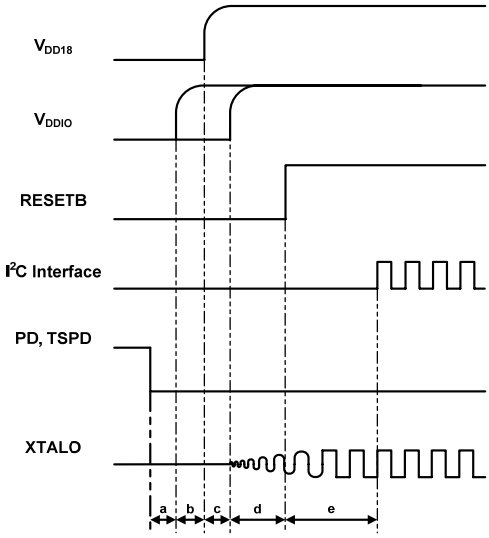


Figure 2. Digital Timing Diagram

ELECTROSTATIC CHARATERISTICS

Table 8.

Characteristic	HBM	MM	Remarks
V_{DD} positive	> 1000 [V]	>100 [V]	
V_{DD} negative	> 1000 [V]	>100 [V]	
Vss positive	> 1000 [V]	>100 [V]	
Vss negative	> 1000 [V]	>100 [V]	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Rating
DC Supply Voltage	V_{DD} (1.2V)	1.7 V
	V_{DD} (1.8V)	2.3 V
	V_{DD} (2.8V)	3.3 V
Input/Output Voltage	V_{IN}/V_{OUT} (1.2V)	1.7 V
	V_{IN}/V_{OUT} (1.8V)	2.3 V
	V_{IN}/V_{OUT} (2.8V)	3.3 V
DC Input Current	L_{IN}	±200mA
Storage Temperature	Tstg	–65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN MAP (BGA PACKAGE TYPE)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	LS	LRFIN	B3RFIN	FMRFIN	RBIAS	GND	GND	GNDISOA2	VSS12_RXADC_A_Q	REFBOT	VDD12_RXADC_D	VSS12	HOLD_AGC	A
B	B3LNAOUT	B3S	RFGND5	NC	BBQNTP	BBIPTP	VDD12DIG	NC	GNDISOD2	REFTOP	VDD12_RXADC_A_I	AGC_CON	VTG_AP_S	B
C	B3PGAIN	VDD12RF1	VDD12BB	NC	BBQPTP	BBINTP	RFGND6	VDD12FUSE	VDD12_RXADC_A_Q	VSS12_RXADC_A_Q	VDD12	LNA_CON	SI2C_RF_AS0	C
D	RFGND3	VDD12RF2	RFIND	RFGND4	GND	GND	GND	RFGND6	CML	VSS12_RXADC_A_I	VTG_AP_P	SI2C_RF_AS1	CLK_OUT	D
E	RFGND2	VDD12VCO	REGCAP	LFO						VSS28	VDD28	VSS28_XTAL	XTAL_OUT	E
F	RFGND1	VDD12PLL	VDD12CP	GNDISOA1						VDD12	VSS12	VDD28_XTAL	XTAL_IN	F
G	GND	GND	GND	GND						VDD12_CLK_PLL	CLK_PLL_FILTER	VBB_VSSA_VSSD12_CLK_PLL	GND	G
H	GNDISOD1	VDD12	VSS12	VSS28						PIP_REQ	PIP_SPI_CLK_SCK	PIP_SPI_DATA_SD	PIP_SPI_EN_WS	H
J	VDD28	CHIPSEL	MODE1	MODE2						VDD18_28_AP_S	SI2C_RF_SCL	SI2C_RF_SDA	PIP_DEMAND	J
K	MODE0	OSCSEL	TMS	TDO	VSS18_28_AP_P	HOST_ADDR1	HOST_DATA0	HOST_DATA6	VSS18_28_AP_P	AP_DEMAND_SPI_INT	INT	RESOUTB	VSS18_28_AP_S	K
L	MODE3	TDI	HOST_ADDR10	HOST_ADDR7	HOST_ADDR4	OEB	HOST_DATA2	HOST_DATA4	VDD18_28_AP_P	HOST_DATA11	HOST_DATA14	SPI_EN	RESINB	L
M	TRSTB	HOST_ADDR11	HOST_ADDR8	HOST_ADDR5	HOST_ADDR3	CSB	VDD12	HOST_DATA3	HOST_DATA7	HOST_DATA10	HOST_DATA13	SPI_CLK	SPI_DATA	M
N	TCK	HOST_ADDR9	HOST_ADDR6	VDD18_28_AP_P	HOST_ADDR2	WEB	HOST_DATA1	VSS12	HOST_DATA5	HOST_DATA8	HOST_DATA9	HOST_DATA12	HOST_DATA15	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

ADMTV315
Top View
7×7 mm BGA 144 balls

Figure 3. BGA Package Pin Map (Top View)

Table 10. Operation Mode

Operation Mode	MODE3	MODE2	MODE1	MODE0	CHIPSEL
NORMAL 1	1	1	1	1	1
NORMAL 2	1	1	1	0	1
CHIP_DISABLE	X	X	X	X	0

Normal 1: Host Memory interface (Parallel I/F) used for DMB BB register access

Normal 2: I^2C interface (Serial I/F) used for DMB BB register access (I^2C is used for RF register access in normal 1 and 2.)

Table 11. Dual Voltage Selection

Voltage Selection Pin	Value	Voltage Selection
VTG_AP_P	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Parallel Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Parallel Interface with AP
VTG_AP_S	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Serial Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Serial Interface with AP

Voltage source and IO list influenced by VTG_AP_P (Parallel I/F IO)

- Voltage source: VDD 18_28_AP_P
- IO: CSB, OEB, WEB, HOST_ VDD R (11:1), HOST_DATA (15:0)

Voltage source and IO list influenced by VTG_AP_S (Serial I/F IO and IO connected to AP)

- Voltage source: VDD 18_28_AP_S
- IO: INT, RESINB, RESOUTB, SI2C_RF_SCL, SI2C_RF_SDA, SPI_CLK, SPI_DATA, SPI_EN, AP_DEMAND_SPI_INT, PIP_SPI_CLK_SCK, PIP_SPI_DATA_SD, PIP_SPI_EN_WS, PIP_DEMAND, PIP_REQ

Table 12. Pin Function Descriptions (BGA Package Type)

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
Clock, Reset, Mode, VTG, CHIPSEL (13 Pin)						
MODE0	K1	I	2.8	IS-PU		MODE selection 0
MODE1	J3	I	2.8	IS-PU		MODE selection 1
MODE2	J4	I	2.8	IS-PU		MODE selection 2
MODE3	L1	I	2.8	IS-PU		MODE selection 3
XTAL_IN	F13	I	2.8	IXA		XTAL clock input
XTAL_OUT	E13	O	2.8	OXA		XTAL clock output
CLK_OUT	D13	O	2.8	Z5	5	Clock output
OSCSEL	K2	I	2.8	IS-PD		Oscillator selection 0: 16.384 MHz 1: 19.2 MHz
RESINB	L13	I	1.8/2.8	ISL		Chip reset & AP I/F Hi-Z control (when chip off, maintain RESINB=L)
RESOUTB	K12	O	1.8/2.8	Z5	5	Reset output
VTG_AP_P	D11	I	2.8	IS-PU		AP IO voltage selection for parallel interface
VTG_AP_S	B13	I	2.8	IS-PU		AP IO voltage selection for serial interface
CHIPSEL	J2	I	2.8	IS-PD		Test chip selection in PiP test
RF Interface (3 Pin)						
AGC_CON	B12	O	2.8	Z5-PD	5	Automatic gain control signal
LNA_CON	C12	O	2.8	Z5-PD	5	LNA step control signal
HOLD_AGC	A13	O	2.8	Z5-PD	5	AGC hold control for null period
Application Processor Interface (31 Pin)						
HOST_ADDR1	K6	I	1.8/2.8	IS-PD		AP parallel interface address 1
HOST_ADDR2	N5	I	1.8/2.8	IS-PD		AP parallel interface address 2
HOST_ADDR3	M5	I	1.8/2.8	IS-PD		AP parallel interface address 3
HOST_ADDR4	L5	I	1.8/2.8	IS-PD		AP parallel interface address 4
HOST_ADDR5	M4	I	1.8/2.8	IS-PD		AP parallel interface address 5
HOST_ADDR6	N3	I	1.8/2.8	IS-PD		AP parallel interface address 6
HOST_ADDR7	L4	I	1.8/2.8	IS-PD		AP parallel interface address 7
HOST_ADDR8	M3	I	1.8/2.8	IS-PD		AP parallel interface address 8
HOST_ADDR9	N2	I	1.8/2.8	IS-PD		AP parallel interface address 9
HOST_ADDR10	L3	I	1.8/2.8	IS-PD		AP parallel interface address 10
HOST_ADDR11	M2	I	1.8/2.8	IS-PD		AP parallel interface address 11
CSB	M6	I	1.8/2.8	ISL-PU		Chip select
WEB	N6	I	1.8/2.8	ISL-PU		Write Enable
INT	K11	O	1.8/2.8	O3	3	Interrupt
OEB	L6	I	1.8/2.8	ISL-PU		Out Enable
HOST_DATA0	K7	B	1.8/2.8	BX3-KP	3	AP parallel interface data 0
HOST_DATA1	N7	B	1.8/2.8	BX3-KP	3	AP parallel interface data 1
HOST_DATA2	L7	B	1.8/2.8	BX3-KP	3	AP parallel interface data 2
HOST_DATA3	M8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 3
HOST_DATA4	L8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 4
HOST_DATA5	N9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 5
HOST_DATA6	K8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 6
HOST_DATA7	M9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 7
HOST_DATA8	N10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 8
HOST_DATA9	N11	B	1.8/2.8	BX3-KP	3	AP parallel interface data 9
HOST_DATA10	M10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 10

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
HOST_DATA11	L10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 11
HOST_DATA12	N12	B	1.8/2.8	BX3-KP	3	AP parallel interface data 12
HOST_DATA13	M11	B	1.8/2.8	BX3-KP	3	AP parallel interface data 13
HOST_DATA14	L11	B	1.8/2.8	BX3-KP	3	AP parallel interface data 14
HOST_DATA15	N13	B	1.8/2.8	BX3-KP	3	AP parallel interface data 15
SPI Interface (4 Pin)						
SPI_CLK	M12	B	1.8/2.8	BS3-PD	3	SPI interface clock signal
SPI_EN	L12	B	1.8/2.8	BS3-PU	3	SPI interface enable signal
SPI_DATA	M13	B	1.8/2.8	BS3-PD	3	SPI interface data signal
AP_DEMAND_SPI_INT	K10	B	1.8/2.8	BS3-PU	3	SPI interface demand/interrupt
I²S Interface (3 Pin) / PiP Interface (5 Pin)						
PIP_DEMAND	J13	I	1.8/2.8	IS-PD		PIP demand
PIP_REQ	H10	O	1.8/2.8	O3	3	PIP request
PIP_SPI_CLK_SCK	H11	B	1.8/2.8	BS3-PD	3	I2S Serial Clock/PIP SPI clock
PIP_SPI_EN_WS	H13	B	1.8/2.8	BS3-PU	3	I2S Word Select/PIP SPI enable
PIP_SPI_DATA_SD	H12	B	1.8/2.8	BS3-PD	3	I2S Serial Data/PIP SPI data
I²C Interface (4 Pin)						
SI2C_RF_SCL	J11	B	2.8	BS3-OD-PUC		I2C interface serial clock
SI2C_RF_SDA	J12	B	2.8	BS3-OD-PUC		I2C interface serial data
SI2C_RF_AS0	C13	I	2.8	IS-PD		I2C interface slave address 0
SI2C_RF_AS1	D12	I	2.8	IS-PD		I2C interface slave address 1
JTAG Interface (5 Pin)						
TCK	N1	I	2.8	IS-PU		JTAG port for clock
TDO	K4	O	2.8	Z3	3	JTAG port for data output
TDI	L2	I	2.8	IS-PU		JTAG port for data input
TRSTB	M1	I	2.8	ISL-PU		JTAG port for reset
TMS	K3	I	2.8	IS-PU		JTAG port for mode select
CLK64_PLL (1 Pin)						
CLK_PLL_FILTER	G11	O		AO		Clock PLL Filter
RX-ADC (3 Pin)						
REFTOP	B10	O		AO		ADC reference top
REFBOT	A10	O		AO		ADC reference bottom
CML	D9	O		AO		ADC common mode level
1.2 Analog RX-ADC Power/Ground (6 Pin)						
VDD12_RXADC_A_I	B11		1.2	P		
VSS12_RXADC_A_I	D10		1.2	G		
VDD12_RXADC_A_Q	C9		1.2	P		
VSS12_RXADC_A_Q	A9		1.2	G		
VDD12_RXADC_D	A11		1.2	P		
VSS12_RXADC_D	C10		1.2	G		
1.2 V Digital Core Power/Ground (8 Pin)						
VDD12	H2		1.2	P		
VDD12	M7		1.2	P		
VDD12	F10		1.2	P		
VDD 12	C11		1.2	P		
VSS12	H3		1.2	G		
VSS12	N8		1.2	G		

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
VSS12	F11		1.2	G		
VSS12	A12		1.2	G		
2.8 V XTAL I/O Power/Ground (2 Pin)						
VDD 28_XTAL	F12		2.8	P		
VSS28_XTAL	E12		2.8	G		
2.8 V Digital I/O Power/Ground (4 Pin)						
VDD 28	J1		2.8	P		
VDD 28	E11		2.8	P		
VSS28	H4		2.8	G		
VSS28	E10		2.8	G		
1.8/2.8 V Digital I/O Power/Ground (Dual Mode for Application Processor Interface) (6 Pin)						
VDD 18_28_AP_P	N4		1.8/2.8	P		
VDD 18_28_AP_P	L9		1.8/2.8	P		
VSS18_28_AP_P	K5		1.8/2.8	G		
VSS18_28_AP_P	K9		1.8/2.8	G		
VDD 18_28_AP_S	J10		1.8/2.8	P		
VSS18_28_AP_S	K13		1.8/2.8	G		
1.2 V Analog CLK_PLL Power/Ground (3 Pin)						
VDD 12_CLK_PLL	G10		1.2	P		
VBB_VSSA_VSSD12 _CLK_PLL	G12		1.2	G		
GND	G13		1.2	G		
RF Block (46 Pin)						
LS	A1	IO	1.2	PRF		L-band LNA source
LRFIN	A2	I	1.2	PRF		L-band RF input
B3RFIN	A3	I	1.2	PRF		Band-III RF input
FMRFIN	A4	I	1.2	PRF		FM RF input
RBIAS	A5	IO	1.2	PA		Bias resistor
GND	A6	G	1.2	G		Ground
GND	A7	G	1.2	G		Ground
GNDIOA2	A8	G	1.2	G		Ground
B3LNAOUT	B1	O	1.2	PRF		Band-III LNA output
B3S	B2	IO	1.2	PRF		Band-III LNA source
RFGND5	B3	G	1.2	G		Ground
RFRSSI	B4	O	1.2	PA		RFRSSI test point
BBQNTP	B5	IO	1.2	PA		Baseband QN test point
BBIPTP	B6	IO	1.2	PA		Baseband IP test point
VDD 12DIG	B7	P	1.2	PA		Power supply for digital
NC	B8					No connection
GNDISOD2	B9	G	1.2	G		Ground
B3PGAIN	C1	I	1.2	PRF		Band-III PGA input
VDD 12RF1	C2	P	1.2	P		Power supply for RF
VDD 12BB	C3	P	1.2	P		Power supply for analog baseband
BBAGC	C4	I	1.2	PA		Baseband AGC input (DC voltage)
BBQPTP	C5	IO	1.2	PA		Baseband QP test point
BBINTP	C6	IO	1.2	PA		Baseband IN test point
RFGND6	C7	G	1.2	G		Ground
VDD 12FUSE	C8	P	1.2	P		Power supply for fuse
RFGND3	D1	G	1.2	G		Ground

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
VDD 12RF2	D2	P	1.2	P		Power supply for RF
RFIND	D3	IO	1.2	PRF		RF inductor
RFGND4	D4	G	1.2	G		Ground
GND	D5	G	1.2	G		Ground
GND	D6	G	1.2	G		Ground
GND	D7	G	1.2	G		Ground
RFGND6	D8	G	1.2	G		Ground
RFGND2	E1	G	1.2	G		Ground
VDD 12VCO	E2	P	1.2	P		Power supply for VCO
RFGCAP	E3	IO	1.2	PA		Regulator bypass capacitor
LFO	E4	IO	1.2	PA		Loop filter
RFGND1	F1	G	1.2	G		Ground
VDD 12PLL	F2	P	1.2	P		Power supply for PLL
VDD 12CP	F3	P	1.2	P		Power supply for charge pump
GNDISOA1	F4	G	1.2	G		Ground
GND	G1	G	1.2	G		Ground
GND	G2	G	1.2	G		Ground
GND	G3	G	1.2	G		Ground
GND	G4	G	1.2	G		Ground
GNDISOD1	H1	G	1.2	G		Ground

[1] P = power, G = ground, I = input, O = output, B = bi-direction, D = dual voltage, ZO = tri-state output, AI = analog input, AO = analog output, PU = pull-up, PD = pull-down, S = Schmitt trigger, FS = fail safe IO, OD = open drain, KP = contains busholder, SI = TCXO input, XA = Xtal.

PIN MAP (ADMTV315ACBZRL WLCSP PACKAGE TYPE)

	1	2	3	4	5	6	7	8	9	10	
A	NA	B3PGAIN	RFIND	NC	VDD12CP	GND	VDD12	CHIPSEL	HOST_ADDR 11	HOST_ADDR 10	A
B	B3RFIN	B3LNAOUT	VDD12RF2	VDD12SYN	LFO	GND	VDD28	HOST_ADDR 9	HOST_ADDR 8	HOST_ADDR 7	B
C	RBIAS	GND	VDD12RF1 _BB	GND	GND	MODE	VDD18_28_ AP_P	HOST_ADDR 6	HOST_ADDR 5	HOST_ADDR 4	C
D	BBIPTP	BBQPTP	GND	NC	NC	GND	OEB	HOST_ADDR 1	HOST_ADDR 3	HOST_ADDR 2	D
E	VDD12FUSE	VDD12DIG	GND	NC	NC	GND	WEB	CSB	HOST_DATA 1	HOST_DATA 0	E
F	GND	GND	NC	NC	NC	VDD12	HOST_DATA 2	HOST_DATA 5	HOST_DATA 4	HOST_DATA 3	F
G	VDD12_RX ADC_A_Q	VDD12_RX ADC_D	GND	GND	GND	GND	VDD18_28_A P_P	HOST_DATA 8	HOST_DATA 7	HOST_DATA 6	G
H	VDD12_RX ADC_A_I	VTG_AP_P	GND	VDD12	VDD18_28 _AP_S	HOST_DATA 15	HOST_DATA 14	HOST_DATA 11	HOST_DATA 10	HOST_DATA 9	H
J	VDD12	SI2C_RF_ AS1	VDD28_ XTAL	XTAL_OUT	VDD12_ CLK_PLL	SI2C_RF _SCL	AP_DEMAND_ SPI_INT	SPI_EN	HOST_DATA 13	HOST_DATA 12	J
K	VTG_AP_S	SI2C_RF_ AS0	VDD28	XTAL_IN	CLK_PLL _FILTER	SI2C_RF_ SDA	RESINB	INT	SPI_DATA	SPI_CLK	K
	1	2	3	4	5	6	7	8	9	10	

Figure 4.ADMTV315ACBZRL WLCSP Package Pin Map (Top View)

Table 13. Operation Mode

Operation Mode[Pin No.]	MODE[C6]	CHIPSEL[A8]
NORMAL 1	0	1
NORMAL2	1	1
CHIP_DISABLE	X	0

Normal 1: I²C interface (Serial I/F) used for DMB Base-Band register and RF register access.

Normal 2: Host Memory interface (Parallel I/F) used for DMB Base-Band register access.

Table 14. Dual Voltage Selection

Voltage Selection Pin [Pin No.]	Value	Voltage Selection
VTG_AP_P[H2]	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Serial & Parallel Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Serial & Parallel Interface with AP
VTG_AP_S[K1]	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Serial Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Serial Interface with AP

Voltage source and IO list influenced by VTG_AP_P (Parallel I/F IO)

- Voltage source: VDD 18_28_AP_P
- IO: CSB, OEB, WEB, HOST_ VDD R (11:1), HOST_DATA (15:0)

Voltage source and IO list influenced by VTG_AP_S (Serial I/F IO and IO connected to AP)

- Voltage source: VDD 18_28_AP_S
- IO: INT, RESINB, RESOUTB, SI2C_RF_SCL, SI2C_RF_SDA, SPI_CLK, SPI_DATA, SPI_EN, AP_DEMAND_SPI_INT, PIP_SPI_CLK_SCK, PIP_SPI_DATA_SD, PIP_SPI_EN_WS, PIP_DEMAND, PIP_REQ

Table 15. Pin Function Descriptions (WLCSP Package Type)

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
Clock, Reset, Mode, VTG, CHIPSEL (7 Pin)						
MODE	C6	I	2.8	IS-PU		MODE selection
XTAL_IN	K4	I	2.8	IXA		XTAL clock input
XTAL_OUT	J4	O	2.8	OXA		XTAL clock output
RESINB	K7	I	1.8/2.8	ISL		Chip reset & AP I/F Hi-Z control (when chip off, maintain RESINB=L)
VTG_AP_P	H2	I	2.8	IS-PU		AP IO voltage selection for parallel interface
VTG_AP_S	K1	I	2.8	IS-PU		AP IO voltage selection for serial interface
CHIPSEL	A8	I	2.8	IS-PD		Test chip selection in PiP test
Application Processor Interface (31 Pin)						
HOST_ADDR1	D8	I	1.8/2.8	IS-PD		AP parallel interface address 1
HOST_ADDR2	D10	I	1.8/2.8	IS-PD		AP parallel interface address 2
HOST_ADDR3	D9	I	1.8/2.8	IS-PD		AP parallel interface address 3
HOST_ADDR4	C10	I	1.8/2.8	IS-PD		AP parallel interface address 4
HOST_ADDR5	C9	I	1.8/2.8	IS-PD		AP parallel interface address 5
HOST_ADDR6	C8	I	1.8/2.8	IS-PD		AP parallel interface address 6
HOST_ADDR7	B10	I	1.8/2.8	IS-PD		AP parallel interface address 7
HOST_ADDR8	B9	I	1.8/2.8	IS-PD		AP parallel interface address 8
HOST_ADDR9	B8	I	1.8/2.8	IS-PD		AP parallel interface address 9
HOST_ADDR10	A10	I	1.8/2.8	IS-PD		AP parallel interface address 10
HOST_ADDR11	A9	I	1.8/2.8	IS-PD		AP parallel interface address 11
CSB	E8	I	1.8/2.8	ISL-PU		Chip select
WEB	E7	I	1.8/2.8	ISL-PU		Write Enable
INT	K8	O	1.8/2.8	O3	3	Interrupt
OEB	D7	I	1.8/2.8	ISL-PU		Out Enable
HOST_DATA0	E10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 0
HOST_DATA1	E9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 1
HOST_DATA2	F7	B	1.8/2.8	BX3-KP	3	AP parallel interface data 2
HOST_DATA3	F10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 3
HOST_DATA4	F9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 4
HOST_DATA5	F8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 5
HOST_DATA6	G10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 6
HOST_DATA7	G9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 7
HOST_DATA8	G8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 8
HOST_DATA9	H10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 9
HOST_DATA10	H9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 10
HOST_DATA11	H8	B	1.8/2.8	BX3-KP	3	AP parallel interface data 11
HOST_DATA12	J10	B	1.8/2.8	BX3-KP	3	AP parallel interface data 12
HOST_DATA13	J9	B	1.8/2.8	BX3-KP	3	AP parallel interface data 13
HOST_DATA14	H7	B	1.8/2.8	BX3-KP	3	AP parallel interface data 14
HOST_DATA15	H6	B	1.8/2.8	BX3-KP	3	AP parallel interface data 15
SPI Interface (4 Pin)						
SPI_CLK	K10	B	1.8/2.8	BS3-PD	3	SPI interface clock signal
SPI_EN	J8	B	1.8/2.8	BS3-PU	3	SPI interface enable signal
SPI_DATA	K9	B	1.8/2.8	BS3-PD	3	SPI interface data signal
AP_DEMAND_SPI_INT	J7	B	1.8/2.8	BS3-PU	3	SPI interface demand/interrupt
I^2C Interface (4 Pin)						
SI2C_RF_SCL	J6	B	2.8	BS3-OD-		I^2C interface serial clock

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
				PUC		
SI2C_RF_SDA	K6	B	2.8	BS3-OD-PUC		I^2C interface serial data
SI2C_RF_AS0	K2	I	2.8	IS-PD		I^2C interface slave address 0
SI2C_RF_AS1	J2	I	2.8	IS-PD		I^2C interface slave address 1
CLK64_PLL (1 Pin)						
CLK_PLL_FILTER	K5	O		AO		Clock PLL Filter
1.2 Analog RX-ADC Power(3 Pin)						
VDD12_RXADC_A_I	H1		1.2	P		
VDD12_RXADC_A_Q	G1		1.2	P		
VDD12_RXADC_D	G2		1.2	P		
1.2 V Digital Core Power (4 Pin)						
VDD12	A7		1.2	P		
VDD12	F6		1.2	P		
VDD12	H4		1.2	P		
VDD 12	J1		1.2	P		
2.8 V XTAL I/O Power (1 Pin)						
VDD 28_XTAL	J3		2.8	P		
2.8 V Digital I/O Power (2 Pin)						
VDD28	B7		2.8	P		
VDD28	K3		2.8	P		
1.8/2.8 V Digital I/O Power/Ground (Dual Mode for Application Processor Interface) (3 Pin)						
VDD18_28_AP_P	C7		1.8/2.8	P		
VDD18_28_AP_P	G7		1.8/2.8	P		
VDD18_28_AP_S	H5		1.8/2.8	P		
1.2 V Analog CLK_PLL Power (1 Pin)						
VDD12_CLK_PLL	J5		1.2	P		
BASE BAND Ground (11 Pin)						
GND	A6		1.2	G		
GND	B6		1.2	G		
GND	D6		1.2	G		
GND	E6		1.2	G		
GND	F1		1.2	G		
GND	F2		1.2	G		
GND	G3		1.2	G		
GND	G4		1.2	G		
GND	G5		1.2	G		
GND	G6		1.2	G		
GND	H3		1.2	G		
RF Block (20 Pin)						
NA	A1					Not assign
B3PGAIN	A2	I	1.2	PRF		Band-III PGA input
RFIND	A3	IO	1.2	PRF		RF inductor
VDD12CP	A5	P	1.2	P		Power supply for charge pump
B3RFIN	B1	I	1.2	PRF		Band-III RF input
B3LNAOUT	B2	O	1.2	PRF		Band-III LNA output
VDD12RF2	B3	P	1.2	P		Power supply for RF
VDD12SYN	B4	P	1.2	P		Power supply for VCO, PLL, CP and REGCAP
LFO	B5	IO	1.2	PA		Loop filter

Mnemonic	Ball	Dir[1]	Voltage (V)	Pad Type	Drive (mA)	Function
RBIAS	C1	IO	1.2	PA		Bias resistor
GND	C2	G	1.2	G		Ground
VDD12RF1_BB	C3	P	1.2	P		Power supply for RF, analog baseband
GND	C4	G	1.2	G		Ground
GND	C5	G	1.2	G		Ground
BBIPTP	D1	IO	1.2	PA		Baseband IP test point
BBQPTP	D2	IO	1.2	PA		Baseband QP test point
GND	D3	G	1.2	G		Ground
VDD12FUSE	E1	P	1.2	P		Power supply for fuse
VDD 12DIG	E2	P	1.2	P		Power supply for digital
GND	E3	G	1.2	G		Ground

[1] P = power, G = ground, I = input, O = output, B = bi-direction, D = dual voltage, ZO = tri-state output, AI = analog input, AO = analog output, PU = pull-up, PD = pull-down, S = Schmitt trigger, FS = fail safe IO, OD = open drain, KP = contains busholder, SI = TCXO input, XA = Xtal.

REGISTER MAP OF RF PART

Table 16. Read only Register table

Register Name	Type	MSB	Address						LSB
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RD00	R	CHIPID1<7:0>							
RD01	R	CHIPID0<7:0>							
RD02	R	SPLITID<7:0>							
RD03	R	Blank		Blank		Blank		Blank	Blank
RD04	R	Blank	Blank						
RD05	R	GVBB<7:0>							
RD06	R	GVBBI<7:0>							
RD07	R	GVBBQ<7:0>							
RD08	R	Blank				Blank			
RD09	R	Blank				Blank			
RD0A	R	Blank				Blank			
RD0B	R	IOFSCON<7:0>							
RD0C	R	Blank				Blank			
RD0D	R	QOFSCON<7:0>							
RD0E	R	Blank			Blank				
RD0F	R	Blank			Blank				
RD10	R	Blank				Blank			
RD11	R	Blank				Blank			
RD12	R	Blank			Blank				
RD13	R	Blank			Blank				
RD14	R	READEFUSE<15:8>							
RD15	R	READEFUSE<7:0>							
RD16	R	BBAGCBBD<7:0>							
RD17	R	RFRSSID<7:0>							
RD18	R	ADJRSSID<7:0>							
RD19	R	RFPWRDETD<7:0>							
RD1A	R	BBRSSID<7:0>							
RD1B	R	BBAGCEXTD<7:0>							
RD1C	R	TMPSNSD<7:0>							
RD1D	R	VTUNED<7:0>							
RD1E	R	Reserved							
RD1F	R	Reserved							

NOTES
Reset values can be changeable without notice. Email Mobile_TV_support@analog.com to check the latest values.

Table 17. Read/Write Register table

Register Name	Initial	Type	MSB	Address						LSB
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR20	0×6b	R/W	BAND<1:0>		LPFBW	ADJ<1:0>		TOP<2:0>		
WR21	0×72	R/W	OB_EN	EXT_EN	INT_EN	PDAAC	CLKSEL<2:0>			READEN
WR22	0×20	R/W	DIVSEL<1:0>		ICP<5:0>					

Register Name	Initial	Type	MSB	Address						LSB
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR23	0×b0	R/W	CTUNE_ ON	RTUNE_ ON	AAC_RN	RN_PLL	CAL_ON	PCAL_ ON	AAC_ EN	VCO BIASSW
WR24	0×80	R/W	ICP_OFS<4:0>					ICP_EXT	PC4	DTHEN
WR25	0×40	R/W	BBPWR<1:0>		N<13:8>					
WR26	0×0b	R/W	N<7:0>							
WR27	0×00	R/W	Blank		EXTGVBB<1:0>		F<19:16>			
WR28	0×00	R/W	F<15:8>							
WR29	0×00	R/W	F<7:0>							
WR2A	0×00	R/W	SWPD LNA	SWPD RFPGA	SWPD MIXER	SWPD LPF	SWPD CTUNE	SWPD BBPGA	SWPD OUTBUF	SWPD VCO
WR2B	0×00	R/W	SWPD PLL	SWPD PWDET	SWPD ADJRSSI	SWPD RFRSSI	SWPD BBRSSI	SWPD TMPSNS	SWPD RTUNE	SWPD ADC
WR2C	0×3f	R/W	SWPD LDO	SWPD BGR	TSPD LNA	TSPD RFPGA	TSPD MIXER	TSPD LPF	TSPD CTUNE	TSPD BBPGA
WR2D	0×ff	R/W	TSPD OUTBUF	TSPD VCO	TSPD PLL	TSPD PWDET	TSPD ADJRSSI	TSPD RFRSSI	TSPD BBRSSI	TSPD TMPSNS
WR2E	0×f5	R/W	TSPD RTUNE	TSPD ADC	TSPD LDO	TSPD BGR	Reserved			
WR2F	0×42	R/W	Reserved							
WR30	0×40	R/W	Reserved							
WR31	0×22	R/W	Reserved							
WR32	0×22	R/W	Reserved							
WR33	0×a4	R/W	Reserved							
WR34	0×64	R/W	Reserved							
WR35	0×8b	R/W	Reserved							
WR36	0×40	R/W	Reserved							
WR37	0×3c	R/W	Reserved							
WR38	0×bc	R/W	Reserved							
WR39	0×6f	R/W	Reserved							
WR3A	0×30	R/W	Reserved							
WR3B	0×d8	R/W	Reserved							
WR3C	0×00	R/W	Reserved							
WR3D	0×bb	R/W	Reserved				CONBAND<4:1>			
WR3E	0×7c	R/W	Blank	CONBAND	Reserved					
WR3F	0×10	R/W	Reserved							
WR40	0×f0	R/W	Reserved							
WR41	0×33	R/W	Reserved							
WR42	0×04	R/W	Reserved							
WR43	0×f6	R/W	Reserved							
WR44	0×76	R/W	Reserved							
WR45	0×36	R/W	Reserved							
WR46	0×80	R/W	Reserved							
WR47	0×40	R/W	Reserved							
WR48	0×b0	R/W	Reserved							
WR49	0×40	R/W	Reserved							
WR4A	0×c0	R/W	Reserved							
WR4B	0×93	R/W	Reserved							
WR4C	0×40	R/W	Reserved							

Register Name	Initial	Type	MSB	Address						LSB
			bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WR4D	0×8d	R/W	Reserved							
WR4E	0×72	R/W	Reserved							
WR4F	0×d7	R/W	Reserved							
WR50	0×0a	R/W	Blank	Reserved						
WR51	0×7a	R/W	Blank	Reserved						
WR52	0×12	R/W	Blank	Reserved						
WR53	0×72	R/W	Blank	Reserved						
WR54	0×1a	R/W	Blank	Reserved						
WR55	0×56	R/W	Blank	Reserved						
WR56	0×02	R/W	Blank	Reserved						
WR57	0×3e	R/W	Blank	Reserved						
WR58	0×3c	R/W	Blank	Reserved						
WR59	0×2e	R/W	Blank	Reserved						
WR5A	0×4e	R/W	Blank	Reserved						
WR5B	0×36	R/W	Blank	Reserved						
WR5C	0×32	R/W	Blank	Reserved						
WR5D	0×3e	R/W	Blank	Reserved						
WR5E	0×1a	R/W	Blank	Reserved						
WR5F	0×3e	R/W	Blank	Reserved						
WR60	0×7f	R/W	Blank	Reserved						
WR61	0×00	R/W	Blank	Reserved						
WR62	0×7f	R/W	Blank	Reserved						
WR63	0×8d	R/W	Reserved							
WR64	0×72	R/W	Reserved							
WR65	0×c3	R/W	Reserved							
WR66	0×00	R/W	Reserved							
WR67	0×c3	R/W	Reserved							
WR68	0×d3	R/W	Reserved							
WR69	0×1a	R/W	Reserved							
WR6A	0×2c	R/W	Reserved							
WR6B	0×35	R/W	Reserved							
WR6C	0×00	R/W	Reserved							
WR6D	0×50	R/W	Reserved							
WR6E	0×00	R/W	Reserved							
WR6F	0×90	R/W	Reserved							
WR70	0×00	R/W	Reserved							
WR71	0×3e	R/W	Reserved							
WR72	0×ff	R/W	Reserved							
WR73	0×00	R/W	Reserved							
WR74	0×00	R/W	Reserved							
WR75	0×00	R/W	Reserved							

NOTES
Initial values can be changeable without notice. Email Mobile_TV_support@analog.com to check the latest values.

Table 18. Register description

Address [Bits]	Type	Name	Description	Default Value
		LNA		
0x20[7:6]	R/W	**BAND<1:0>**	LNA Band Selection, (0:FM, 1:BAND3, 2:BAND3, 3:LBAND)	
0x03[1]	R	**BIASSHORT**	Mode Change SW (0: Steady state, 1: mode control moment [for 50usec])	
		LPF DIGITAL BLOCK		
0x20[5]	R/W	**LPFBW<0>**	LPF mode selection, 0 : FM, 1 : T-DMB	
0x08[4:0]	R	**CTUNE<4:0>**	Cap bank tuning value from digital block	
		CTUNE DIGITAL BLOCK		
0x23[7]	R/W	**CTUNE_ON<0>**	Main clock and CTUNE_ON make TUNEEN signals. TUNEEN signal toggles at falling edge of main clock. CTUNE en/disable, 0 : disable, 1 : enable	
0x21[3:1]	R/W	**CLKSEL<2:0>**	CTUNE CLK selection, 1 : 16.384MHz, 2 : 19.2MHz, 4 : 24.576MHz (Do not use)	
0x09[4:0]	R	**CV**	Cap bank value by tuning	
		OCA & BBPGA & OUTBUF		
0x21[7]	R/W	**OB_EN<0>**	OUTBUF output node switch control. 0 : Off, 1 : On	
0x21[6]	R/W	**EXT_EN<0>**	Internal switch control. 0 : Off, 1 : On	
0x21[5]	R/W	**INT_EN<0>**	External switch control. 0 : Off, 1 : On	
		VCO & LOOP FILTER		
0x21[4]	R/W	**PDAAC<0>**	power down of automatic amplitude control circuit. (0: Power on ACC, 1: Power off AAC, Default=0)	
0x23[5]	R/W	**AAC_RN<0>**	Reset of AAC	
0x23[1]	R/W	**AAC_EN<0>**	0 : AAC hold, 1 : AAC Enable	
0x22[7:6]	R/W	**DIVSEL<1:0>**	Band election. "00" : L-band, "01" : Band-III, "11": FM	
0x23[0]	R/W	**VCOBIASSW<0>**	Enable when AAC_EN is "1"	
0x3D[3:0] 0x3E[6]	R/W	**CONBAND<4:1>** **CONBAND<0>**	Load resistor control words <0>: Band_2DIV, <1>: Band_3DIV, <2>: Band_4DIV, <4>: Band_BUF. <3>: Band_DIVIII, : L-band=" 0", Band-III & FM="1"	
0x0E[5:0]	R	**VCORG<5:0>**	Externally supplied words for tank MIM capacitance in the VCO core. write mode : VCORGSPI (VCORGSPI register operate when EXTVCORG is "1".) 000000 : min., 111111:max.	
0x0F[5:0]	R	**VCOCON<5:0>**	AAC bias value	
0x1D[7:0]	R	**VTUNED<7:0>**	ADC output of VTUNE	
		PLLA		
0x22[5:0]	R/W	**ICP<5:0>**	Charge pump current setting value.	
0x23[3]	R/W	**CAL_ON<0>**	0 : Hold, 1 : Charge pump calibration enable.	
0x23[2]	R/W	**PCAL_ON<0>**	0 : Hold, 1 : Charge pump initial calibration enable.	

Address [Bits]	Type	Name	Description	Default Value
0x24[7:3]	R/W	**ICP_OFS<4:0>**	EICP_CALI<4:0> setting offset value. See EICP_CALI<4:0> description.	
0x24[2]	R/W	**ICP_EXT<0>**	Manual EICP_CALI<4:0> setting enable. See EICP_CALI<4:0> description.	
0x23[4]	R/W	**RN_PLL<0>**	PLL reset. 1 : operation, 0 : PLL reset.	
0x10[4:0]	R	**EICP_CALI<4:0>**	Charge pump UP/DN current calibration code. 1) If ICP_EXT = 0 & ICP_OFS<4) = 0 EICP_CALI<4:0> = MICP_CALO<4:0> + ICP_OFS<3:0> 2) If ICP_EXT = 0 & ICP_OFS<4) = 1 EICP_CALI<4:0> = MICP_CALO<4:0> - ICP_OFS<3:0> 3) If ICP_EXT = 1 EICP_CALI<4:0> = ICP_OFS<4:0>	
0x11[4:0]	R	**MICP_CALO<4:0>**	Charge pump UP/DN current calibration result code without offset. See EICP_CALI<4:0> description.	
		PLLD		
0x24[1]	R/W	**PC4<0>**	Pre-scaler divide ratio setting. 0 : 8/9, 1 : 4/5	
0x25[5:0] 0x26[7:0]	R/W	**N<13:8>** **N<7:0>**	PLL feedback divider integer value.	
0x27[3:0] 0x28[7:0] 0x29[7:0]	R/W	**F<19:16>** **F<15:8>** **F<7:0>**	PLL feedback divider fractional value.	
0x24[0]	R/W	**DTHEN<0>**	Sigma-degta modulator dithering control. 0 : Off, 1 : On	
0x03[0]	R	**LOCK<0>**	PLL Lock status indicator. 0 : Un-lock, 1 : Lock	
		ADJRSSI		
0x20[4:3]	R/W	**ADJ<1:0>**	RSSI attenuator gain control,(00~11 : 6dB step, Min=0dB, Max=-18dB,default=01)	
		RFRSSI		
0x20[2:0]	R/W	**TOP<2:0>**	RSSI attenuator gain control,(000~110 : 6dB step, Min=0dB, Max=-36dB,default=011)	
		BBRSSI		
0x25[7:6]	R/W	**BBPWR<1:0>**	RSSI attenuator gain control,(00~11 : 6dB step, Min=0dB, Max=-18dB,default=01)	
		RTUNE		
0x23[6]	R/W	**RTUNE_ON<0>**	Main clock and RTUNE_ON make RTUNE_EN signals. RTUNE_EN signal toggles at falling edge of main clock. CTUNE en/disable, 0 : disable, 1 : enable	
0x12[5:0]	R	**RTUNE<5:0>**	RTUNE value 1) If RTUNE_EXT = 0 & RTUNEOFS<5> = 0 RTUNE<5:0> = RV<5:0> + RTUNEOFS<4:0> 2) If RTUNE_EXT = 0 & RTUNEOFS<5> = 1 RTUNE<5:0> = RV<5:0> - RTUNEOFS<4:0> 3) If RTUNE_EXT = 1 RTUNE<5:0> = RTUNEOFS<5:0>	
0x13[5:0]	R	**RV<5:0>**	Internal RTUNE setting value without offset	
		EFUSE		

Address [Bits]	Type	Name	Description	Default Value
0x21[0]	R/W	**READEN<0>**	After chip reset, READEN should go to high (>10us) and then fall to low to make READEFUSE data valid	
0x14[15:8] 0x15[7:0]	R	**READEFUSE<15:0>**	Read Fuse programming data in READ mode	
		RFAGC DIGITAL BLOCK		
0x17[7:0]	R	**RFRSSID<7:0>**	RFRSSI detection value after ADC	
0x18[7:0]	R	**ADJRSSID<7:0>**	ADJRSSI detection value after ADC	
0x19[7:0]	R	**RFPWRDETD<7:0>**	RF power detector detection value after ADC	
0x03[5:4]	R	**LNAGAIN<1:0>**	LNA gain state value 0 : low gain, 1,2 : mid gain, 3 : high gain	
0x03[3:2]	R	**GVLPF<1:0>**	LPF gain state value 0 : low gain (-2.4 dB), 1 : mid gain (3.3 dB), 2 : high gain (8.7 dB), 3 : DO NOT USE	
0x04[6:0]	R	**RFAGC<6:0>**	RFAGC gain state value. 0x00 : lowest gain, 0x7f : highest gain	
		BBAGC DIGITAL BLOCK		
0x27[5:4]	R/W	**EXTGVBB<1:0>**	GVBB selection. 0 : internal, 1: I2C, 2 : external, 3: from demodulator	
0x1A[7:0]	R	**BBRSSID<7:0>**	BBRSSI detection value after ADC	
0X1B[7:0]	R	**BBAGCEXTD<7:0>**	External AGC voltage value after ADC	
0X16[7:0]	R	**BBAGCBBD<7:0>**	AGC value from demodulator	
0X05[7:0]	R	**GVBB<7:0>**	Baseband gain value (0x00 : minimum gain ~ 0xc3: maximum gain)	
0X06[7:0]	R	**GVBBI<7:0>**	I-path baseband gain value (0x00 : minimum gain ~ 0xc3: maximum gain)	
0X07[7:0]	R	**GVBBQ<7:0>**	Q-path baseband gain value (0x00 : minimum gain ~ 0xc3: maximum gain)	
		DCOC I2C		
0X0A[12:8] 0X0B[7:0]	R	**IOFSCON<12:0>**	I-path DCOC value of OCA	
0X0C[12:8] 0X0D[7:0]	R	**QOFSCON<12:0>**	Q-path DCOC value of OCA	
		SOFTWARE POWER DOWN		
0x2A[7]	R/W	**SWPDLNA<0>**	LNA software power down	
0x2A[6]	R/W	**SWPDRFPGA<0>**	RFPGA software power down	
0x2A[5]	R/W	**SWPDMIXER<0>**	MIXER software power down	
0x2A[4]	R/W	**SWPDLPF<0>**	LPF software power down	
0x2A[3]	R/W	**SWPDCTUNE<0>**	CTUNE software power down	
0x2A[2]	R/W	**SWPDBBPGA<0>**	BBPGA software power down	
0x2A[1]	R/W	**SWPDOUTBUF<0>**	OUTBUF software power down	
0x2A[0]	R/W	**SWPDVCO<0>**	VCO software power down	

Address [Bits]	Type	Name	Description	Default Value
0x2B[7]	R/W	**SWPDPLL<0>**	PLL software power down	
0x2B[6]	R/W	**SWPDPWDET<0>**	PWDET software power down	
0x2B[5]	R/W	**SWPDADJRSSI<0>**	ADJRSSI software power down	
0x2B[4]	R/W	**SWPDRFRSSI<0>**	RFRSSI software power down	
0x2B[3]	R/W	**SWPDBBRSSI<0>**	BBRSSI software power down	
0x2B[2]	R/W	**SWPDTMPSNS<0>**	TMPSNS software power down	
0x2B[1]	R/W	**SWPDRTUNE<0>**	RTUNE software power down	
0x2B[0]	R/W	**SWPDDADC<0>**	ADC software power down	
0x2C[7]	R/W	**SWPDDLDO<0>**	LDO software power down	
0x2C[6]	R/W	**SWPDBGR<0>**	BGR software power down	
TIME-SLICING POWER DOWN				
0x2C[5]	R/W	**TSPDLNA<0>**	LNA time-slicing power down enable	
0x2C[4]	R/W	**TSPDPGA<0>**	RFPGA time-slicing power down enable	
0x2C[3]	R/W	**TSPDMIXER<0>**	MIXER time-slicing power down enable	
0x2C[2]	R/W	**TSPDLPF<0>**	LPF time-slicing power down enable	
0x2C[1]	R/W	**TSPDCTUNE<0>**	CTUNE time-slicing power down enable	
0x2C[0]	R/W	**TSPDBBPGA<0>**	BBPGA time-slicing power down enable	
0x2D[7]	R/W	**TSPDOUTBUF<0>**	OUTBUF time-slicing power down enable	
0x2D[6]	R/W	**TSPDVCO<0>**	VCO time-slicing power down enable	
0x2D[5]	R/W	**TSPDPLL<0>**	PLL time-slicing power down enable	
0x2D[4]	R/W	**TSPDPWDET<0>**	PWDET time-slicing power down enable	
0x2D[3]	R/W	**TSPDADJRSSI<0>**	ADJRSSI time-slicing power down enable	
0x2D[2]	R/W	**TSPDRFRSSI<0>**	RFRSSI time-slicing power down enable	
0x2D[1]	R/W	**TSPDBBRSSI<0>**	BBRSSI time-slicing power down enable	
0x2D[0]	R/W	**TSPDTMPSNS<0>**	TMPSNS time-slicing power down enable	
0x2E[7]	R/W	**TSPDRTUNE<0>**	RTUNE time-slicing power down enable	
0x2E[6]	R/W	**TSPDADC<0>**	ADC time-slicing power down enable	
0x2E[5]	R/W	**TSPDLDO<0>**	LDO time-slicing power down enable	
0x2E[4]	R/W	**TSPDBGR<0>**	BGR time-slicing power down enable	
ETC				
0X1C[7:0]	R	**TMPSNSD<7:0>**	ADC output of temperature sensor	

THEORY OF OPERATION

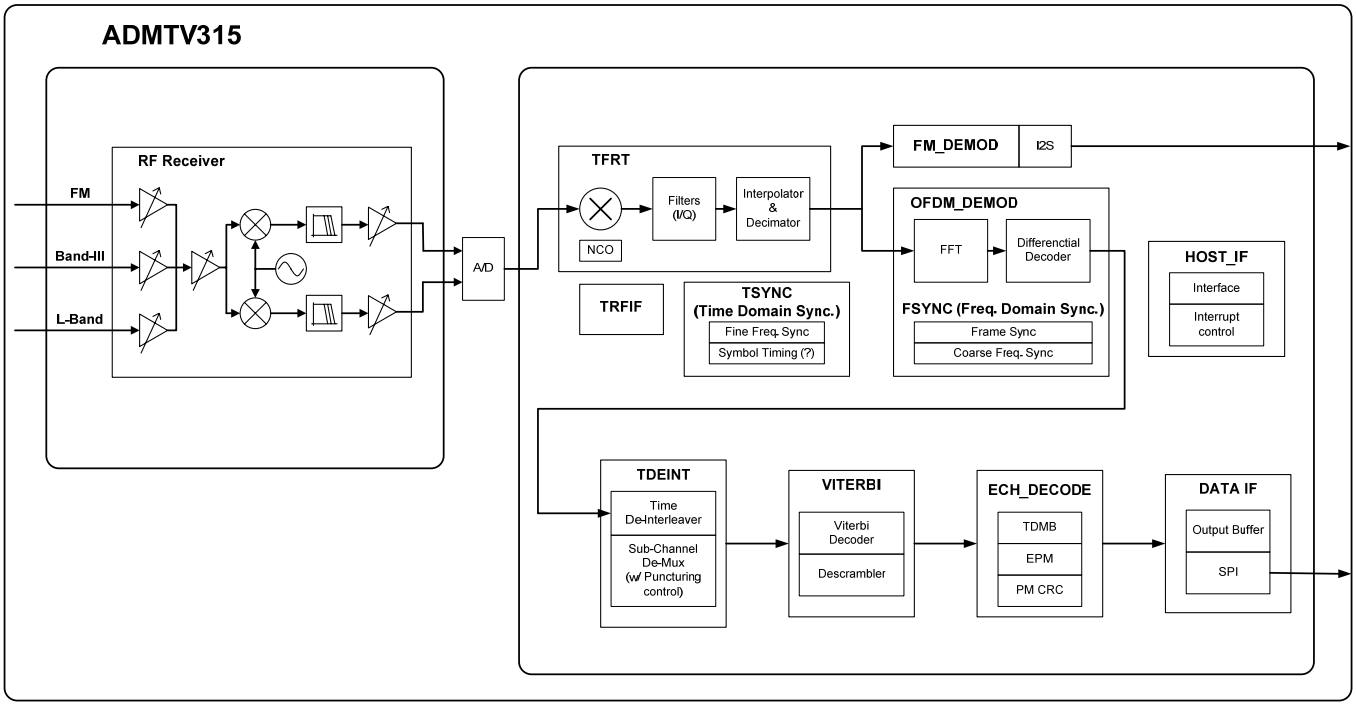


Figure 5. ADMTV315 Interface

[1] P = power, G = ground, I = input, O = output, B = bi-directional, D = dual voltage, ZO = tri-state output, AI = analog input, AO = analog output, PU = pull-up, PD = pull-down, S = Schmitt trigger, FS = fail safe IO, OD = open drain, KP = contains busholder, SI = TCXO input, XA = xtal.

RF LOW NOISE AMPLIFIER (LNA), RF PROGRAMMABLE GAIN AMPLIFIER (PGA) AND DOWN-CONVERTER

RF LNA, PGA and down-converter amplify coming RF signals and down-convert to zero-IF frequency. LNA has 3-gain modes, which are high, mid and low gain with gain step of 20dB. LNA gain state can be read from LNAGAIN register (0: low gain, 1, 2: mid gain, 3: high gain). RFPGA has around 30 dB gain dynamic range. RFPGA controlled by the Digital Gain code, which read from RFAGC<6:0> register. RFPGA gain is from 0×00 (minimum gain) to 0×7f (maximum gain). Gain step is around 0.7 dB. Zero-IF down conversion mixer down-converts signal from RFPGA's output.

LOCAL OSCILLATOR (LO)

ADMTV315 includes an on-chip VCO, which eliminates external LC tank. The VCO uses only 1.2V. The internal VCO covers whole Band-III, L-band and FM, which are 168 ~ 245 MHz, 88 ~ 108MHz and 1450 ~ 1492MHz, respectively. Along with fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of video signals.

PHASE LOCKED LOOP (PLL)

ADMTV315 frequency synthesizer consists of a sigma-delta fractional-N PLL and a VCO.

The synthesizer uses fractional-N type architecture with high performance 20bits sigma-delta modulator to get a high resolution and the fast switching time as well as a good phase noise. The charge pump programmed by 6-bit digital control and its current range is from 20μA to 1280μA. The loop filter voltage and VCO range can adjust Charge pump current. Unlike the integer-N type synthesizer used in other silicon tuners, sigma-delta modulated frequency synthesizer provides: 1. Fast switching time, 2. Ultra high frequency resolution, 3. Good phase noise due to its wide bandwidth. The switching time is less than 30μsec for the worst case of power up sequence. Using 16.384 MHz oscillator, 20-bit sigma-delta modulated fractional-N phase locked loop exhibits very fine frequency resolution of 16Hz. It can compensate the frequency offset induced by error ratio and temperature drift, etc. of the reference crystal. The LO frequency, f_{LO}, is calculated as following equation:

$$PLL\ Frequency = \left(\frac{Clock\ Frequency \times \left(PLLN + \frac{PLLF}{2^{20}} \right)}{PLLR} \right)$$

$$f_{LO} = \left(\frac{PLL\ Frequency}{PLLS} \right)$$

where:
PLLN is the N-counter divide value selected by the PLLN register.
PLLF is the fractional value selected by the PLLF register.
PLLS is the reference divide ratio selected by the DIVSEL.

The DIVSEL register value is due to the VCOSEL register and frequency range.

BASEBAND LOW-PASS FILTER (LPF) AND VARIABLE GAIN AMPLIFIER (VGA)

The baseband (BB) block contains LPF and PGA. The RF signal goes down to zero-IF through RF zero-IF down-converter. The baseband LPF selects the wanted signal in the output of down-converter. The cut-off frequency of LPF is about 768kHz for T-DMB and 225kHz for FM. To compensate the variation of cutoff frequency in the LPF, the automatic cutoff-tuning circuit is included and this circuit guarantees the cut-off frequency accuracy.

The baseband AGC controls the input level of ADC in demodulator. Gain of baseband PGA is controlled by 8-bit gain control register. The PGA gain setting can be read from GVBB register. The GVBB<7:0> ranges from 0×00 to 0×c3. Digital gain step is around 0.25 dB. Baseband PGA gain setting can be programmable by I2C GVBBI2C<7:0> register for ADMTV315 test mode. There are three modes for baseband gain setting according to EXTGVBB<1:0> register setting as:

- RF internal AGC using analog baseband RSSI
- Manual gain setting using GVBBI2C
- Gain setting from demodulator's AGC digital code.

AUTOMATIC GAIN CONTROL (AGC)

In ADMTV315, there are 2 AGC loops, which are RFAGC and BBAGC. LNA has 3-step gain control, and gain difference is 18 dB. RFPGA has around 30 dB gain dynamic range, and controlled by RFAGC<6:0> register. The register value is from 0×00 (minimum gain) to 0×7f (maximum gain). GVLPF has gain 11dB. RFAGC consists of these 3 blocks. RFAGC dynamic range is around 77 dB.

BBAGC has programmable gain amplifier with gain step of 0.25 dB. The BB gain is determined by digital gain setting of GVBB<7:0> register. The register value is from 0×00 (minimum gain) to 0×c3 (maximum gain). BBAGC dynamic range is around 48dB. With these two dynamic ranges (RF 70dB, IF 48dB), dynamic range of ADMTV315 is larger than 100 dB.

Recommended output amplitude of ADMTV315 is from 300mVpp to 700mVpp at each OUT and OUTB pin.

POWER-DOWN CONTROL

ADMTV315 has three power-down modes: hardware power-down (CHIPSEL), time-slicing power-down (TSPD pin), and software power-down (SWPD register settings).

Recovery time from power-down depends on the PLL lock time and the demodulator's AGC response.

- If the CHIPSEL pin is Low, all block is power-down state including the crystal oscillator.
- If the TSPDxxx block register (refer to table 17) set '1', the xxxBlock turn to power-down.
- If the SWPDxxx block register (refer to table 17) set '1', the xxxBlock turn to power-down.

In case of a hardware power-down and time-slicing power-down, all blocks including the crystal oscillator block are power down. Therefore, all digital parameters are stored as they were before power-down.

After being power-on by the CHIPSEL pin, the tuner does not need to operate the VCO searching loop and automatic gain control. Therefore, the power-on delay time is about 250 μs. However, after a SWPD power-on, the tuner needs to operate the VCO searching loop and automatic gain control because the digital block is active during the SWPD. Therefore, the software power-on delay time of about 12 ms is relatively longer than the power-on delay times of the time-slicing power-down and hardware power-down.

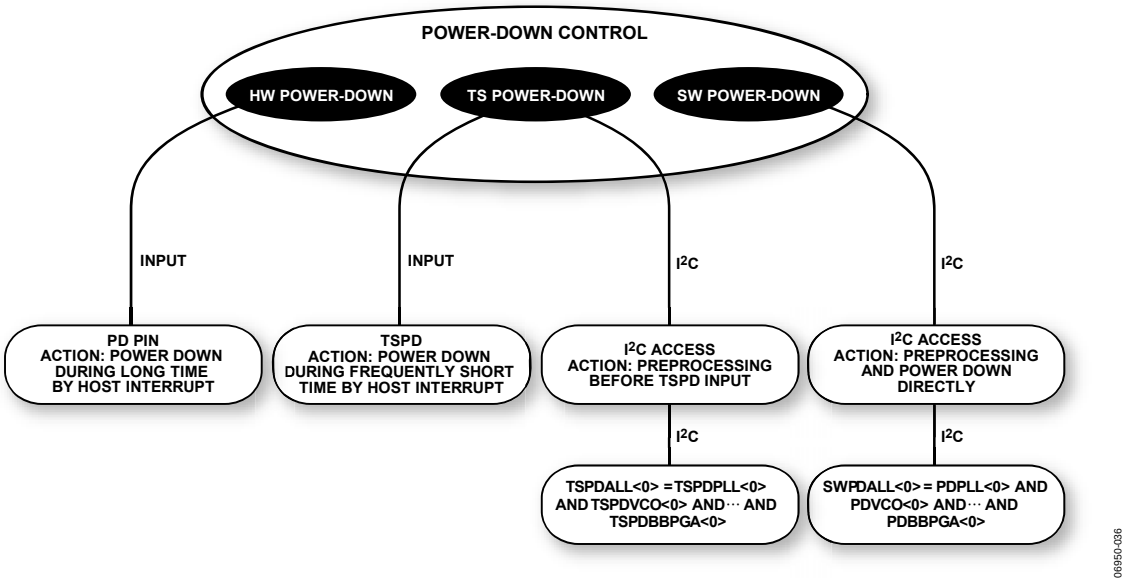


Figure 6. Three Power- Down Modes

SYSTEM INTERFACE

DATA INTERFACE

[Base Address: ADMTV315 Base + 0×180]

DATA_IF is an interface for sending the data decoded in modem to AP (Application Processor). It supports parallel interface and serial interface modes. One of these two modes must be chosen according to AP type and interface implementation method. The main features for each interface are as follows.

- Parallel Interface
  - Host memory interface with interrupt function.
  - FIC, CIF channel buffer with each individual interrupt
- Serial interface
  - Master/Slave mode SPI
    Motorola SPI-compatible interface
    Texas Instruments synchronous serial interface
  - Support SPI re-transmission function for PiP mode.
  - Transmission speed
    Master Mode: Baud rate = 49.152 Mbps ÷ 2 × (1+SCR)
    Slave Mode: Baud rate up to 24Mbps
  - 188/192 byte packet size selectable
  - Flow control using demand signal in Master mode

Data Format

In case of serial data, data is distinguished from the header in one packet (188 byte).

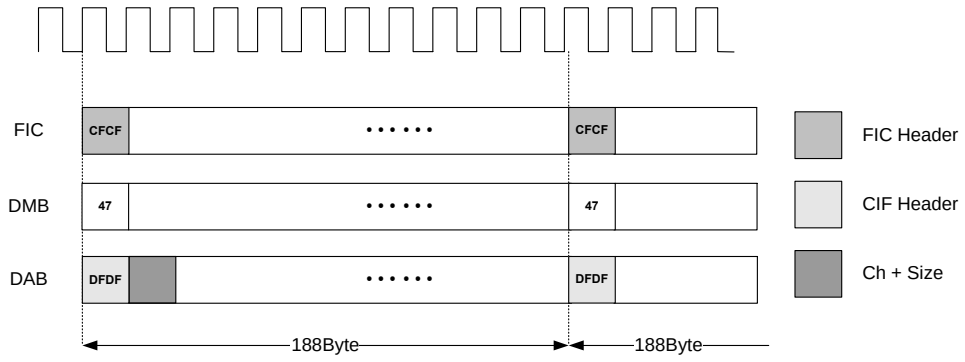


Figure 7. Serial Data Format

Data format in Parallel / Serial Interface is shown in figure 8.

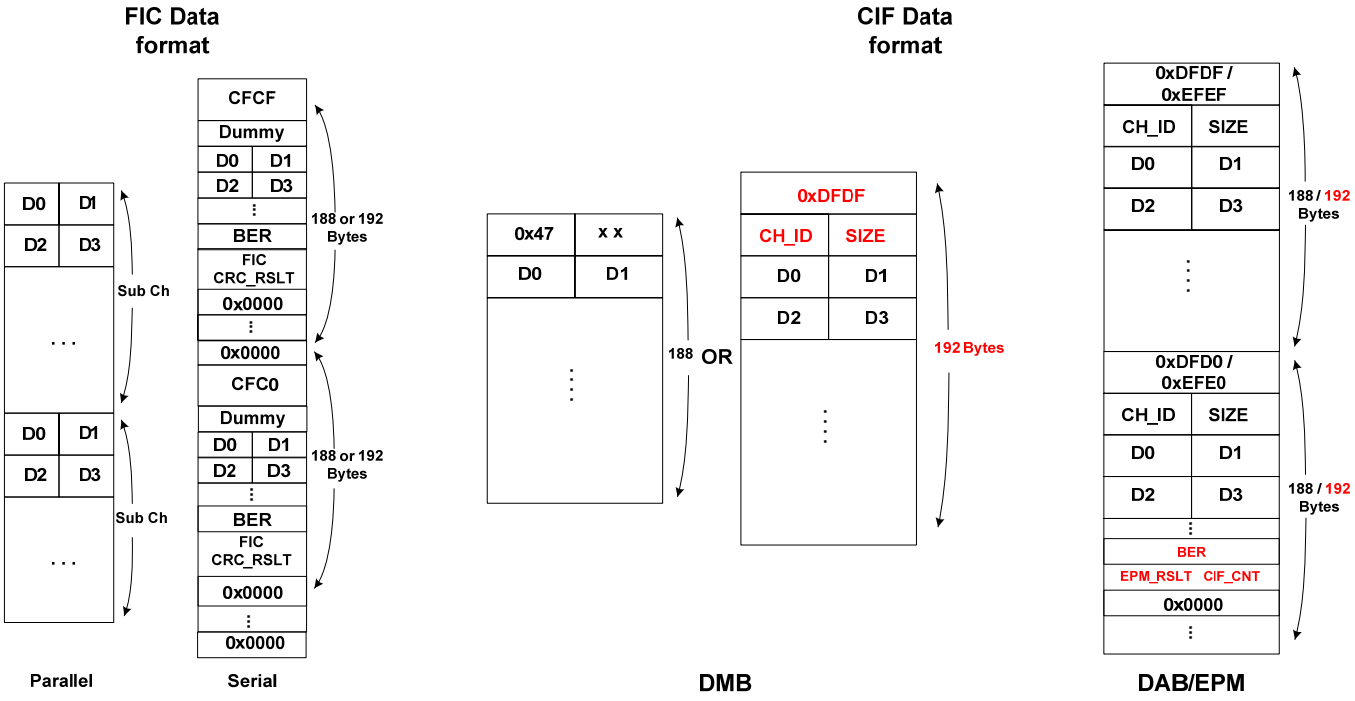


Figure 8. Serial /Parallel Interface Data Buffer Formatting

1. CIF data in Parallel interface

DF'DF'08'3C'FF'FC'94'44'
34'75'66'44'43'44'31'21'11'12'49'24'00'00'00'A8'
BA'1C'C7'80'00'00'10'03'0C'41'04'CF'45'54'96'55'
85'D5'61'57'DA'7D'A6'D9'5D'85'D8'76'07'5F'71'C6'
DD'81'D7'E0'79'F7'9F'72'07'DC'8E'58'24'96'19'63'
7E'58'A0'AA'79'2A'9E'49'A7'8E'78'E8'9A'2A'67'8A'
BA'67'AE'89'F5'51'41'9A'61'A7'3E'07'B2'A3'15'44'
B1'B4'91'00'E0'99'AE'6C'5E'65'9D'45'72'7B'34'55'
79'1B'B6'43'8B'9A'29'23'44'20'E5'58'13'C5'5A'0D'
33'B1'62'36'E2'68'77'11'3B'5D'91'37'3D'ED'8C'2C'
33'6D'A8'76'A0'5C'C6'DD'B4'D4'94'A4'5A'A4'AD'C5'
3A'EF'85'99'44'E5'C1'AE'D2'36'88'1A'06'51'4D'08'
60'2A'1C'0F'BC'3E'99'9A'49'1F'84'37'1D'05'33'B4'
CC'D9'C8'74'7E'CD'6B'5B'52'59'AD'D9'21'26'98'4A'
1C'CA'2D'EB'E2'65'AB'09'22'EC'A4'D5'62'3C'69'1D'
5C'D6'E5'F3'2E'6F'96'74'4C'6D'06'ED'74'B2'DE'47'
92'63'99'5F'24'D5'56'8C'0C'5B'76'A8'1D'3D'4E'F9'
92'3D'22'B3'59'87'2D'37'38'B1'C4'A6'6B'06'36'36'
B5'D4'60'74'46'E7'22'F6'CD'4A'BB'34'87'E9'C0'FE'
68'B2'5A'66'2F'B4'1A'D6'05'45'66'9E'F3'25'56'A9'

40'3E'A0'9B'D8'EE'B4'7D'2C'9C'25'CB'10'96'69'17'
76'13'09'97'36'50'37'BB'57'55'35'57'32'59'38'A9'
1E'B1'A8'26'B6'B9'AD'23'9A'93'9D'A0'1E'EB'0F'88'
B6'89'76'26'CE'78'80'A1'4C'86'5B'85'9C'1A'9E'35'
93'80'00'1C'BB'93'E1'2E'93'D1'7C'50'B7'2C'12'EB'
80'78'A2'2A'7E'8F'11'64'1C'96'BC'72'E4'7D'8A'88'
32'DF'56'0D'C3'ED'2D'8B'BE'A3'CD'5A'21'BE'15'9D'
B3'8A'63'47'32'06'80'E4'8C'14'20'24'50'B7'24'9F'
B6'1A'54'5A'BC'59'D9'6F'AD'8F'C4'8E'B2'64'F0'4A'
03'74'43'2B'11'6A'5E'12'F6'D6'77'56'6A'CB'15'C9'
C1'81'93'00'ED'ED'89'E6'24'B7'21'02'

DF'DF' : CIF identifier

08'3C' : CH_ID + Size[CU] -> MSB 6 bit is a Sub-channel ID and others 10 bit is a data size

0x08 0x3C = 00001000 00111100

Therefore, 000010 (0x02) is a sub-channel ID, 00 00111100(0x3C) is a data size

0x3C[CU] = 0x3C X 8 [byte] = 480 [byte].

The CIF data size is 480[byte] excluding 0xDF, 0xDF, 0x08 and 0x3C.

According to the set MSL of DATA_IF Control Register to MSB_FIRST or LSB_FIRST, byte order is different which read from AP in case of Parallel interface. (Refer to cmc521Endian's function of the API document)

2. TS data in Parallel interface

DF'DF'04'CC'47'41'00'19'00'02'B0'97'00'01'FD'00'
00'E1'14'F0'66'1D'64'11'01'02'60'00'4F'01'0C'23'
41'04'03'2F'00'02'23'00'04'04'16'02'0D'00'00'FF'
00'00'08'00'00'00'08'00'05'07'30'A0'70'14'00'0F'
0F'06'10'00'C6'00'01'5F'90'00'00'00'00'21'00'00'
00'00'03'03'26'00'01'24'00'04'04'0D'02'05'00'00'
FF'00'00'08'00'00'00'08'00'06'10'00'C6'00'01'5F'
90'00'00'00'00'21'00'00'00'00'03'13'E1'11'F0'04'
1E'02'00'02'13'E1'12'F0'04'1E'02'00'01'12'E1'13'
F0'04'1E'02'00'03'12'E1'14'F0'04'1E'02'00'04'5E'
0D'3E'2B'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
DF'DF'04'CC'47'41'11'19'00'04'B0'29'00'00'FD'00'
00'C0'C0'92'00'00'00'A4'DE'DE'E8'8E'E4'DE'EA'E0'
00'13'00'12'E2'09'10'A0'8A'01'79'81'30'2A'01'FF'
00'B3'AF'54'16'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'

DF'DF' : CIF identifier
08'3C' : CH_ID[7:2] + Size[CU]
TS(Video data) is also CIF data, so identifier is 0xDF 0xDF.
CH_ID value is valid, but the size value is not.
MPEG TS data size is 188 byte and Header size is 4 byte, so total data length is 192 byte (4 byte + 188 byte)

3. FIC data in Parallel interface

'05'00'E0'41'24'34'FF'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'01'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'11'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'31'
0D'01'13'48'88'18'04'00'89'74'09'74'89'74'0F'22'
F1'E0'04'15'01'C0'12'F1'E0'04'11'01'58'06'00'71'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'F1'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'01'F1'
60'08'22'F1'E0'
04'12'01'58'0A'06'03'00'40'3C'10'01'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'03'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'07'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'0F'F1'
FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'1F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'3F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'7F'F1'

'FIC buffer full interrupt' occurs per 384 byte as FIC data.
To know FIC CRC value read from FIC_CRC_REG register whenever interrupt occurs.

4.. CIF data in Serial interface

DF'DF'08'3C'FF'FC'94'44'
34'75'66'44'43'44'31'21'11'12'49'24'00'00'00'A8'
BA'1C'C7'80'00'00'10'03'0C'41'04'CF'45'54'96'55'
85'D5'61'57'DA'7D'A6'D9'5D'85'D8'76'07'5F'71'C6'
DD'81'D7'E0'79'F7'9F'72'07'DC'8E'58'24'96'19'63'
7E'58'A0'AA'79'2A'9E'49'A7'8E'78'E8'9A'2A'67'8A'
BA'67'AE'89'F5'51'41'9A'61'A7'3E'07'B2'A3'15'44'
B1'B4'91'00'E0'99'AE'6C'5E'65'9D'45'72'7B'34'55'
79'1B'B6'43'8B'9A'29'23'44'20'E5'58'13'C5'5A'0D'
33'B1'62'36'E2'68'77'11'3B'5D'91'37'3D'ED'8C'2C'
33'6D'A8'76'A0'5C'C6'DD'B4'D4'94'A4'5A'A4'AD'C5'
3A'EF'85'99'44'E5'C1'AE'D2'36'88'1A'06'51'4D'08'
60'2A'1C'0F'
DF'D0'08'3C'BC'3E'99'9A'49'1F'84'37'1D'05'33'B4'
CC'D9'C8'74'7E'CD'6B'5B'52'59'AD'D9'21'26'98'4A'
1C'CA'2D'EB'E2'65'AB'09'22'EC'A4'D5'62'3C'69'1D'
5C'D6'E5'F3'2E'6F'96'74'4C'6D'06'ED'74'B2'DE'47'
92'63'99'5F'24'D5'56'8C'0C'5B'76'A8'1D'3D'4E'F9'
92'3D'22'B3'59'87'2D'37'38'B1'C4'A6'6B'06'36'36'
B5'D4'60'74'46'E7'22'F6'CD'4A'BB'34'87'E9'C0'FE'
68'B2'5A'66'2F'B4'1A'D6'05'45'66'9E'F3'25'56'A9'
40'3E'A0'9B'D8'EE'B4'7D'2C'9C'25'CB'10'96'69'17'
76'13'09'97'36'50'37'BB'57'55'35'57'32'59'38'A9'
1E'B1'A8'26'B6'B9'AD'23'9A'93'9D'A0'1E'EB'0F'88'
B6'89'76'26'CE'78'80'A1'4C'86'5B'85'
DF'D0'08'3C'9C'1A'9E'35'
93'80'00'1C'BB'93'E1'2E'93'D1'7C'50'B7'2C'12'EB'
80'78'A2'2A'7E'8F'11'64'1C'96'BC'72'E4'7D'8A'88'
32'DF'56'0D'C3'ED'2D'8B'BE'A3'CD'5A'21'BE'15'9D'
B3'8A'63'47'32'06'80'E4'8C'14'20'24'50'B7'24'9F'
B6'1A'54'5A'BC'59'D9'6F'AD'8F'C4'8E'B2'64'F0'4A'
03'74'43'2B'11'6A'5E'12'F6'D6'77'56'6A'CB'15'C9'
C1'81'93'00'ED'ED'89'E6'24'B7'21'02'*00'f3'0f'c8'* -> (0x00<<8|0xf3):BER (0x0F<<8|0xc8):EPM_RSLT CIF_CNT (last 4 byte)
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00' -> The rest is filled with Zero.
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

```
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'
```

All data is transferred by per188byte in case of Serial Interface. Except Video channel, CIF identifier of the first 188 byte in all CIF data is 0xDF 0xDF, and after that CIF identifier is 0xDF, 0xD0 until get to 0xDF 0xDF.

5. TS(Video)data in Serial interface

```
47'41'00'19'00'02'B0'97'00'01'FD'00'
00'E1'14'F0'66'1D'64'11'01'02'60'00'4F'01'0C'23'
41'04'03'2F'00'02'23'00'04'04'16'02'0D'00'00'FF'
00'00'08'00'00'00'08'00'05'07'30'A0'70'14'00'0F'
0F'06'10'00'C6'00'01'5F'90'00'00'00'00'21'00'00'
00'00'03'03'26'00'01'24'00'04'04'0D'02'05'00'00'
FF'00'00'08'00'00'00'08'00'06'10'00'C6'00'01'5F'
90'00'00'00'00'21'00'00'00'00'03'13'E1'11'F0'04'
1E'02'00'02'13'E1'12'F0'04'1E'02'00'01'12'E1'13'
F0'04'1E'02'00'03'12'E1'14'F0'04'1E'02'00'04'5E'
0D'3E'2B'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
47'41'11'19'00'04'B0'29'00'00'FD'00'
00'C0'C0'92'00'00'00'A4'DE'DE'E8'8E'E4'DE'EA'E0'
00'13'00'12'E2'09'10'A0'8A'01'79'81'30'2A'01'FF'
00'B3'AF'54'16'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
```

Transfer as a MPEG2 packet type.

6. FIC data in Serial interface

CF'CF'00'60'05'00'E0'41'24'34'FF'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'01'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'11'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'31'00'64'0F'FF'00'00'00'00'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC or (0x00<<8|0x07):LBAND CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'
CF'CF'04'60'
0D'01'13'48'88'18'04'00'89'74'09'74'89'74'0F'22'
F1'E0'04'15'01'C0'12'F1'E0'04'11'01'58'06'00'71'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'F1'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'01'F1'
00'5D'0F'FF'00'00'00'00'00'00'00'00'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC or (0x00<<8|0x07):LBAND CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'
CF'CF'08'60'08'22'F1'E0'
04'12'01'58'0A'06'03'00'40'3C'10'01'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'03'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'07'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'0F'F1'00'73'0F'FF' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC or (0x00<<8|0x07):LBAND CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'
CF'CF'0C'60'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'1F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'3F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'7F'F1'00'9E'0F'FF'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC or (0x00<<8|0x07):LBAND CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

CF'CF' : FIC data Identifier
0C'60' : continuous count + data length
Continuous count of FIC data increase in order 0x00, 0x04, 0x08 and 0x0C.
The 0x60 indicates a length of FIC data (96byte). FIC data is transferred by per 188byte include a part of FIB data.

Two FIC parsing method
(1)Available parsing per 96 byte whenever receiving FIC data.,
(2)Available execute parsing 384byte at one time after received in order 0x00, 0x04, 0x08 and 0x0C(continuous count).

TAIL_ON of DIF_CTL register set to '1' then FIC stream data(188byte) include BER and CRC. BER is combination of 101st , 102nd data, and CRC values is combination of 103rd , 104th data.
If CRC value is 0xFFF, it means FIC stream data is valid in Band III.(CRC value is 0x0007 in L Band)
When TAIL_ON of DIF_CTL register set to '1', do not calculate CRC check in FIB parsing because CRC value change in to CRC result value by ADMTV315.
IF you want to calculate the value of the software, have to TAIL_ON of DIF_CTL register reset to '0'.

SPI (Serial Peripheral Interface)

1. Motorola SPI

Motorola SPI is designed to control clock polarity and clock phase, define MSB byte and transfer sequence. Figure 9 and 10 show individual waveform. Each setting mode can be controlled with register.

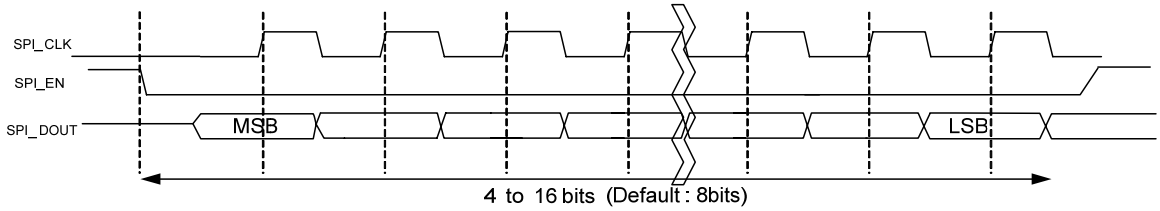


Figure 9. SPH=0 Waveform

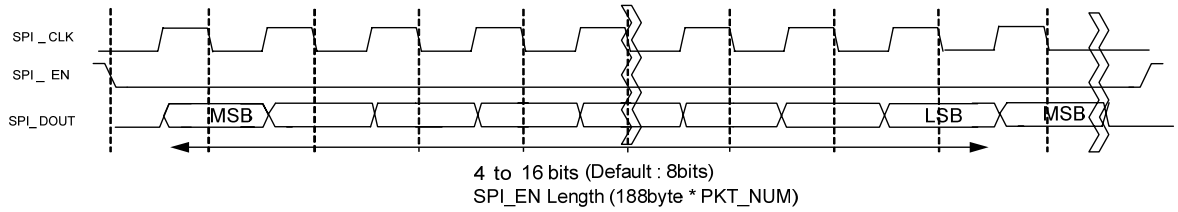


Figure 10. SPH=1 Waveform

2. Texas Instruments SSF

Texas Instruments SSF (Synchronous Serial Frame) supports large part of TI AP format. It uses the same signaling for clock polarity, clock phase and MSB/LSB first control as those of Motorola SPI, but different signaling for EN.

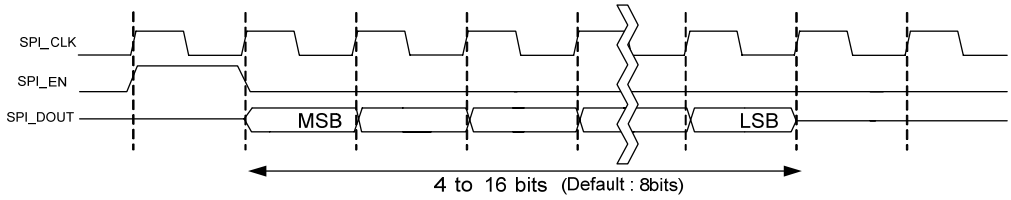


Figure 11. Single Transfer

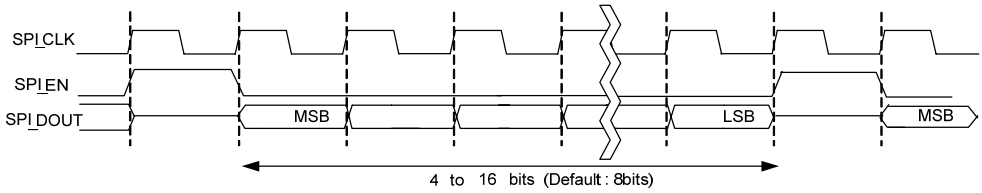


Figure 12. Continuous Transfer

3. Configuration SPI Mode

(1) Demand Mode

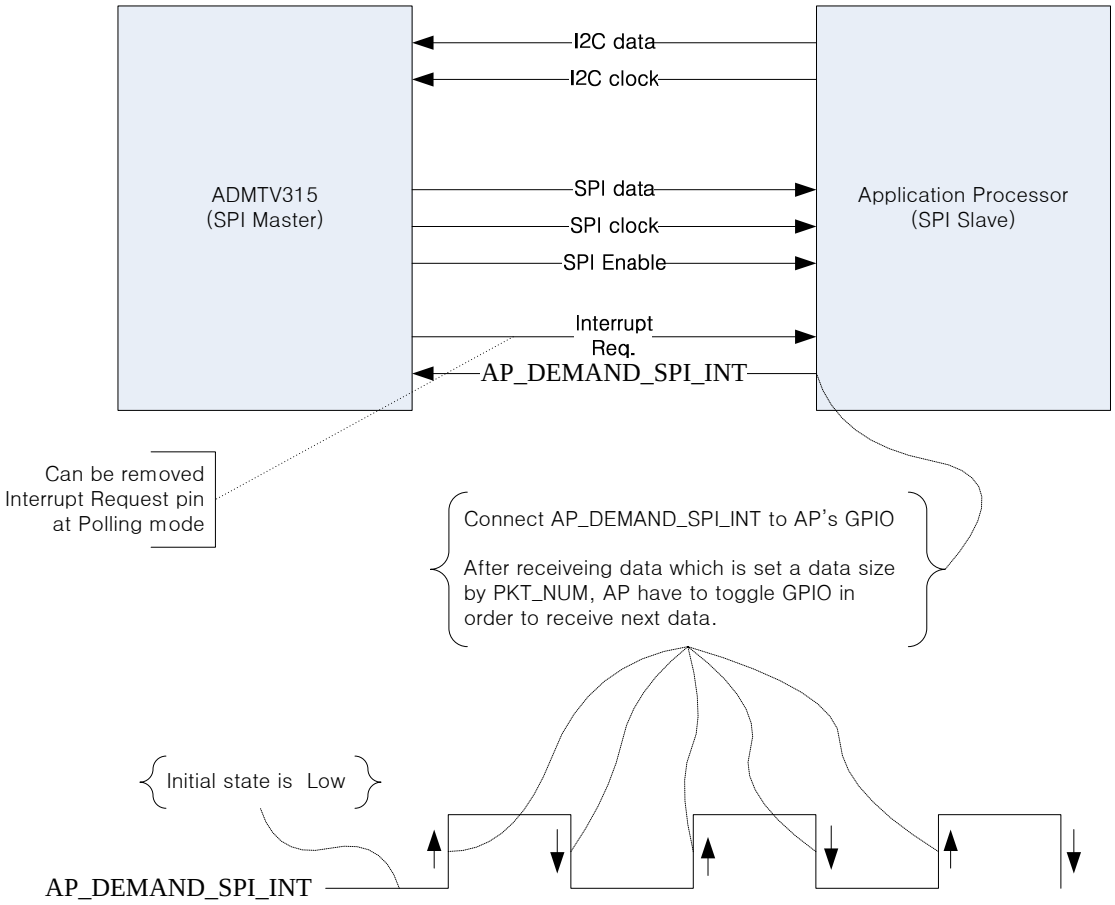


Figure 13. SPI_Demand mode

AP operates as a SPI slave at SPI Demand mode.

Whenever AP delivers AP's status to ADMTV315 through AP_DEMAND_SPI_INT toggle, then ADMTV315 transmit data. Refer to Figure 13. AP will be assign GPIO pin in order to AP_DEMAND_SPI_INT and its pin set to initial Low.

Need to set Register for Demand mode.

A. Set DEMADN_MODE to '1'
B. Set REG_DEMADN_ON to '0' (Set REG_DEMADN_ON to '1' in PIP mode)
C. GPIO pin of AP, which connected AP_DEMADN_SPI_INT, set 'L' from initial state.

(2) Slave Mode

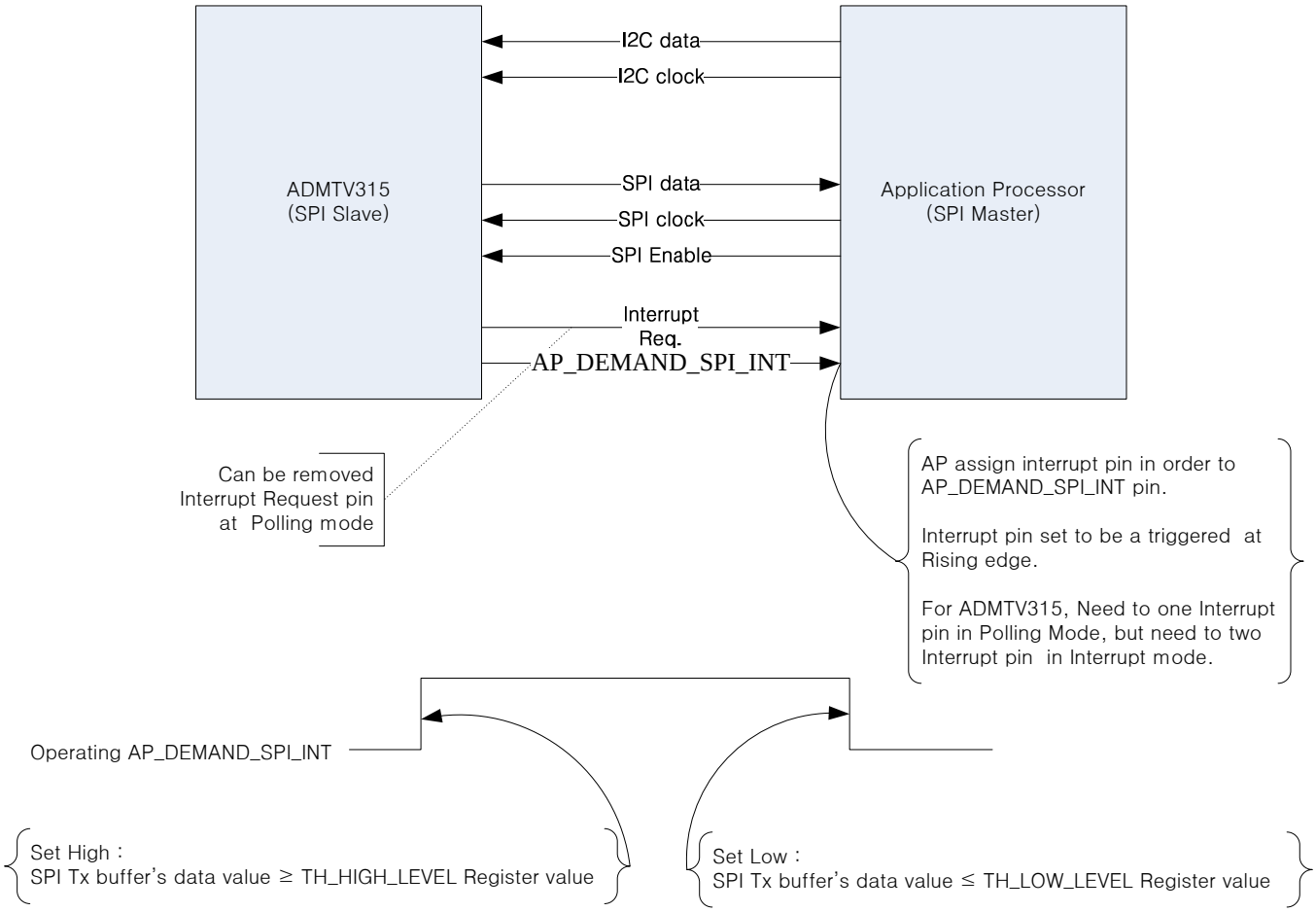


Figure 14. SPI_Slave mode

AP_DEMAND_SPI_INT change to high when Tx buffer's data value becomes above TH_HIGH_LEVEL Register value, and change to low when Tx buffer's data value becomes below TH_LOW_LEVEL Register value. After receiving data as same as TH_HIGH_LEVEL register values, then AP stops SPI Clock signal to ADMTV315.

AP_DEMAND_SPI_INT connect to AP's External Interrupt pin, and Interrupt pin set to be a triggered at rising edge.

PKT_NUM register is set to '0' in Slave Mode. It doesn't support PIP(Pitcher In Pitcher) in Slave mode.

(3) Master Mode

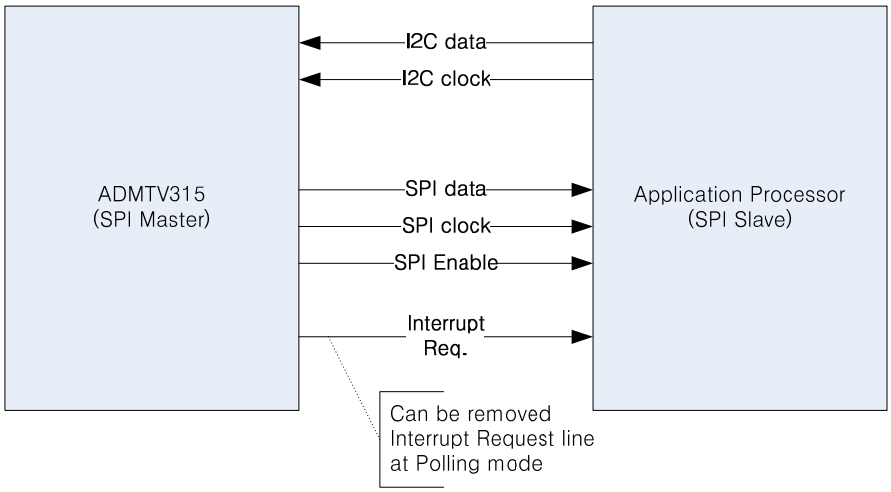


Figure 15. SPI_Master mode

SPI data transmit repeatedly as same as PKT_NUM register values, and has interval as same as PCK_INTV register value.

PCK_INTV register setting need to have a time for received data processing time in AP.

PiP (Picture in Picture)

When ADMTV315 send to AP TS stream of more than 2 pieces of ADMTV315 in PiP mode, then it can be controlled operating to use just one channel by time dividing method. Each demodulator is identified from header which has pre-defined information by S/W setting in early state.

Operation sequence of PiP

In order to operate demodulator without data loss, the following sequence is mandatory.

1. PiP master On(PiP master setting sequence when operated in PiP mode)
   (1) DATA_IF_CR – Serial mode selection
   (2) SIF_CR – PiP master, Reg_demand, PiP_mode, Demand_mode, Half_mode, SPI_on
   (3) REG_DEMAND – ON
   (4) SPI_CR
   (5) SPI_PAD_CTRL – SPI_PAD_CTRL_EN, SPI_PAD_OEn (1'b0)
   (6) SIF_ON
2. PiP slave On (SPI operating sequence when operated in PiP Slave mode)
   (1) DATA_IF_CR
   (2) SIF_CR - PiP slave, PiP_mode, Demand_mode, Half_mode, SPI_on
   (3) PIP_STATE Read - update check
   (4) SPI_CR
   (5) SPI_PAD_CTRL
   (6) SIF_ON
3. PiP slave Off (A slave off sequence for operating one channel in PiP mode)

(1) SIF_OFF

(2) SIF_CR – PiP OFF

(3) PIP_STATE Read – update check

(4) DATA_IF_CR – Serial mode off

(5) SW_RESET

Power-down Sequence in PIP mode

1. PiP OFF
2. Check PIP OFF register update
3. SW_ RESET
4. Power_ OFF

NOTES: Channel off in PIP mode without power down can be executed regardless of operating sequence and manual control.

Parallel I/F

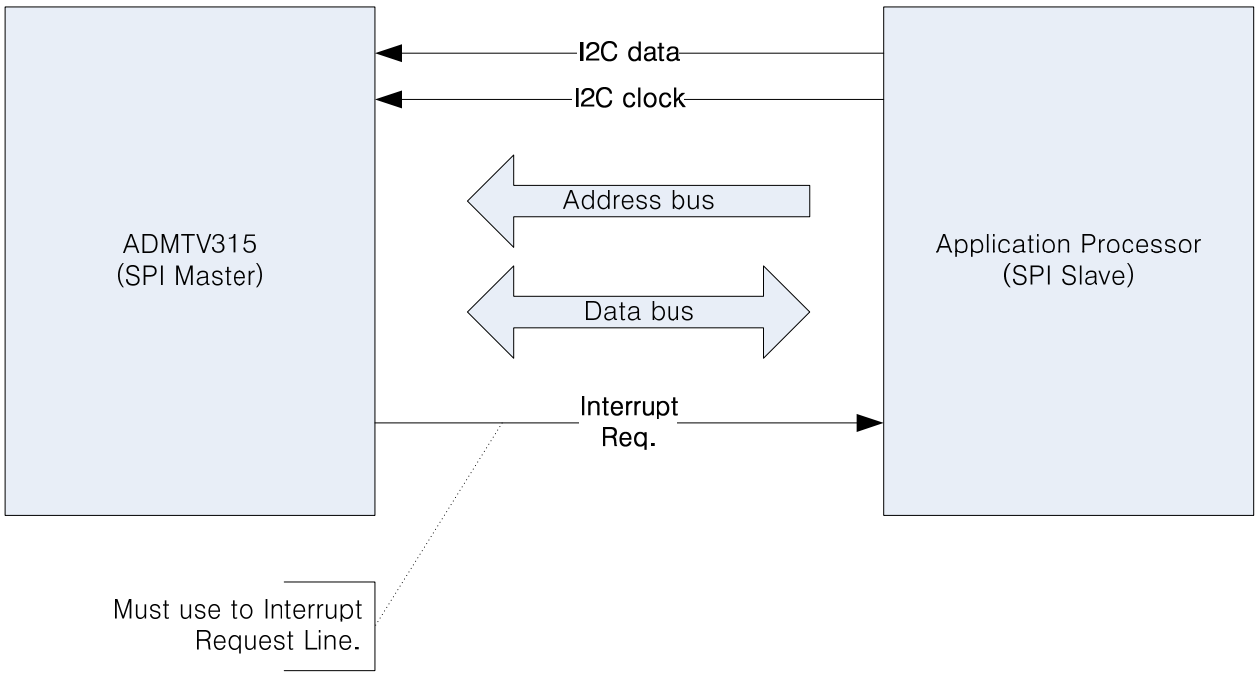


Figure 16. Parallel I/F

In case of Parallel Interface, it uses I2C to access to register Read/Write of RF block.

When CIF/FIC buffer is full with CIF/FIC data, CIF/FIC interrupt occurs via interrupt line and then AP reads data from FIC_MEM_READ and CIF_MEM_READ register as same as size set in CIF_TOTAL_CNT and FIC_TOTAL_CNT register

There are three method of CIF Buffer Interrupt : 'CIF buffer full interrupt' has occurred by DIF_INT_SRC_SEL bit of the DATA_IF Control register.

1. The buffer data of ADMTV315 has become above value of TH_HIGH_LEVEL register.
2. Gather one data packet of Sub-channel.
3. Use to both of 1,2 ways.

Register Description of Base-Band Part [Base address : ADMTV315 Base + 0x180]

Address [6:0]	Type	Name	Description	Default Value
			SW_RESET Register	
0x00 [0]	W	**SW_RESET**	OUT_BUF / SIF Block Software Reset	-
			DATA_IF Control Register	
0x02 [11]	R/W	**FIC/CIF_OFF_SYNC_UPDATE**	Updated FIC/CIF OFF by iCH_CHG 0 : Real time update register 1 : use Syncupdate	0x0
0x02 [10]	R/W	**SERL_PARL_SEL**	OUT_BUF / SIF block Clock Enable Signal. 0 : OUT_BUF Operating Clock Enable 1 : SIF Block Clock Enable	0x0
0x02 [9:8]	R/W	**INT_SRC_SEL**	Interrupt Source Select 0 : 'Ch change' has became a 'Int src' by TDEINT. 1 : When it was a above data of High Threshold level, 'Sub Channel End' has became a 'Int src'. 2 : Use to all interrupt source	0x0
0x02 [7]	R/W	**TAIL_ON**	TAIL information 0 : Output only data information 1 : Output BER, CRC, CIF Counter etc…	0x0
0x02 [6]	R/W	**FM_DMB_SEL**	Input Source select 0 : Input select through DMB_DEC 1 : Input select through FM_DEMOD	0x0
0x02 [5]	R/W	**MLS16**	Switch MSB 16bit and LSB 16bit 0 : MSB(16bit) First, LSB(16bit) Last 1 : LSB First, MSB Last	0x0
0x02 [4]	R/W	**MLS**	Switch MSB 8bit and LSB 8bit 0 : MSB(8bit) First, LSB(8bit) Last 1 : LSB First, MSB Last	0x0
0x02 [3:2]	R/W	**FIC MODE**	FIC Size Setting 00 : 384 byte 01 : 96 byte 10 : 128 byte 11 : 192 byte	0x00
0x02 [1]	R/W	**FIC_OFF**	NOT Transfer FIC Data 0 : Transfer FIC Data 1 : Not transfer FIC Data	0x1
0x02 [0]	R/W	**CIF_OFF**	NOT Transfer CIF Data 0 : Transfer CIF Data 1 : Not transfer CIF Data	0x0
			DATA_HEADER	
0x04[15:0]	R/W	**FIC_HEADER**	DATA_IF FIC Header Register	0xCFCF
0x06[15:0]	R/W	**DMB_HEADER**	DATA_IF DMB Header Register	0xDFDF
0x08[15:0]	R/W	**DAB_HEADER**	DATA_IF DAB Header Register	0xDFDF
0x0A[15:0]	R/W	**EPM_HEADER**	DATA_IF EPM Header Register	0xEFEF
			THRESHOLD LEVEL	
0x0C [15:0]	R/W	**TH_HIGH_LEVEL**	Serial I/F : High Threshold level of the SPI INT signal	0x758

			Parallel I/F : above Level, Occurs Interrupt by Sub Channel end Signal	
0x0E [15:0]	R/W	**TH_LOW_LEVEL**	Low Threshold level of the SPI INT signal	0x3AC
			PIF DATA READ	
0x10 [15:0]	R	**FIC_MEM_READ**	Read to FIC Data from DATA_IF_RAM0	0x0000
0x12 [15:0]	R	**CIF_MEM_READ**	Ready to CIF data from DATA_IF_RAM1	0x0000
			DATA Counter Register	
0x14 [12:0]	R	**CIF_TOTAL_CNT**	Total Data Packet from CIF Buffer(per 2byte) 16bit access read CIF_TOTAL_CNT	0x0000
0x16 [12:0]	R	**CIF_DMB0_CNT**	Total DMB0 Data Packet from CIF Buffer	0x0000
0x18 [12:0]	R	**CIF_DMB1_CNT**	Total DMB1 Data Packet from CIF Buffer	0x0000
0x1A [12:0]	R	**CIF_DMB2_CNT**	Total DMB2 Data Packet from CIF Buffer	0x0000
0x1C [12:0]	R	**CIF_DMB3_CNT**	Total DMB3 Data Packet from CIF Buffer	0x0000
0x1E [12:0]	R	**FIC_TOTAL_CNT**	Total FIC Data from FIC Buffer (per byte) 16bit access read FIC_TOTAL_CNT/2	0x0000
			SIF_ON Register	
0x20 [0]	R/W	**SIF_ON**	SIF Block On/Off Select 0 : SIF OFF Mode 1 : SIF ON	0x0
			SIF Control Register (Default : 16'h00A0)	
0x22 [15:12]	R/W	**RESERVED**	-	0x00
0x22 [11]	R/W	**PiP_MASTER**	PiP REQ signal generation 0 : PiP Slave 1 : PiP Master	0x0
0x22 [10]	R/W	**DEMAND_MODE_SYNC_UPDATE**	Updated DEMAND mode via PKT_END 0 : real time updated register 1 : use Sync-update	0x0
0x22 [9]	R/W	**HEADER_AND_OFF**	Change continuously Header ID 0 : Change Header ID ex) first header ID 0xDF 0xDF, next header ID 0xDF 0xD0 1 : No change Header ID ex) first header ID 0xDF 0xDF, next header ID 0xDF 0xDF	0x0
0x22 [8]	R/W	**REG_DEMAND_ON**	Used Register Demand 0 : Useless 1 : Available control Demod via Register	0x0
0x22 [7]	R/W	**PIP_MODE**	PIP MODE 0 : Not PIP 1 : PIP	0x0
0x22 [6]	R/W	**MS**	Select Master / Slave Mode of SPI 0 : Master 1 : Slave	0x0
0x22 [5]	R/W	**SPI_STB_POL**	Determine the polarity of Strobe(enable) signal of SPI 0 : Active low 1 : Active high	0x0
0x22 [4]	R/W	**DEMAND_MODE**	Demand Input Use or Not 0 : Packet data transfer without Demand 1 : Demand Mode, Transfer start via Demand Signal	0x0
0x22 [3]	R/W	**RESYNC_ON**	Automatically synchronize at RESYNC 0 : Reported without Sync 1 : Synchronizing after RESYNC	0x0
0x22 [2]	R/W	**SPI_HOLD**	Occurs to Data Hold request to set 0 : SPI Go on 1 : SPI Stop and Data Hold	0x0
0x22 [1]	R/W	**HALF_MODE**	Select Transfer Data Size 0 : Data transfer per 16 bit 1 : Data transfer per 8 bit(16bit divide 2) (DSS have to set 8bit)	0x1

0x22 [0]	R/W	**SPI_ON**	FIC Header Insert On/Off 0 : Parallel to Serial Transfer Block Off 1 : Parallel to Serial Transfer	0x1
			SIF Packet Control Register (Default : 16'h0107)	
0x24 [4]	R/W	**TS_PKT**	Transfer per MPEG-TS Packet 0 : Transfer per 192 byte 1 : Transfer per 188 byte	0x01
0x24 [3:0]	R/W	**PKT_NUM**	Set Packet Size When Packetizing 0 : Immediate transfer without Packetinzing 1 ~ 15 : transfer per 1~15 tie	0x0A
			SIF Packet Interval Register (Default : 16'h0107)	
0x26 [15:0]	R/W	**PCK_INTV**	Serial Packet transfer the case of the minimum spacing between Packet (= PCK_INTV * 1/ Baud rate)	0x0400
			SPICR Register (Default : 16'h0107)	
0x28 [15:8]	R/W	**SCR**	Serial clock rate. The SCR is used to generate the transmission and receive bit rate. Baud rate = F(CLK) / 2*(1+SCR) default Baud rate = 24.576 / 4 = 6.144 MHz	0x01
0x28 [7]	R/W	**SPH**	SSPCLKOUT phase control 0 : no clock shift with data 1 : half clock shift with data	0x0
0x28 [6]	R/W	**SPO**	SSPCLKOUT polarity control 0 : first edge – rising 1 : first edge - falling	0x0
0x28 [5:4]	R/W	**FRF**	Frame format select 00 : Motorola SPI 01 : TI SSF 10 : Reserved 11 : Reserved	0x0
0x28 [3:0]	R/W	**DSS**	TX Data size select 0000~0010 : Reserved 0011 : 4-bit data 0100 : 5-bit data 0101 : 6-bit data 0110 : 7-bit data 0111 : 8-bit data 1000 : 9-bit data 1001 : 10-bit data 1010 : 11-bit data 1011 : 12-bit data 1100 : 13-bit data 1101 : 14-bit data 1110 : 15-bit data 1111 : 16-bit data	0x7
			PTR Register	
0x2A [11:0]	R	**SIF_WR_PTR**	Memory WRITE point to the instruction register on Serial Data transfer mode	0x0
0x2C [11:0]	R	**SIF_RD_PTR**	Memory READ point to the instruction register on Serial Data transfer mode	
			PIP_STATE Register	
0x2E [11:0]	R	**PIP_UPDATE**	Check to updated on/off of PIP_MODE	
			ERROR Register (1'h0)	
0x32 [1]	R	**Overflow ERROR**	PIF Memory Overflow 0 : No Error 1 : Error Detection	-
0x32 [0]	R	**RESYNC ERR**	SIF Sync Error 0 : No Error 1 : Error Detection	-
0x34 [0]	W	**RESYNC ERR CLEAR**	Error Clear register	-
			FIC_RD_ADDR_READ Register (Default : 8'h00)	
0x36 [7:0]	R/W	**FIC_RD_ADDR**	FIC Memory Read Address	0x00
			DEMAND INTERVAL COUNTER Register	

0x38 [12:0]	R/W	**DEMAND_INTV_CNT**	Holding SPI bus as value of counter	0x0
			REGISTER DEMAND	
0x3A [0]	W	**REG_DEMAND**	Swap to Demand Value	-
			SPI PAD CONTROL Register	
0x3C [1]	R/W	**SPI_PAD_CTRL_EN**	SPI(CLK, EN, DATA) PAD Control Enable 0 : PAD control via SPI 1 : Control via Register value	0x0
0x3C [0]	R/W	**SPI_PAD_OEn**	SPI PAD OEn signal 0 : Output 1 : Input	0x0

APB SUB-SYSTEM

SYSTEM ARCHITECTURE

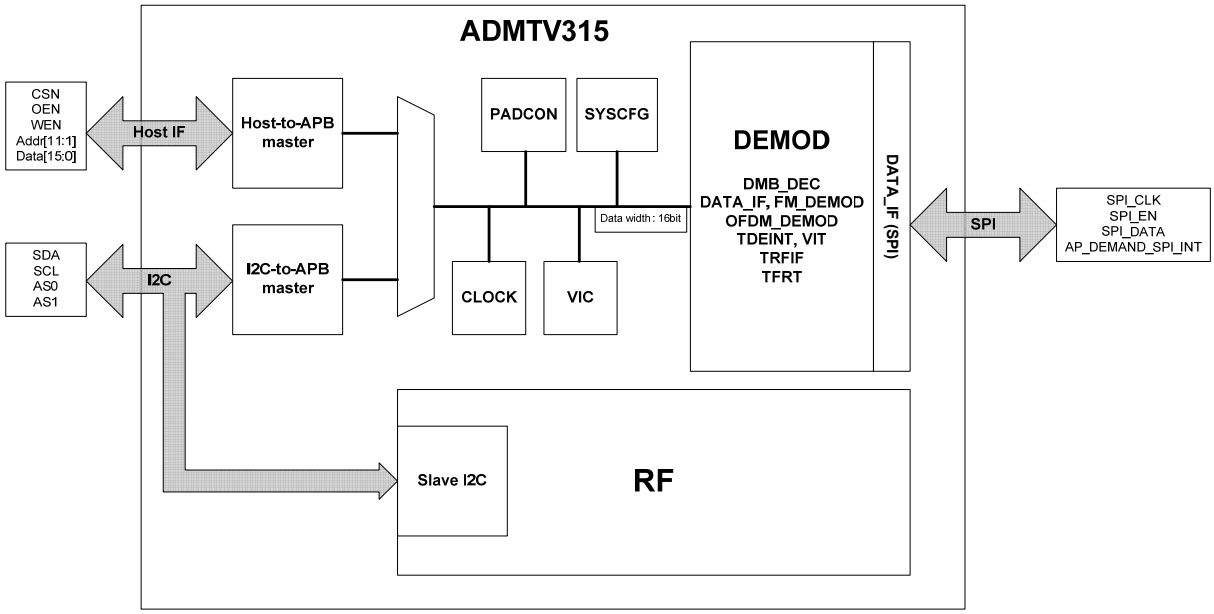


Figure 1137. ADMTV315 System Architecture

ADDRESS MAP

Table 159. APB Sub-System Address Map

Start address [9:0]	End address [9:0]	Description	Size: Half word (2 Byte)
		PSEL_CLK: Clock top	
0×000	0×07F	CLK_TOP	64 Half word
		PSEL_SYSTEM: VIC, SYSCFG, PADCON	
0×080	0×09F	VIC	16 Half word
0×0A0	0×0BF	SYSCFG	16 Half word
0×0C0	0×0DF	PADCON	16 Half word
0×0E0	0×0FF	Reserved	16 Half word
		PSEL_DEC: MT_DEC	
0×100	0×17F	MT_DEC	64 Half word
		PSEL_DATA_IF: DATA_IF, FM_DEMOD	
0×180	0×1BF	DATA_IF	32 Half word
0×1C0	0×1FF	FM_DEMOD	32 Half word
		PSEL_OFDM_DEMOD: OFDM_DEMOD	
0×200	0×27F	OFDM_DEMOD	64 Half word
		PSEL_TDEINT: TDEINT, VIT	
0×280	0×2BF	TDEINT	32 Half word
0×2C0	0×2FF	VIT	32 Half word
		PSEL_TRFIF: TRFIF	
0×300	0×37F	TFRIF	64 Half word
		PSEL_TFRT: TFRT	
0×380	0×3FF	TFRT	64 Half word

NOTES:
The above address values are referenced to [9:0] and they are addressed by AP.

AP CONNECTION DIAGRAM

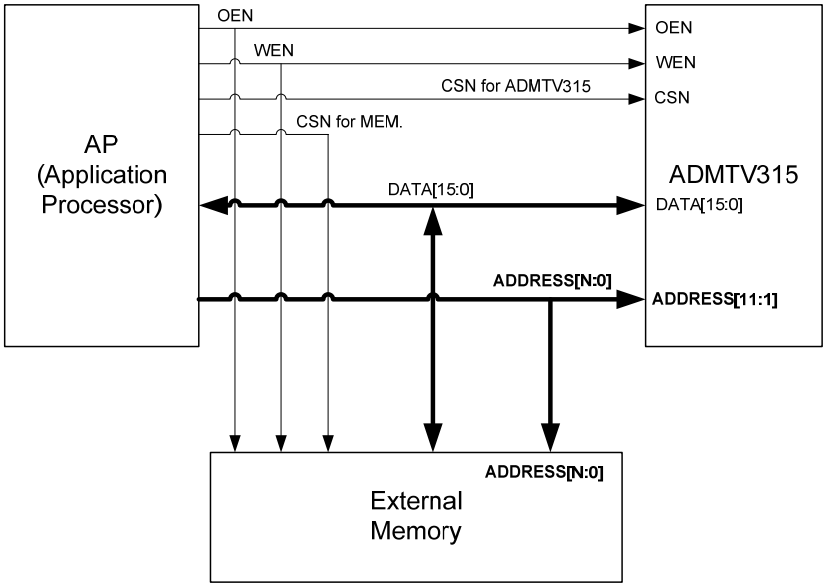


Figure 148. Host Interface Connection Diagram

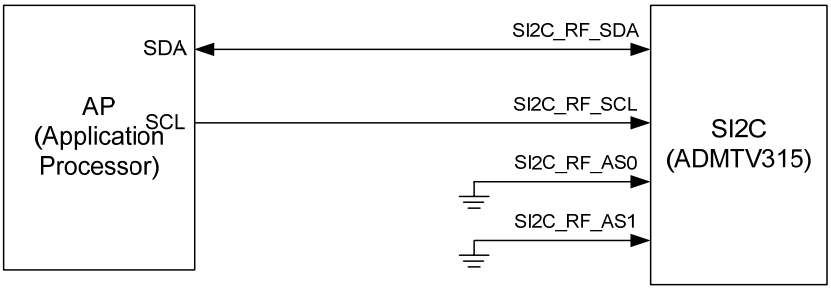


Figure 19. I²C interface Connection Diagram (Stand Alone Package)

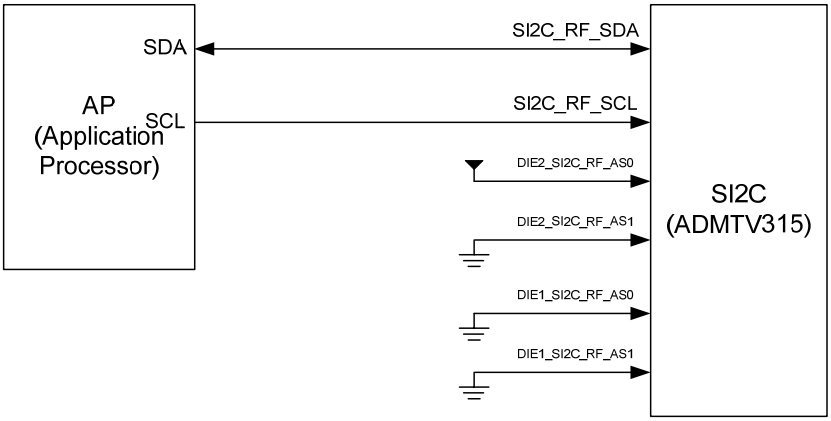


Figure 20. I²C Interface Connection Diagram (2 PIP Package)

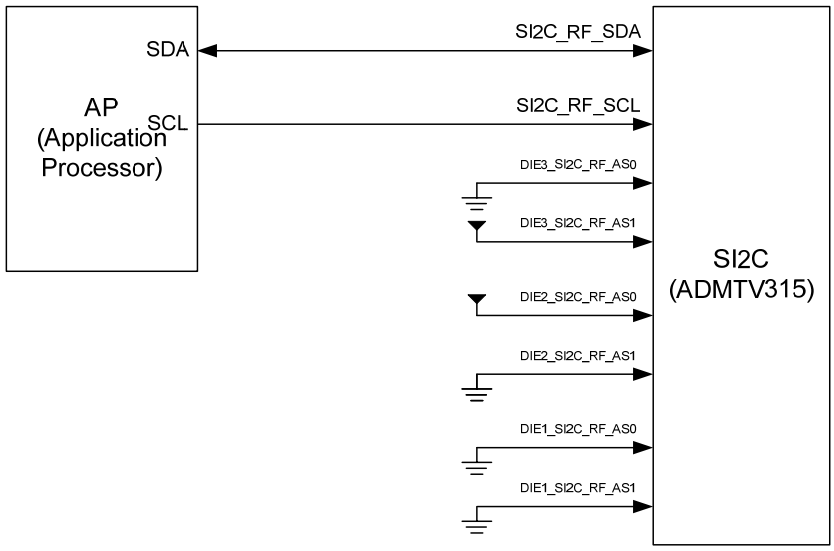


Figure 21 . I²C interface Connection Diagram (3 PIP Package)

APB SUB-SYSTEM COMPONENTS

ADMTV315 is a basic CPUless system that has no internal processor and operates with control signals from CPU of AP. It has an APB master block which converts asynchronous memory interface (Host interface) signal or slave I²C interface (SI²C) signal coming from AP to APB interface signals. MCU of AP can access to all of ADMTV315 registers through this interface.

There are 2-types of access modes in as:

- Normal mode 1: AP accesses to ADMTV315 by Host interface. (See mode table.)
- Normal mode 2: AP accesses to ADMTV315 by SI2C interface. (See mode table.)

Users can select freely one of these modes, which is most suitable for his application purpose. However, internal RF blocks of ADMTV315 can be accessible by SI²C interface only. For stable access by Host interface from AP, there should be timing margin as shown in figure 21.

In this timing diagram, CSB can operate normally only when HOST_ADDR[11:10] has the same value as AS1 and AS0, i.e.,

HOST_ADDR[11:10] = {AS1, AS0}

Host Interface

- Async. Memory (SRAM) interface
- Mode pin set to normal mode 1.
- 16bit access (half word) only

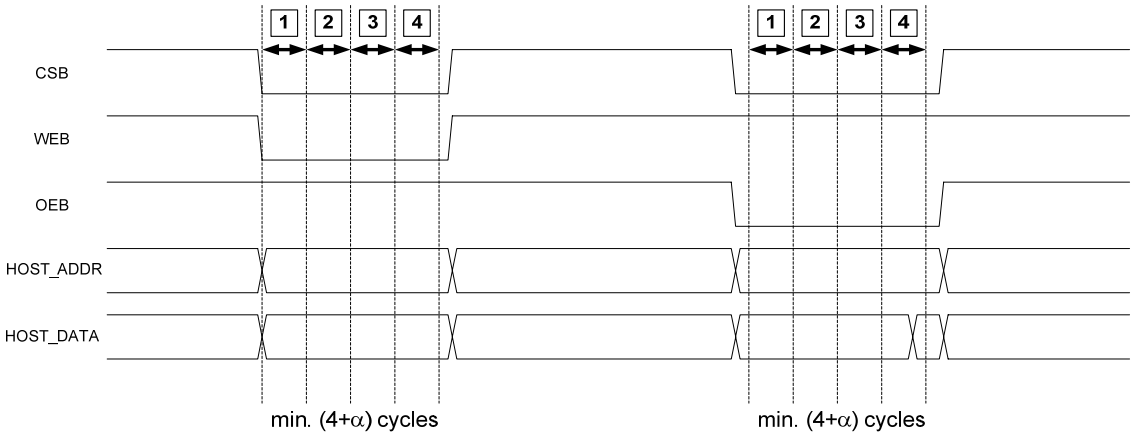


Figure 22. Read/Write Access Timing Diagram

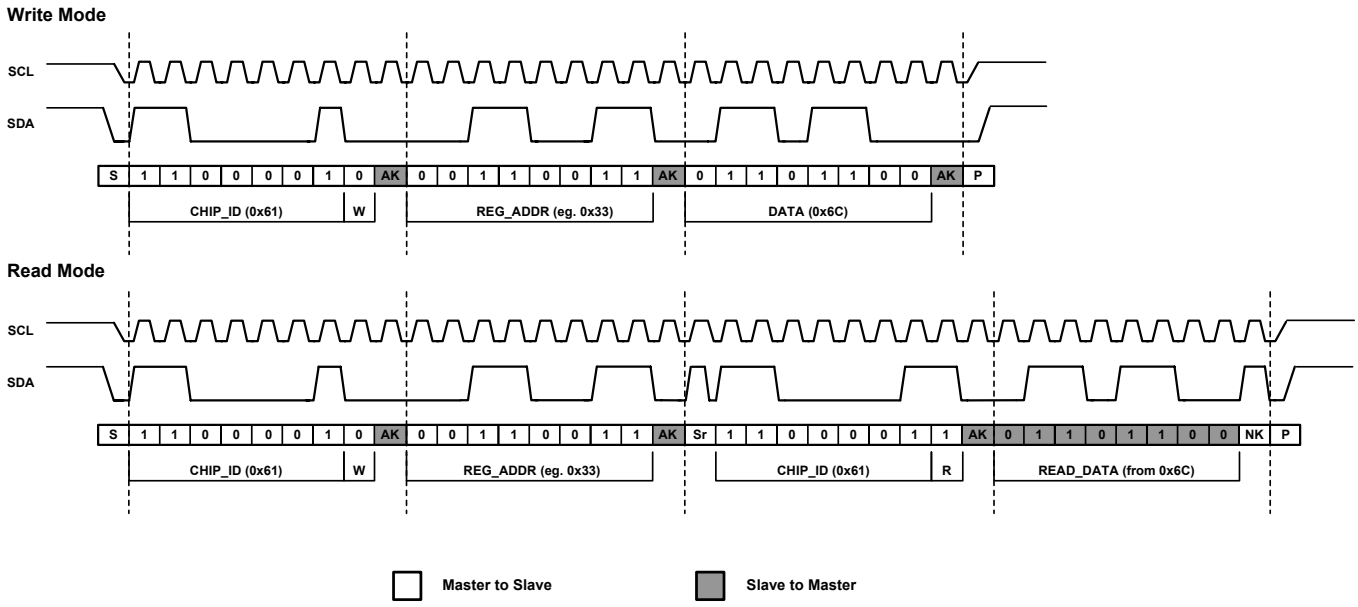
SI²C Interface

- Slave only interface
- Mode pin set to normal mode 2.
- Supports both of standard mode (100 kbps) and fast mode (400 kbps)
- Baseband I²C features
  - Slave address length = 6bits.
  - MSB 4bits (A5 ~ A2) value = b1010. LSB 2 bits (A1 ~ A0) is obtained from primary input (AS1, AS0).
  - Register address = 9bits.
  - I²C basic functional combinations are 2-byte write-access, 2-byte read-access and multiple write-accesses.
- RF Tuner I²C features
  - Slave address length = 7bits.
  - MSB 4bits (A6 ~ A0) value = b1100001. (0×61)
  - Register address = 8 bits.
  - I²C basic functional combinations are 1-byte write-access, 1-byte read-access and multiple write-accesses.

I²C Timing Characteristics

(T_A = 25°C, V_{DDIO} = 3.3 V, GND = 0 V, unless otherwise noted.)

According to standard I²C specification, the CLK frequency reaches maximum 400 kHz in fast-mode and 100 kHz in standard-mode. To communicate with RF tuner, you need to comply as the following timing diagrams.



NOTES
S = Start condition, P = Stop condition, Sr = Repeated Start (Stop + Start, fast transition) condition, AK = Acknowledge: Active low, NK = Not Acknowledge: Active high, W = Write mode, R = Read mode
CMC52100-S1 needs a stop transition in the repeated start condition. Therefore, upper access condition is able to be modified on standard I²C.

Figure 23. Serial Control Port Write/ Read Mode

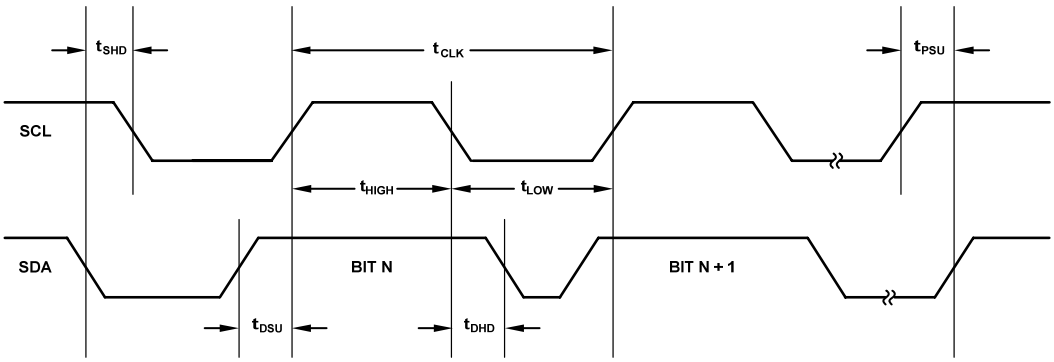


Figure 2154. Serial Control Port Timing

Table 20. Serial Control Port Timing

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
Hold Time (Repeat) Start Condition[1]	t_{SHD}	4.0		0.6		µs
SCL Clock Period	t_{CLK}	0	100	0	400	kHz
HIGH Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
LOW Period of the SCL Clock	t_{LOW}	4.7		1.3		µs
Set-up Time for STOP Condition	t_{PSU}	4.0		0.6		µs

Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
Data Set-up Time	t_{DSU}	250		100[2]		ns
Data Hold Time for I²C Bus Devices.	t_{DHD}	5.0				µs
		0[3]	3.45[4]	0[3]	0.9[4]	µs

NOTES
[1]Afer this period, the first clock pulse is generated.
[2]A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{DSU} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.
[3]A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
[4]The maximum t_{DHD} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

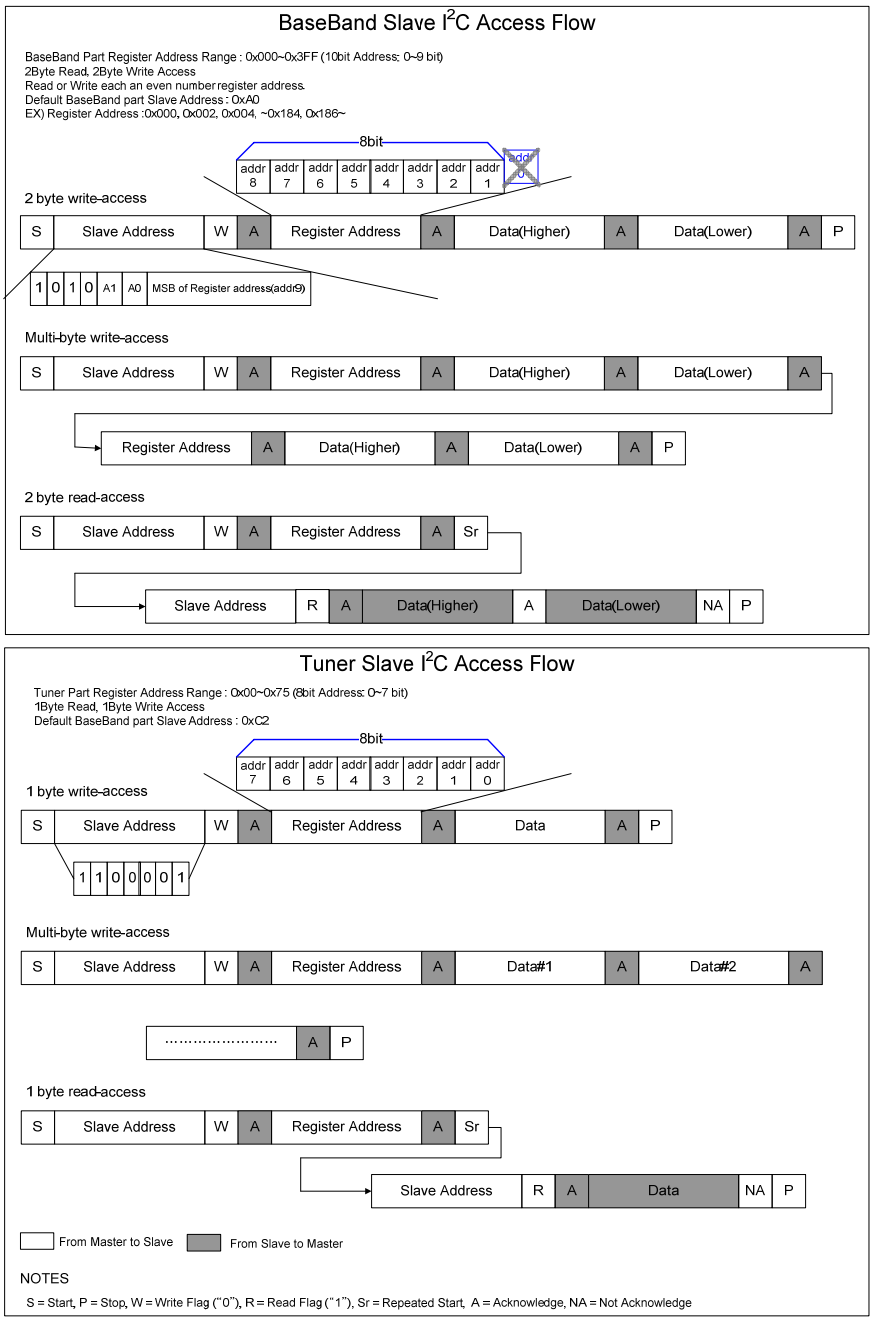


Figure 25. Functional Combination

Vectored Interrupt Controller

The VIC provides a software interface to the interrupt system. In a system with an interrupt controller, software must determine the source that is the requesting service and where its service routine is loaded. A VIC does both of these in hardware. It supplies the interrupt index of the corresponding to the highest priority requesting interrupt source.

The interrupt vector [0] has the highest priority, followed by interrupt vector [1] ~ [15]. In addition, interrupt vector0 has the higher priority than interrupt vector1. The priority of each of the vectored interrupt is programmable, enabling the order the interrupt are served in to be dynamic changing. This is done by programming the value in the vector priority registers. If multiple interrupts are set to the same-programmed priority level, the fixed hardware priority level is used to determine the order the interrupts on that level are serviced. This is also applicable when the priority registers are not programmed. Interrupt [0] has the highest hardware priority level, and interrupt [15] has the lowest. The software can control each request line to generate software interrupts.

There are 32-vectored interrupts available. Reading from the vector interrupt index register, VIC_INDEX, provides the fixed index of the interrupt sources, and the updates the interrupt priority hardware that masks out the current and any lower priority interrupt requests. Writing to the VIC_INDEX register indicates to the interrupt priority hardware that current interrupt is served, enabling the masking of lower priority or the same priority interrupts to be removed and for the interrupts to become active.

There are several features as follows.

- Support for 16 vectored interrupts
- Fixed hardware interrupt priority levels
- Programmable interrupt priority levels
- Software interrupt generation
- Raw interrupt status
- Interrupt request status

S/W setting guide for boot-up

1. Clear INT_PEND* register (mandatory)
2. Set VIC_PRIORITY_*_* register for each interrupt (not mandatory)
3. Set INTENABLE* register for each interrupt (mandatory)

Interrupt Service Routine procedure

1. Read INT_INDEX register and branch to the Interrupt Service Routine
2. Clear INT_PEND register for corresponding interrupt
3. Execute your ISR
4. Write any value to INT_INDEX register and return from the interrupt.

APPLICATIONS

BGA PACKAGE TYPE

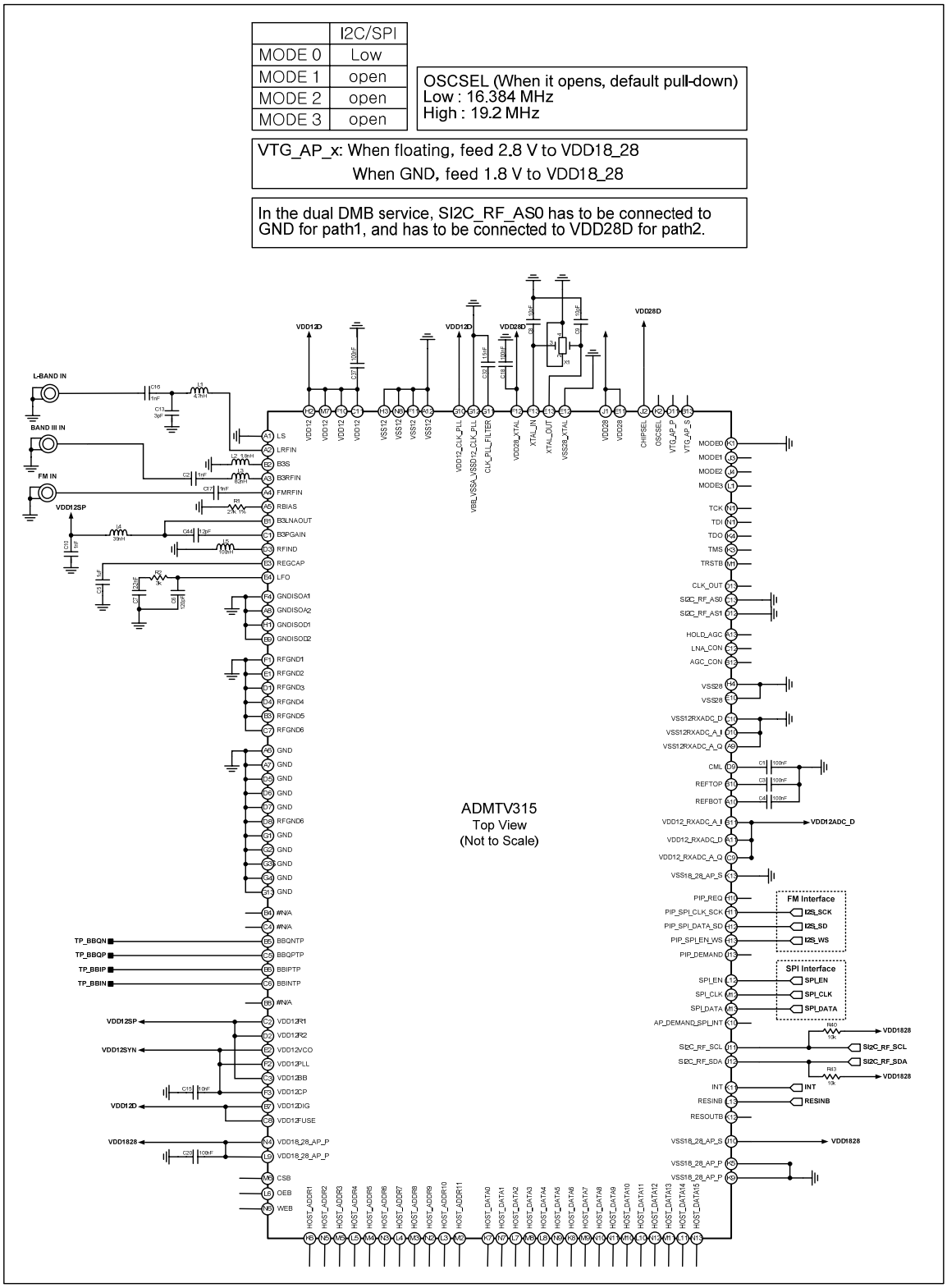


Figure 26. SPI Application Schematic

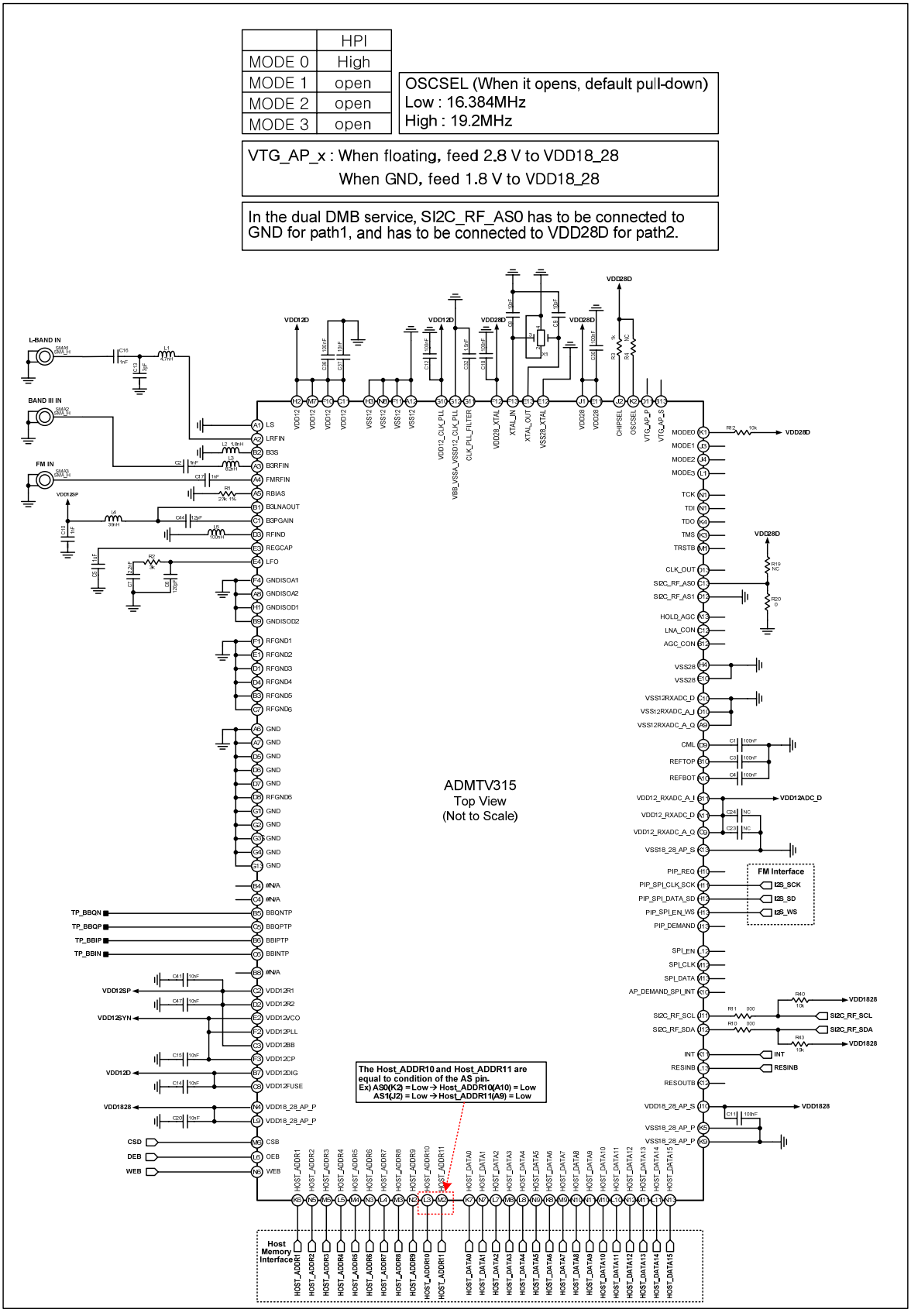


Figure 27. Host Interface Application Schematic

WLCSP PACKAGE TYPE

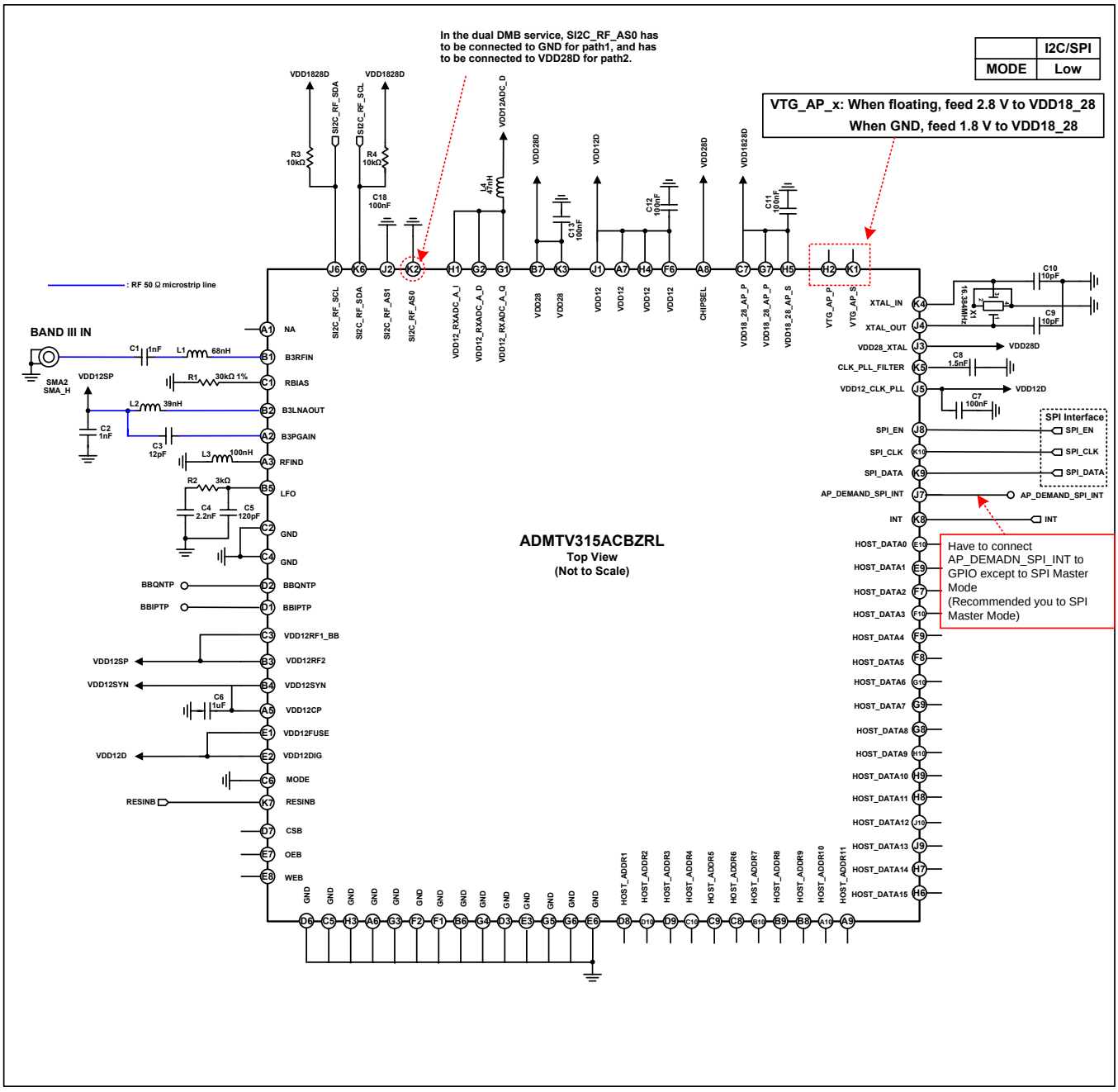


Figure 28. SPI Application Schematic

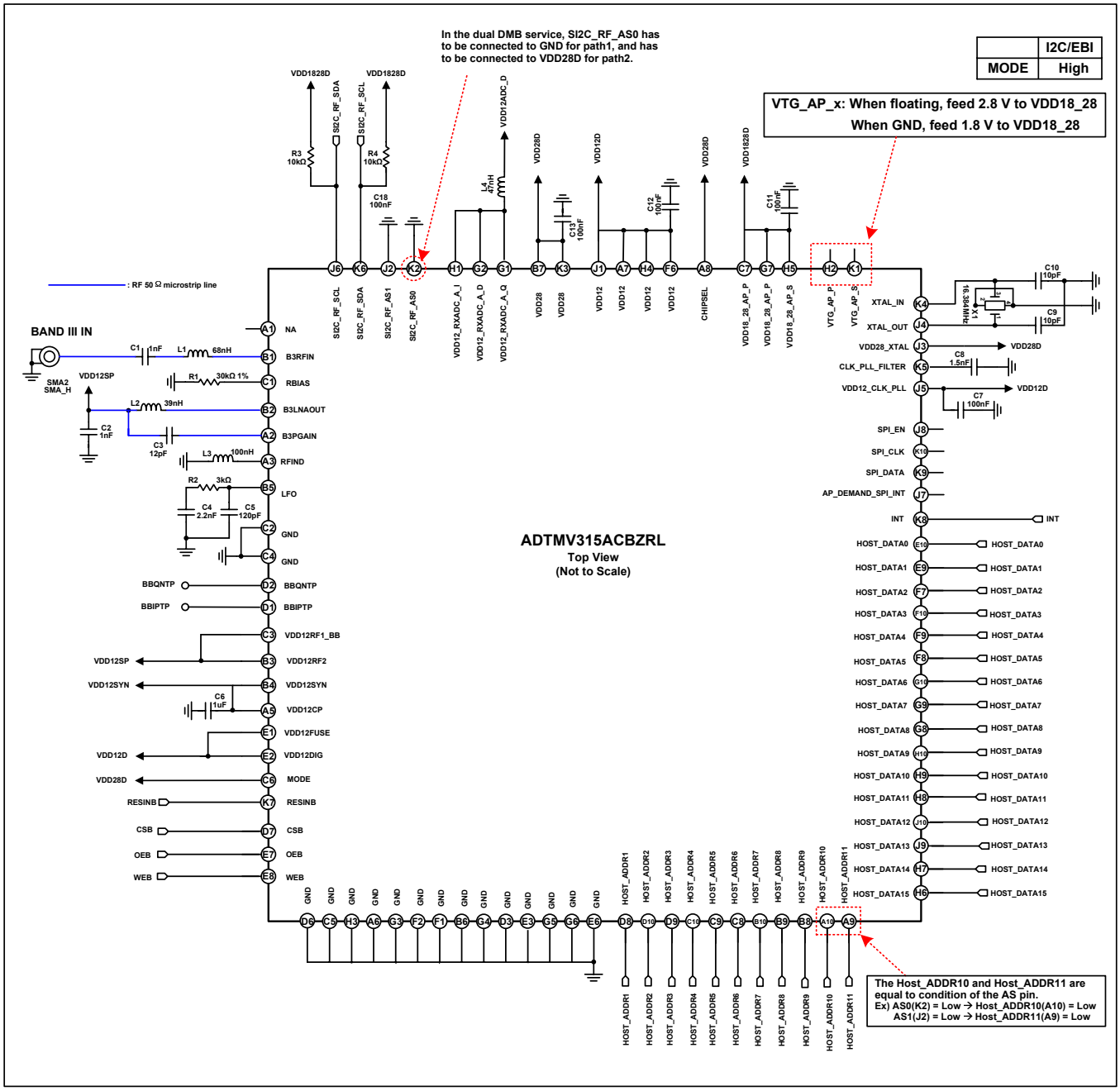


Figure 216. Application Host Interface Schematic

OUTLINE DIMENSIONS

BGA PACKAGE TYPE

Package

- Size: 7 × 7mm²
- Max height: 1.0 mm
- Ball Array: 13 × 13 matrix, 4 rows, 144 balls, 0.5 mm pitch

Solder Ball

- Lead-free
- 0.3 mm diameter

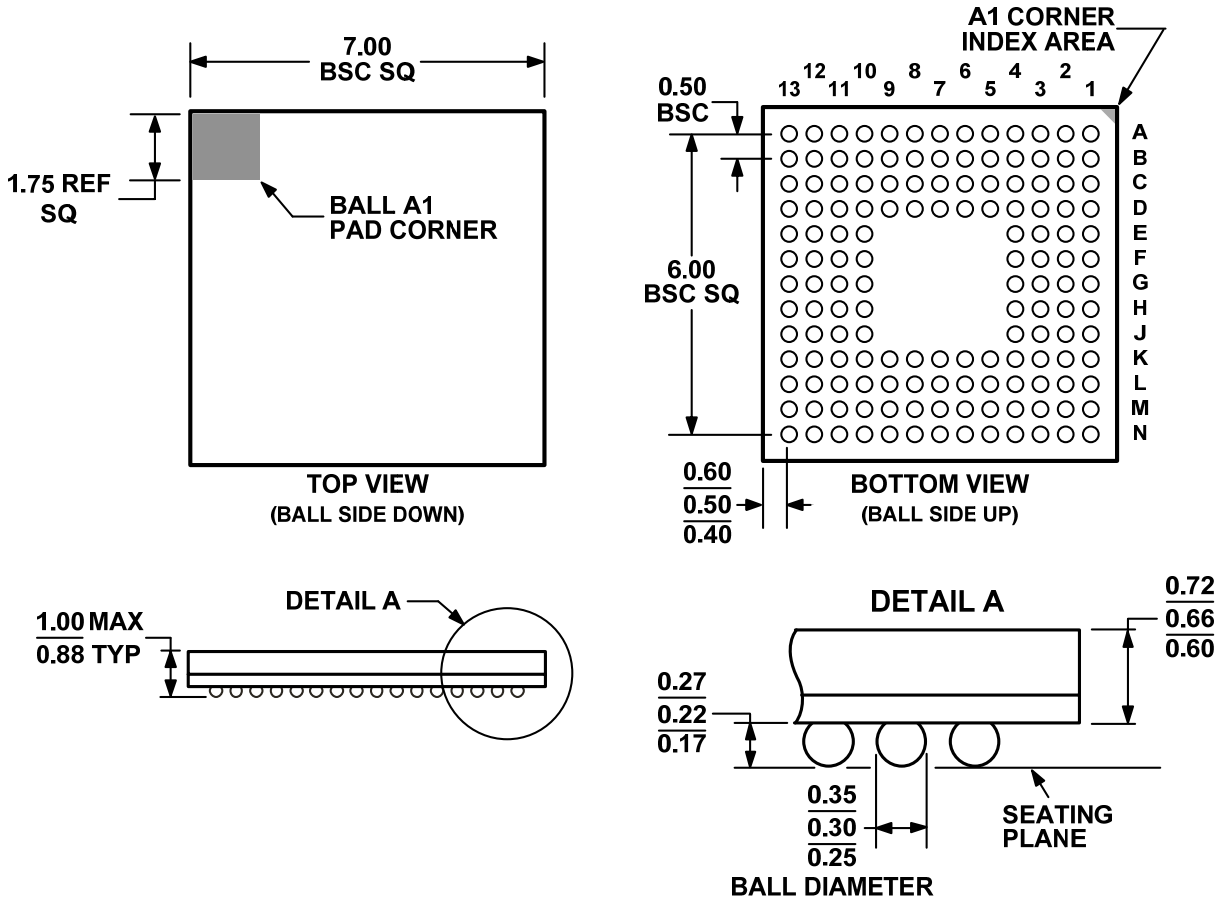


Figure 29. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
7 mm x 7 mm Body
(CB-144)
Dimensions shown in millimeters

WLCSP PACKAGE TYPE

Package

- Size: 5 x 5mm
- Max Height: 0.75mm
- Ball Array: 10 x 10 depopulated, 92 balls, 0.45mm pitch

Solder Ball

- Lead-free
- 0.3 mm diameter

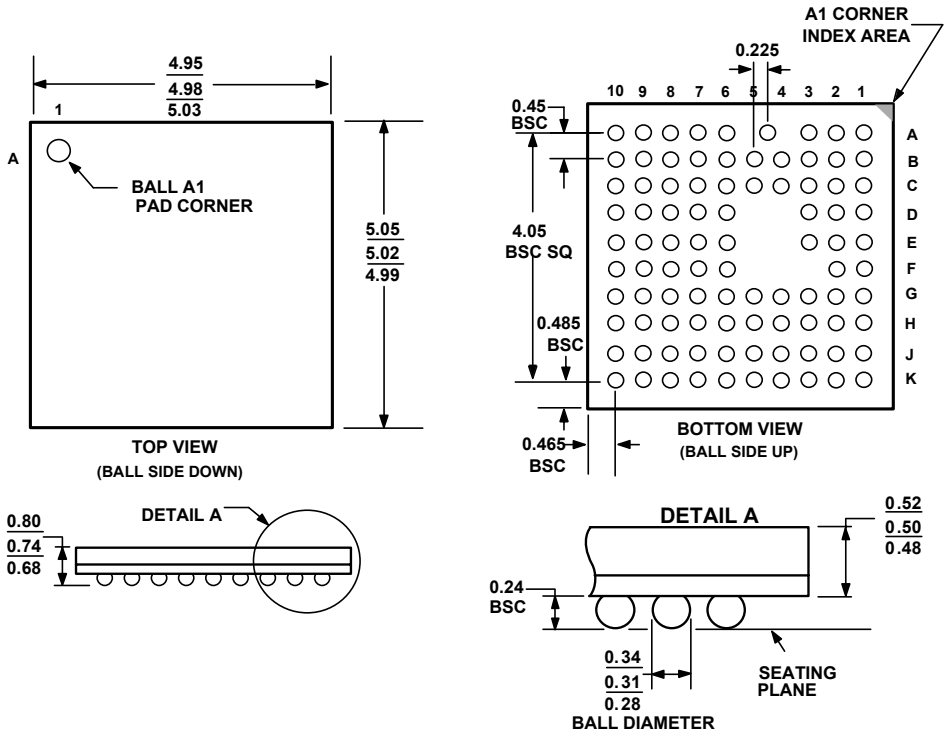


Figure 30. 75-Ball Wafer Level Chip Scale Package [CSP]
5 mm x 5 mm Body
(CB-92)
Dimensions shown in millimeters

ORDERING GUIDE

Note) ADMTV315ACBZRL does not support for L-Band and HMI(Host Memory Interface.)

PKG	Description	Ordering Guide	Marking	SAP Registration
CSP-BGA	Band-III/FM	ADMTV315ABCZRL	315A	o
	Band-III/FM/L-Band	ADMTV315BBCZRL	315B	o
CSP	Band-III	ADMTV315ACBZRL	315A	o
Eval. Board	Evaluation Board for ADMTV315A	ADMTV315AC-EB		
	Evaluation Board for ADMTV315B	ADMTV315BC-EB		
	Evaluation Board for ADMTV315A	ADMTV315AW-EB		

NOTES

PR07978-0-12/08(PrA)