Mobile TV One-chip Receiver for T-DMB/DAB/FM

Preliminary Technical Data

ADMTV316

FEATURES

RF Tuner and Demodulator SoC for T-DMB/DAB/FM
Supports Dual-band: Band III and FM
Wide Dynamic Range: -100 dBm ~ 0 dBm in 50 Ω
Simultaneously receive 2 channels for PiP
Low Power Consumption in PiP mode: 200 mW
Selectable Reference Clock: 16.384/19.2 MHz
1.2 V Supply Voltage for Core and 1.8/2.8 V Dual Supply Voltage selectable for I/O
Supports JTAG I/O Boundary Scan
Fully Compliant to T-DMB Standards in Korea and ETSI 300 401 Physical Layer Definition
Satisfied TTAS.KO-07.0024 Specification of the data Services for VHF Digital Multimedia Broadcasting
Supports ETSI EN 300 744 (204,188) Outer Coder
192-Balls Chip Scale Package Ball Grid Array (CSP_BGA)
9 × 9 mm² × 1.2 mm, 0.5 mm pitch

FUNCTIONAL BLOCK DIAGRAMS

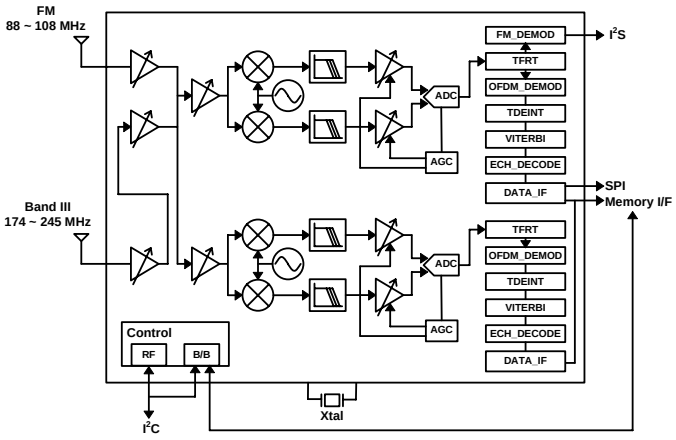

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

ADMTV316 is a highly integrated SoC (System-on-Chip) T-DMB/DAB receiver, which supports dual bands (Band III and FM). This device is composed of high performance RF front-end tuner and OFDM (Orthogonal Frequency Division Multiplex) demodulator in a small-size single package. The zero-IF down-conversion RF front-end includes LNA, RF PGA, mixer, high-resolution fractional-N PLL, on-chip low phase noise VCO, BB PGA, and automatic cutoff frequency-tuning LPF. The baseband of ADMTV316 includes 10bit ADC, OFDM demodulator and FEC/audio/data decoders. This device supports various serial interfaces such as I^2C, I^2S, and SPI to make interface with external devices more flexible. With good sensitivity and wide dynamic range, ADMTV316 is the best solution for T-DMB/DAB application. It is designed to comply with TTAS.KO-07.0024 specification of the data services for VHF Digital Multimedia Broadcasting (T-DMB) and ETSI EN 300 401 (European DAB).

The additional features of ADMTV316 are as follows:

- Supports transmission mode 1, 2, 3 and 4
- Supports digital frequency control and timing control
- Supports simultaneous channel reception
  - Maximum 64 sub-channels
  - 4 enhanced channels (TDMB/ESM/EPM)
- Supports various AP (HOST) interfaces
  - SRAM Base parallel interface (control + data)
  - Serial interface (control: I^2C, data: SPI)
  - Single SPI interface at PIP mode
- Supports TII reception
- Supports FM reception
- Supports automatic setting with Multiplex Configuration Information decoder
  - CIF counter synchronization
  - Multiplex configuration & reconfiguration
  - Enhanced channel (TDMB/EPM)
- Supports full capacity channel decoding
- Minimized external components
  - No external system memory
  - Bit de-interleaver memory included

Rev. PrA

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TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

OPERATING CONDITIONS

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD} (1.2 V)	1.1	1.2	1.3	V
	V_{DD} (1.8 V)	1.65	1.8	1.95	V
	V_{DD} (2.8 V)	2.5	2.8	3.1	V
Input/Output Voltage	V_{IN}/V_{OUT}	1.65		1.95	V
		2.5		3.1	V
Operating Ambient Temperature	T_{opr}	−40		85	°C

TIMING DIAGRAM

Table 2. Digital Timing Diagram

Characteristic	Symbol	Min	Unit
PD Set-up Margin	a	Don't Care	µs
Power up Set-up Margin for V_{DD18}	b	Don't Care	µs
Power up Set-up Margin for V_{DDIO}	c	Don't Care	µs
RESETB Set-up Time for RESETB	d	100	µs
Set-up Time for I^2C Interface	e	100	µs

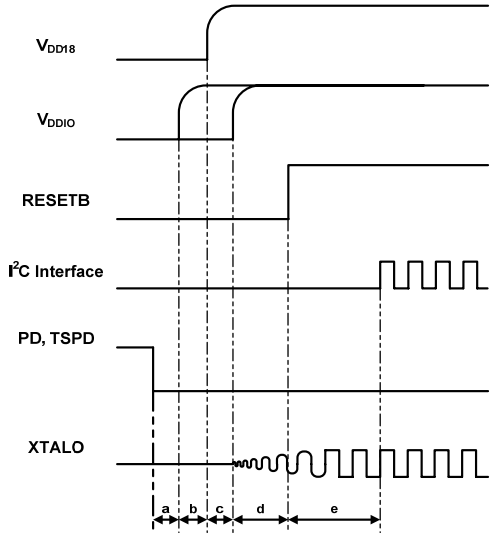


Figure 2. Digital Timing Diagram

ELECTRICAL CHARATERISTICS

Table 3. 1.8 V DC Electrical Characteristics

Ambient temperature = 25°C, all 1.8 V supplies = 1.65 V to 1.95 V, unless otherwise noted.

Parameter	Condition		Symbol	Min	Typ	Max	Unit
Input High Current	Normal	$V_{IN} = V_{DD}$	I_{IH}	-5		5	µA
	Down	Pull - Down		1		30	µA
Input Low Current	Normal	$V_{IN} = V_{SS}$	I_{IL}	-5		5	µA
	Up	Pull - Up		-30		-1	µA
Input High Voltage	CMOS		V_{IH}	0.65× V_{DD}			V
Input High Voltage	SCMOS		V_{T+}			0.7× V_{DD}	V
Input Low Voltage	CMOS		V_{IL}			0.35× V_{DD}	V
Input Low Voltage	SCMOS		V_{T-}	0.3× V_{DD}			V
Output High Voltage	I_{OH} = Drive Current		V_{OH}	V_{DD} - 0.45			V
Output Low Voltage	I_{OL} = Drive Current		V_{OL}			0.45	V
Tri-state Output Leakage Current	$V_{OUT} = V_{DD}$ of V_{SS}		I_{OZ}	-10		10	µA

Table 4. 2.8 V DC Electrical Characteristics

Ambient temperature: 25°C, all 2.8 V supplies = 2.5 V to 3.1 V, unless otherwise noted.

Parameter	Condition		Symbol	Min	Typ	Max	Unit
Input High Current	$V_{IN} = V_{DD}$	Normal	I_{IH}	-5		5	µA
	Pull - Down	Down		5		60	µA
Input Low Current	$V_{IN} = V_{SS}$	Normal	I_{IL}	-5		5	µA
	Pull - Up	Up		-60		-5	µA
Input High Voltage	CMOS		V_{IH}	0.65× V_{DD}			V
Input High Voltage	SCMOS		V_{T+}			0.7× V_{DD}	V
Input Low Voltage	CMOS		V_{IH}			0.35× V_{DD}	V
Input Low Voltage	SCMOS		V_{T-}	0.3× V_{DD}			V
Output High Voltage	I_{OH} = Drive Current		V_{OH}	V_{DD} - 0.45			V
Output Low Voltage	I_{OL} = Drive Current		V_{OL}			0.45	V
Tri-state Output Leakage Current	$V_{OUT} = V_{DD}$ of V_{SS}		I_{OZ}	-10		10	µA

Table 5. FM AC Electrical Characteristics

Ambient temperature: 25°C, all 1.2 V supplies = 1.1 V to 1.3 V, 2.8 V supplies = 2.7 V to 2.9 V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
FM RF Frequency Range	f_{FM}	88		108	MHz
RF input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
Sensitivity	P_{MIN}		7		dBµV

Table 6. Band III AC Electrical Characteristics

Ambient temperature: 25°C, all 1.2 V supplies = 1.1 V to 1.3 V, 2.8 V supplies = 2.7 V to 2.9 V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Band-III RF Frequency Range	$f_{Band-III}$	174		245	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1	3:1	
Sensitivity @ BER	P_{MIN}		-100	-97	dBm
Max Input Power @ BER	P_{MAX}	0			dBm
Digital Adjacent Channel Rejection (n+1)	ACR_{DN+1}	30	37		dBc
Digital Adjacent Channel Rejection (n-1)	ACR_{DN-1}	30	37		dBc
Far-off (+5 MHz)	FO_{+5MHz}	40	47		dBc
Far-off (-5 MHz)	FO_{-5MHz}	40	47		dBc

ELECTROSTATIC CHARATERISTICS

Table 7. Electrostatic Characteristics

Characteristic	HBM	MM	Remarks
Vdd Positive	> 1000 [V]	> 100 [V]	
Vdd Negative	> 1000 [V]	> 100 [V]	
Vss Positive	> 1000 [V]	> 100 [V]	
Vss Negative	> 1000 [V]	> 100 [V]	

ABSOLUTE MAXIMUM RATINGS

Table 8. (T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Rating
DC Supply Voltage	V_{DD} (1.2 V)	1.7 V
	V_{DD} (1.8 V)	2.3 V
	V_{DD} (2.8 V)	3.3 V
Input/Output Voltage	V_{IN}/V_{OUT} (1.2 V)	1.7 V
	V_{IN}/V_{OUT} (1.8 V)	2.3 V
	V_{IN}/V_{OUT} (2.8 V)	3.3 V
DC Input Current	L_{IN}	±200 mA
Storage Temperature	Tstg	–65°C to +150°C

NOTES
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN MAP

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	Path2_B3 RFIN	Path1_B3 RFIN	Path1_FM RFIN	VDD12BB	Path1_RBIAS	GND	GND	GNDISOD2	NC	NC	NC	VDD12_RXA DC_D	VDD12_RXA DC_A_I	VDD12_4	NC	A
B	VDD12RF1	NC	Path2_B3S	Path1_B3S	NC	Path2_RBIAS	BBQNTP	NC	GNDISOA2	Path2_CML	Path2_REF BOT	Path2_REF TOP	VSS12_RXA DC_D	NC	Path2_HOLD _AGC	Path1_HOLD _AGC	B
C	NC	Path2_B3 LNAOUT	Path1_B3 LNAOUT	NC	RFGND5	Path1_BB AGC	BBQPTP	VDD12DIG	NC	Path1_CML	Path1_REF BOT	Path1_REF TOP	VSS12_RXA DC_A_I	NC	Path2_AGC_ CON	Path1_AGC_ CON	C
D	Path1_B3P GAIN	Path2_B3P GAIN	NC	Path2_RF RSSI	NC	Path2_BB AGC	BBINTP	BBIPTP	VDD12FUSE	VSS12_RXA DC_A_Q	VSS12_RXA DC_A_Q	VSS12	VTG_AP_S	NC	Path2_LNA_ CON	Path1_LNA_ CON	D
E	Path1_RFIND	Path2_RFIND	NC	Path1_RF RSSI									VTG_AP_P	Path1_SI2C_ RF_AS1	Path2_SI2C_ RF_AS1	NC	E
F	RFGND3	RFGND2	VDD12VCO	RFGND4									VDD28_2	Path1_SI2C_ RF_AS0	Path2_SI2C_ RF_AS0	NC	F
G	Path1_REG CAP	Path2_REG CAP	NC	VDD12RF2									VSS28	VSS28_ XTAL	VDD28_ XTAL	NC	G
H	RFGND1	VDD12PLL	VDD12CP	GNDISOA1									VSS12	VDD12_3	XTAL_IN	XTAL_OUT	H
J	Path1_LFO	Path2_LFO	NC	GNDISOD1									VBB_VSSA_ VSSD12_ CLK_PLL	NC	NC	NC	J
K	NC	VDD12_1	VDD28_1	VSS12									VDD12_CLK _PLL	PIP_SPI DATA_SD	Path2_CLK_ PLL_FILTER	Path1_CLK_ PLL_FILTER	K
L	Path1_CHIP SEL	Path2_CHIP SEL	NC	VSS28									PIP_SPI EN_WS	PIP_SPI CLK_SCK	NC	NC	L
M	MODE0	MODE1	MODE2	OSCSEL									SI2C_RF_SD A	SI2C_RF_SC L	NC	NC	M
N	MODE3	TMS	NC	VDD18_28_A P_P_1	VSS18_28_A P_P	GND	VDD12_2	VSS12	VDD18_28_A P_P_2	VSS18_28_A P_P	HOST_DATA 13	VSS18_28_A P_S	VDD18_28_A P_S	RESINB	NC	NC	N
P	TRSTB	TCK	HOST_ADDR 9	HOST_ADDR 6	HOST_ADDR 1	CSB	HOST_DATA 2	HOST_DATA 3	HOST_DATA 7	HOST_DATA 9	HOST_DATA 12	Path1_INT	Path2_INT	NC	NC	NC	P
R	NC	HOST_ADDR 11	HOST_ADDR 8	HOST_ADDR 5	HOST_ADDR 2	WEB	HOST_DATA 1	HOST_DATA 4	HOST_DATA 6	HOST_DATA 10	HOST_DATA 11	HOST_DATA 15	AP_DEMAND _SPI_INT	SPI_DATA	NC	NC	R
T	NC	HOST_ADDR 10	HOST_ADDR 7	HOST_ADDR 4	HOST_ADDR 3	OEB	HOST_DATA 0	NC	HOST_DATA 5	HOST_DATA 8	NC	HOST_DATA 14	SPI_EN	SPI_CLK	NC	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

ADMTV316
Top View
9x9mm BGA 192balls

Figure 3. ADMTV316 Pin Map

Table 9. Operation Mode

Operation Mode	MODE3	MODE2	MODE1	MODE0	CHIPSEL
NORMAL 1	1	1	1	1	1
NORMAL 2	1	1	1	0	1
CHIP_DISABLE	X	X	X	X	0

Normal 1: Host Memory interface (Parallel I/F) used for DMB BB register access

Normal 2: I^2C interface (Serial I/F) used for DMB BB register access (I^2C is used for RF register access in normal 1 and 2.)

Table 10. Dual Voltage Selection

Voltage Selection Pin	Value	Voltage Selection
VTG_AP_P	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Parallel Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Parallel Interface with AP
VTG_AP_S	1	2.8 V (2.5 ~ 3.1 V) Interface Pin for Serial Interface with AP
	0	1.8 V (1.65 ~ 1.95 V) Interface Pin for Serial Interface with AP

Voltage source and IO list influenced by VTG_AP_P (Parallel I/F IO)

- Voltage source: VDD18_28_AP_P
- IO: CSB, OEB, WEB, HOST_ADDR (11:1), HOST_DATA (15:0)

Voltage source and IO list influenced by VTG_AP_S (Serial I/F IO and IO connected to AP)

- Voltage source: VDD18_28_AP_S
- IO: INT, RESINB, RESOUTB, SI2C_RF_SCL, SI2C_RF_SDA, SPI_CLK, SPI_DATA, SPI_EN, AP_DEMAND_SPI_INT, PIP_SPI_CLK_SCK, PIP_SPI_DATA_SD, PIP_SPI_EN_WS, PIP_DEMAND, PIP_REQ

Table 11. Pin Function Descriptions

Pin Name	Ball	Dir[1]	Voltage(V)	Pad Type	Drive(mA)	Description
Clock, Reset, Mode, VTG, CHIPSEL (12 Pin)						
MODE0	M1	I	2.8	IS-PU		Path1,2 MODE selection 0
MODE1	M2	I	2.8	IS-PU		Path1,2 MODE selection 1
MODE2	M3	I	2.8	IS-PU		Path1,2 MODE selection 2
MODE3	N1	I	2.8	IS-PU		Path1,2 MODE selection 3
XTAL_IN	H15	I	2.8	IXA		Path1 XTAL clock input
XTAL_OUT	H16	O	2.8	OXA		Path1 XTAL clock output
OSCSEL	M4	I	2.8	IS-PD		Path1,2 Oscillator selection 0: 16.384 MHz 1: 19.2 MHz
RESINB	N14	I	1.8 / 2.8	ISL		Path1 Chip reset & AP I/F Hi-Z control (Maintain RESINB=L at Chip off)
VTG_AP_P	E13	I	2.8	IS-PU		Path1,2 AP IO voltage selection for parallel interface
VTG_AP_S	D13	I	2.8	IS-PU		Path1,2 AP IO voltage selection for serial interface
Path1_CHIPSEL	L1	I	2.8	IS-PD		Path1 Test chip selection in PiP test
Path2_CHIPSEL	L2	I	2.8	IS-PD		Path2 Test chip selection in PiP test
RF Interface (6 Pin)						
Path1_AGC_CON	C16	O	2.8	Z5-PD	5	Path1 Automatic gain control signal
Path1_LNA_CON	D16	O	2.8	Z5-PD	5	Path1 LNA step control signal
Path1_HOLD_AGC	B16	O	2.8	Z5-PD	5	Path1 AGC hold control for null period
Path2_AGC_CON	C15	O	2.8	Z5-PD	5	Path2 Automatic gain control signal
Path2_LNA_CON	D15	O	2.8	Z5-PD	5	Path2 LNA step control signal
Path2_HOLD_AGC	B15	O	2.8	Z5-PD	5	Path2 AGC hold control for null period
Application Processor Interface (32 Pin)						
HOST_ADDR1	P5	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 1
HOST_ADDR2	R5	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 2
HOST_ADDR3	T5	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 3
HOST_ADDR4	T4	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 4
HOST_ADDR5	R4	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 5
HOST_ADDR6	P4	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 6
HOST_ADDR7	T3	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 7
HOST_ADDR8	R3	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 8
HOST_ADDR9	P3	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 9
HOST_ADDR10	T2	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 10
HOST_ADDR11	R2	I	1.8 / 2.8	IS-PD		Path1,2 AP parallel interface address 11
CSB	P6	I	1.8 / 2.8	ISL-PU		Path1,2 Chip select
WEB	R6	I	1.8 / 2.8	ISL-PU		Path1,2 Write Enable
OEB	T6	I	1.8 / 2.8	ISL-PU		Path1,2 Out Enable
HOST_DATA0	T7	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 0
HOST_DATA1	R7	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 1
HOST_DATA2	P7	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 2
HOST_DATA3	P8	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 3
HOST_DATA4	R8	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 4
HOST_DATA5	T9	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 5

Pin Name	Ball	Dir[1]	Voltage(V)	Pad Type	Drive(mA)	Description
HOST_DATA6	R9	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 6
HOST_DATA7	P9	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 7
HOST_DATA8	T10	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 8
HOST_DATA9	P10	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 9
HOST_DATA10	R10	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 10
HOST_DATA11	R11	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 11
HOST_DATA12	P11	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 12
HOST_DATA13	N11	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 13
HOST_DATA14	T12	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 14
HOST_DATA15	R12	B	1.8 / 2.8	BX3-KP	3	Path1,2 AP parallel interface data 15
Path1_INT	P12	O	1.8/2.8	O3	3	Path1 Interrupt
Path2_INT	P13	O	1.8 / 2.8	O3	3	Path2 Interrupt
SPI Interface (4 Pin)						
SPI_CLK	T14	B	1.8 / 2.8	BS3-PD	3	Path1 SPI interface clock signal
SPI_EN	T13	B	1.8 / 2.8	BS3-PU	3	Path1 SPI interface enable signal
SPI_DATA	R14	B	1.8 / 2.8	BS3-PD	3	Path1 SPI interface data signal
AP_DEMAND_SPI_INT	R13	B	1.8 / 2.8	BS3-PU	3	Path1,SPI interface demand/interrupt
I²S Interface (3 Pin)						
PIP_SPI_CLK_SCK	L14	B	1.8 / 2.8	BS3-PD	3	Path2 I²S Serial Clock/PIP SPI clock
PIP_SPI_EN_WS	L13	B	1.8 / 2.8	BS3-PU	3	Path2 I²S Word Select/PIP SPI enable
PIP_SPI_DATA_SD	K14	B	1.8 / 2.8	BS3-PD	3	Path2 I²S Serial Data/PIP SPI data
I²C Interface (6 Pin)						
SI2C_RF_SCL	M14	B	2.8	BS3-OD-PUC		Path1,2 I²C interface serial clock
SI2C_RF_SDA	M13	B	2.8	BS3-OD-PUC		Path1,2 I²C interface serial data
Path1_SI2C_RF_AS0	F14	I	2.8	IS-PD		Path1 I²C interface slave address 0
Path1_SI2C_RF_AS1	E14	I	2.8	IS-PD		Path1 I²C interface slave address 1
Path2_SI2C_RF_AS0	F15	I	2.8	IS-PD		Path2 I²C interface slave address 0
Path2_SI2C_RF_AS1	E15	I	2.8	IS-PD		Path2 I²C interface slave address 1
JTAG Interface (3 Pin)						
TCK	P2	I	2.8	IS-PU		Path1,2 JTAG port for clock
TRSTB	P1	I	2.8	ISL-PU		Path1,2 JTAG port for reset
TMS	N2	I	2.8	IS-PU		Path1,2 JTAG port for mode select
CLK64_PLL (2 Pin)						
Path1_CLK_PLL_FILTER	K16	O		AO		Path1 Clock PLL Filter
Path2_CLK_PLL_FILTER	K15	O		AO		Path2 Clock PLL Filter
RX-ADC External Capacitor (6 Pin)						
Path1_REFTOP	C12	O		AO		Path1 DC reference top
Path1_REFBOT	C11	O		AO		Path1 ADC reference bottom
Path1_CML	C10	O		AO		Path1 ADC common mode level
Path2_REFTOP	B12	O		AO		Path2 ADC reference top
Path2_REFBOT	B11	O		AO		Path2 ADC reference bottom
Path2_CML	B10	O		AO		Path2 ADC common mode level
1.2 Analog RX-ADC Power/Ground (6 Pin)						
VDD12_RXADC_A_I	A14		1.2	P		Path1,2 Rx-ADC power
VDD12_RXADC_A_Q	D11		1.2	P		Path1,2 Rx-ADC power
VDD12_RXADC_D	A13		1.2	P		Path1,2 Rx-ADC power

Pin Name	Ball	Dir[1]	Voltage(V)	Pad Type	Drive(mA)	Description
VSS12_RXADC_A_I	C13		1.2	G		Path1,2 Rx-ADC ground
VSS12_RXADC_A_Q	D10		1.2	G		Path1,2 Rx-ADC ground
VSS12_RXADC_D	B13		1.2	G		Path1,2 Rx-ADC ground
1.2 V Digital Core Power/Ground (8 Pin)						
VDD12	K2		1.2	P		Demodulator 1.2 V core power
VDD12	N7		1.2	P		Demodulator 1.2 V core power
VDD12	H14		1.2	P		Demodulator 1.2 V core power
VDD12	A15		1.2	P		Demodulator 1.2 V core power
VSS12	N8		1.2	G		Demodulator 1.2 V core ground
VSS12	K4		1.2	G		Demodulator 1.2 V core ground
VSS12	H13		1.2	G		Demodulator 1.2 V core ground
VSS12	D12		1.2	G		Demodulator 1.2 V core ground
2.8 V XTAL I/O Power/Ground (2 Pin)						
VDD28_XTAL	G15		2.8	P		Xtal I/O power
VSS28_XTAL	G14		2.8	G		Xtal I/O ground
2.8 V Digital I/O Power/Ground (4 Pin)						
VDD28	K3		2.8	P		Digital I/O power
VDD28	F13		2.8	P		Digital I/O power
VSS28	L4		2.8	G		Digital I/O ground
VSS28	G13		2.8	G		Digital I/O ground
1.8/2.8 V Digital I/O Power/Ground (Dual Mode for Application Processor Interface) (6 Pin)						
VDD18_28_AP_P	N4		1.8 / 2.8	P		Parallel port I/O power
VDD18_28_AP_P	N9		1.8 / 2.8	P		Parallel port I/O power
VDD18_28_AP_S	N13		1.8 / 2.8	P		Serial port I/O power
VSS18_28_AP_P	N5		1.8 / 2.8	G		Parallel port I/O ground
VSS18_28_AP_P	N10		1.8 / 2.8	G		Parallel port I/O ground
VSS18_28_AP_S	N12		1.8 / 2.8	G		Serial port I/O ground
1.2 V Analog CLK_PLL Power/Ground (2 Pin)						
VDD12_CLK_PLL	K13		1.2	P		Clock PLL power
VBB_VSSA_VSSD12 _CLK_PLL	J13		1.2	G		Clock PLL ground
Ground/NA(46 Pin)						
GND	A7					Ground
GND	A8			G		Ground
GND	N6			G		Ground
NC	A1					No Assignment
NC	A10					No Assignment
NC	A11					No Assignment
NC	A12					No Assignment
NC	A16					No Assignment
NC	B2					No Assignment
NC	B5					No Assignment
NC	B14					No Assignment
NC	C1					No Assignment
NC	C4					No Assignment
NC	C14					No Assignment

Pin Name	Ball	Dir[1]	Voltage(V)	Pad Type	Drive(mA)	Description
NC	D3					No Assignment
NC	D5					No Assignment
NC	D14					No Assignment
NC	E3					No Assignment
NC	E16					No Assignment
NC	F16					No Assignment
NC	G3					No Assignment
NC	G16					No Assignment
NC	J3					No Assignment
NC	J14					No Assignment
NC	J15					No Assignment
NC	J16					No Assignment
NC	K1					No Assignment
NC	L3					No Assignment
NC	L15					No Assignment
NC	L16					No Assignment
NC	M15					No Assignment
NC	M16					No Assignment
NC	N3					No Assignment
NC	N15					No Assignment
NC	N16					No Assignment
NC	P14					No Assignment
NC	P15					No Assignment
NC	P16					No Assignment
NC	R1					No Assignment
NC	R15					No Assignment
NC	R16					No Assignment
NC	T1					No Assignment
NC	T8					No Assignment
NC	T11					No Assignment
NC	T15					No Assignment
NC	T16					No Assignment
RF Block (46 Pin)						
Path2_FMRFIN	A4	I	1.2	PRF		Path2 FM RF input
Path1_B3RFIN	A3	I	1.2	PRF		Path1 Band-III RF input
Path2_B3RFIN	A2	I	1.2	PRF		Path2 Band-III RF input
Path1_B3S	B4	IO	1.2	PRF		Path1 Band-III LNA source
Path2_B3S	B3	IO	1.2	PRF		Path2 Band-III LNA source
Path1_RBIAS	A6	IO	1.2	PA		Path1 Bias resistor
Path2_RBIAS	B6	IO	1.2	PA		Path2 Bias resistor
Path1_B3LNAOUT	C3	O	1.2	PRF		Path1 Band-III LNA output
Path2_B3LNAOUT	C2	O	1.2	PRF		Path2 Band-III LNA output
Path1_B3PGAIN	D1	I	1.2	PRF		Path1 Band-III PGA input
Path2_B3PGAIN	D2	I	1.2	PRF		Path2 Band-III PGA input
Path1_RFIND	E1	IO	1.2	PRF		Path1 RF inductor
Path2_RFIND	E2	IO	1.2	PRF		Path2 RF inductor

Pin Name	Ball	Dir[1]	Voltage(V)	Pad Type	Drive(mA)	Description
Path1_RFGCAP	G1	IO	1.2	PA		Path1 Regulator bypass capacitor
Path2_RFGCAP	G2	IO	1.2	PA		Path2 Regulator bypass capacitor
Path1_LFO	J1	IO	1.2	PA		Path1 Loop filter
Path2_LFO	J2	IO	1.2	PA		Path2 Loop filter
Path1_RFRSSI	E4	O	1.2	PA		Path1 RFRSSI test point
Path2_RFRSSI	D4	O	1.2	PA		Path2 RFRSSI test point
Path1_BBAGC	C6	I	1.2	PA		Path1 Baseband AGC input
Path2_BBAGC	D6	I	1.2	PA		Path2 Baseband AGC input
BBIPTP	D8	IO	1.2	PA		Path1 or Path2 Baseband IP test point
BBINTP	D7	IO	1.2	PA		Path1 or Path2 Baseband IN test point
BBQPTP	C7	IO	1.2	PA		Path1 or Path2 Baseband QP test point
BBQNTP	B7	IO	1.2	PA		Path1 or Path2 Baseband QN test point
VDD12RF1	B1	P	1.2	P		Path1,2 Power supply for RF
VDD12RF2	G4	P	1.2	P		Path1,2 Power supply for RF
VDD12VCO	F3	P	1.2	P		Path1,2 Power supply for VCO
VDD12PLL	H2	P	1.2	P		Path1,2 Power supply for PLL
VDD12BB	A5	P	1.2	P		Path1,2 Power supply for analog baseband
VDD12CP	H3	P	1.2	P		Path1,2 Power supply for charge pump
VDD12DIG	C8	P	1.2	PA		Path1,2 Power supply for digital
VDD12FUSE	D9	P	1.2	P		Path1,2 Power supply for fuse
RFGND1	H1	G	1.2	G		Ground
RFGND2	F2	G	1.2	G		Ground
RFGND3	F1	G	1.2	G		Ground
RFGND4	F4	G	1.2	G		Ground
RFGND5	C5	G	1.2	G		Ground
RFGND6	B8	G	1.2	G		Ground
GNDISOA1	H4	G	1.2	G		Ground
GNDIOA2	B9	G	1.2	G		Ground
GNDISOD1	J4	G	1.2	G		Ground
GNDISOD2	A9	G	1.2	G		Ground

[1] P = power, G = ground, I = input, O = output, B = bi-direction, D = dual voltage, ZO = tri-state output, AI = analog input, AO = analog output, PU = pull-up, PD = pull-down, S = Schmitt trigger, FS = fail safe IO, OD = open drain, KP = contains busholder, SI = TCXO input, XA = Xtal.

THEORY OF OPERATION

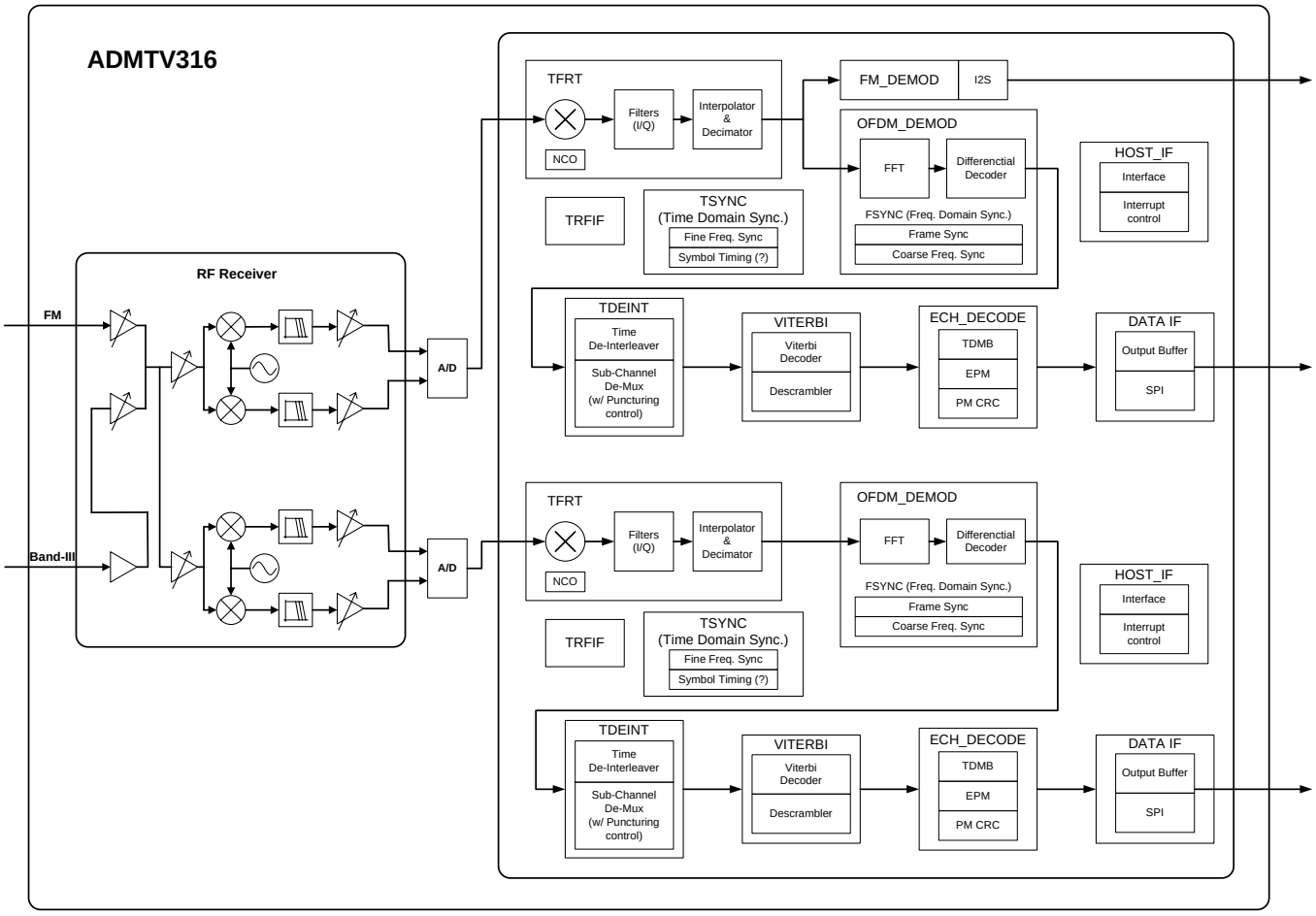


Figure 4. ADMTV316 Block Diagram

RF LNA, PGA AND DOWN-CONVERTER

RF LNA, PGA (Programmable Gain Amplifier) and down-converter amplify coming RF signals and down-convert to zero-IF frequency. LNA has 3-gain modes, which are high, mid and low gain with gain step of 20 dB. LNA gain state can be read from LNAGAIN register (0: low gain, 1, 2: mid gain, 3: high gain). RFPGA has around 30 dB gain dynamic range. RFPGA gain is controlled by digital gain code, which can be read from RFAGC<6:0> register. RFPGA gain is from 0×00 (minimum gain) to 0×7f (maximum gain). Gain step is around 0.7 dB. Zero-IF down conversion mixer down-converts signal from RFPGA's output.

LOCAL OSCILLATOR

ADMTV316 includes an on-chip VCO, which eliminates external LC tank. The VCO uses only 1.2 V. The internal VCO covers whole Band-III and FM, which are 174 ~ 245 MHz and 88 ~ 108 MHz, respectively. Along with fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of video signals.

PLL

ADMTV316 frequency synthesizer consists of a sigma-delta fractional-N PLL and a VCO.

The synthesizer uses fractional-N type architecture with high performance 20bits sigma-delta modulator to get a high resolution and the fast switching time as well as a good phase noise. The charge pump is programmed by 6-bit digital control and its current range is from 20 μA to 1280 μA. Charge pump current can be adjusted by loop filter voltage and VCO range.

Unlike the integer-N type synthesizer used in other silicon tuners, sigma-delta modulated frequency synthesizer provides: 1. Fast switching time, 2. Ultra high frequency resolution, 3. Good phase noise due to its wide bandwidth. The switching

time is less than 30 μsec for the worst case of power up sequence. Using 16.384 MHz oscillator, 20-bit sigma-delta modulated fractional-N phase locked loop exhibits very fine frequency resolution of 16 Hz. It can compensate the frequency offset induced by error ratio and temperature drift, etc. of the reference crystal. The LO frequency, f_{LO}, is calculated as following equation,

LO frequency = {Clock frequency × (PLLN+PLLF÷2^{20})} ÷ PLLS

where PLLN is N-counter divide value, PLLF is the fractional value and PLLS is divide ratio (PLLS = 4). Refer to I²C Table.

BB LPF AND PGA

The baseband block contains LPF and PGA. The RF signal goes down to zero-IF through RF zero-IF down-converter. The baseband LPF selects the wanted signal in the output of down-converter. The cut-off frequency of LPF is about 768 kHz for T-DMB and 225 kHz for FM. To compensate the variation of cutoff frequency in the LPF, the automatic cutoff-tuning circuit is included and this circuit guarantees the cut-off frequency accuracy.

The baseband PGA controls the input level of ADC in demodulator. Gain of baseband PGA is controlled by 8-bit gain control register. The PGA gain setting can be read from GVBB register. The GVBB<7:0> ranges from 0×00 to 0×c3. Digital gain step is around 0.25 dB. Baseband PGA gain setting can be programmable by I²C GVBBI2C<7:0> register for ADMTV316 test mode. There are 3 modes for baseband gain setting according to EXTGVBB<1:0> register setting as:

RF internal AGC using analog baseband RSSI

- Manual gain setting using GVBBI2C
- Gain setting from demodulator's AGC digital code.

AUTOMATIC GAIN CONTROL

In ADMTV316, there are 2 AGC loops, which are RFAGC and BBAGC. LNA has 3-step gain control, and gain difference is 20 dB. RFPGA has around 30 dB gain dynamic range, and controlled by RFAGC<6:0> register. The register value is from 0×00 (minimum gain) to 0×7f (maximum gain). RFAGC consists of these 2 blocks. RFAGC dynamic range is around 70 dB.

BBAGC has programmable gain amplifier with gain step of 0.25 dB. The BB gain is determined by digital gain setting of GVBB<7:0> register. The register value is from 0×00 (minimum gain) to 0×c3 (maximum gain). BBAGC dynamic range is around 48 dB. With these two dynamic ranges (RF 70 dB, IF 48 dB), dynamic range of ADMTV316 is larger than 100 dB.

Recommended output amplitude of ADMTV316 is from 300 mVpp to 700 mVpp at each OUT and OUTB pin.

THREE POWER DOWN MODES

ADMTV316 has three power down modes, which are hardware power down (PD pin), time-slicing power down (TSPD pin), and software power down (register setting).

Recovery time from power down depends on the PLL lock time and the demodulator's AGC response.

1. If PD pin is high, then all blocks including crystal oscillator are powered down.
2. If TSPD pin is high and TSPDxxx block register is high, then xxxBlock is powered down.
3. If SWPDxxx block register is high, then xxxBlock is powered down.

4. Power down and on timing.
In case of hardware PD and TSPD, all blocks including the crystal oscillator block are powered down. So, all digital parameters are stored as just before powered down. After powered on by PD or TSPD pin, the tuner does not need to operate the VCO searching loop and the automatic gain control. So the power-on delay time is about 250 µs. However, after the SWPD ON the tuner needs to operate the VCO searching loop and automatic gain control because the digital block is alive during the SWPD. So the software power on delay time of around 12 ms is relatively longer than PD or TSPD. See figure 20 ~ 22.

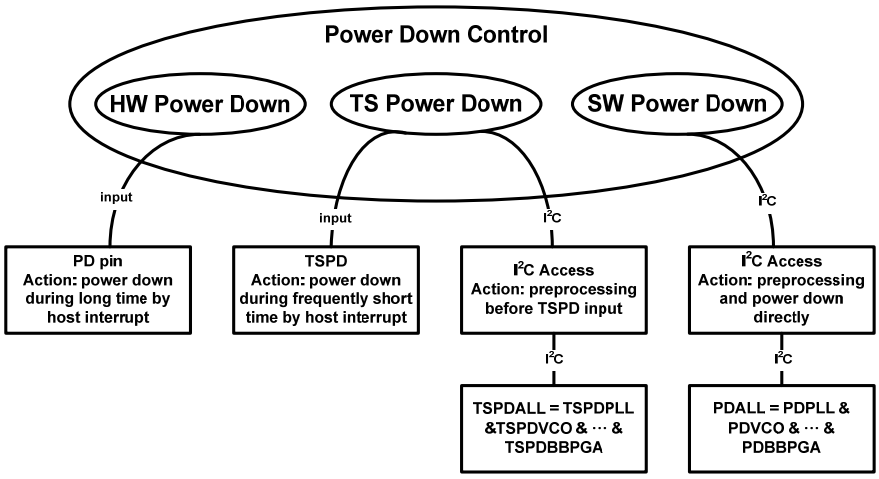


Figure 5. Three Power Down Modes

SYSTEM INTERFACE

DATA INTERFACE

[Base Address: ADMTV316 Base + 0×180]

DATA_IF is an interface for sending the data decoded in modem to AP (Application Processor). It supports parallel interface and serial interface modes. One of these two modes must be chosen according to AP type and interface implementation method. The main features for each interface are as follows.

- Parallel Interface
  - SRAM interface with interrupt function
  - FIC, CIF channel buffer with individual interrupt
- Serial interface
  - Master/Slave mode SPI

    Motorola SPI-compatible interface

    Texas Instruments synchronous serial interface
  - Supports buffered SPI re-transmission function for PiP mode.
  - Transmission speed

    Master Mode: Baud rate = 49.152 MHz ÷ {2 × (1 + SCR)}

    Slave Mode: Baud rate up to 24 MHz
  - 188/192 byte packet size selectable
  - Flow control using demand signal in Master mode

Data Format

Data is identified from the header in one packet (188 byte) data in case of serial data.

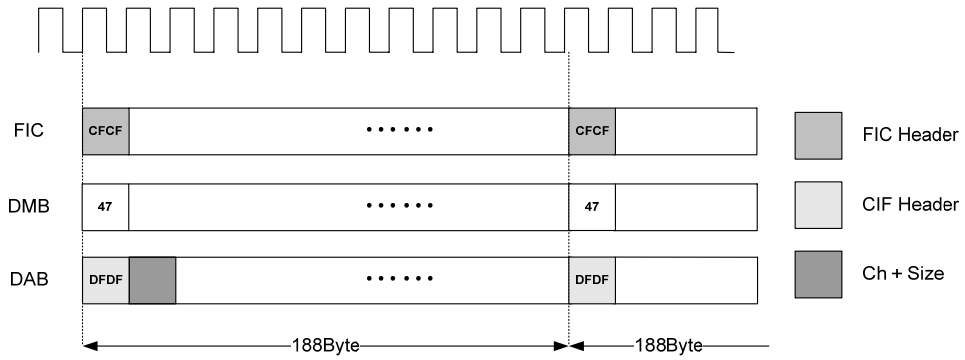


Figure 6. Serial Data Format

Data format in Parallel/Serial Interface is shown in figure 7.

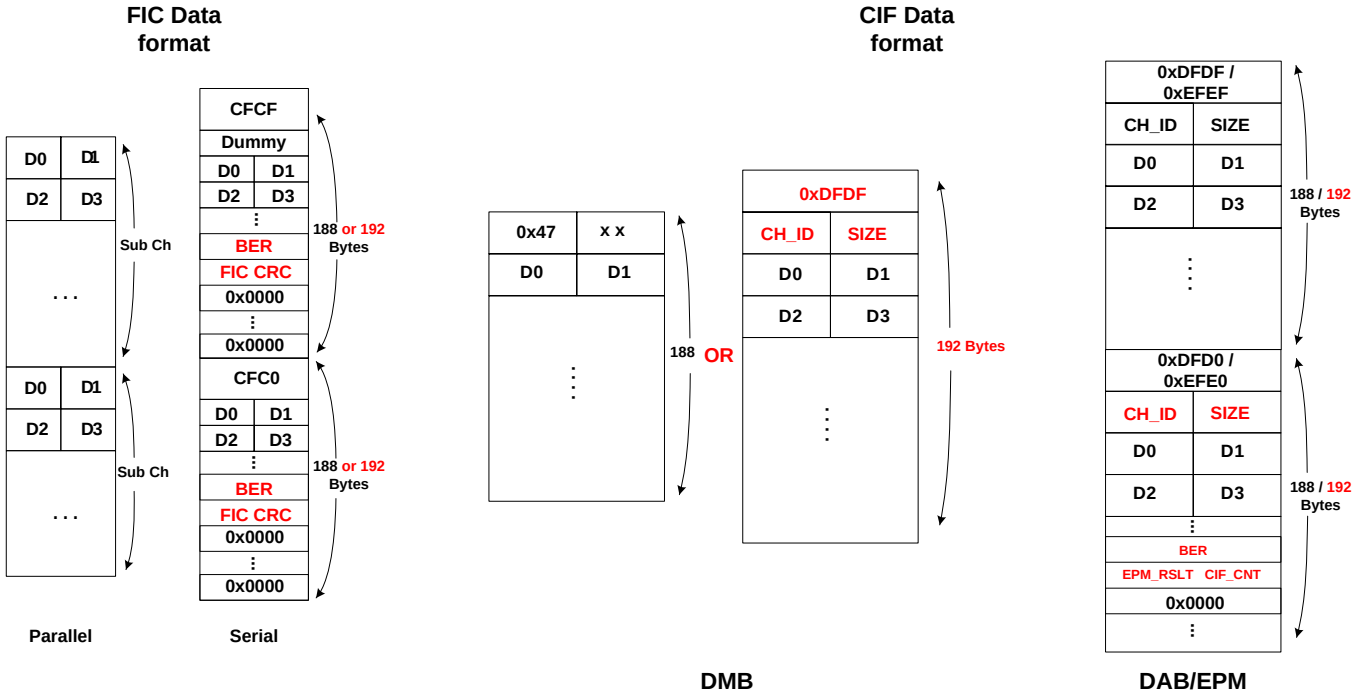


Figure 7. Serial/ Parallel Interface Data Buffer Formatting

1. CIF data in Parallel interface

DF'DF'08'3C'FF'FC'94'44'
34'75'66'44'43'44'31'21'11'12'49'24'00'00'00'A8'
BA'1C'C7'80'00'00'10'03'0C'41'04'CF'45'54'96'55'
85'D5'61'57'DA'7D'A6'D9'5D'85'D8'76'07'5F'71'C6'
DD'81'D7'E0'79'F7'9F'72'07'DC'8E'58'24'96'19'63'
7E'58'A0'AA'79'2A'9E'49'A7'8E'78'E8'9A'2A'67'8A'
BA'67'AE'89'F5'51'41'9A'61'A7'3E'07'B2'A3'15'44'
B1'B4'91'00'E0'99'AE'6C'5E'65'9D'45'72'7B'34'55'
79'1B'B6'43'8B'9A'29'23'44'20'E5'58'13'C5'5A'0D'
33'B1'62'36'E2'68'77'11'3B'5D'91'37'3D'ED'8C'2C'
33'6D'A8'76'A0'5C'C6'DD'B4'D4'94'A4'5A'A4'AD'C5'
3A'EF'85'99'44'E5'C1'AE'D2'36'88'1A'06'51'4D'08'
60'2A'1C'0F'BC'3E'99'9A'49'1F'84'37'1D'05'33'B4'
CC'D9'C8'74'7E'CD'6B'5B'52'59'AD'D9'21'26'98'4A'
1C'CA'2D'EB'E2'65'AB'09'22'EC'A4'D5'62'3C'69'1D'
5C'D6'E5'F3'2E'6F'96'74'4C'6D'06'ED'74'B2'DE'47'
92'63'99'5F'24'D5'56'8C'0C'5B'76'A8'1D'3D'4E'F9'
92'3D'22'B3'59'87'2D'37'38'B1'C4'A6'6B'06'36'36'
B5'D4'60'74'46'E7'22'F6'CD'4A'BB'34'87'E9'C0'FE'
68'B2'5A'66'2F'B4'1A'D6'05'45'66'9E'F3'25'56'A9'
40'3E'A0'9B'D8'EE'B4'7D'2C'9C'25'CB'10'96'69'17'

76'13'09'97'36'50'37'BB'57'55'35'57'32'59'38'A9'
1E'B1'A8'26'B6'B9'AD'23'9A'93'9D'A0'1E'EB'0F'88'
B6'89'76'26'CE'78'80'A1'4C'86'5B'85'9C'1A'9E'35'
93'80'00'1C'BB'93'E1'2E'93'D1'7C'50'B7'2C'12'EB'
80'78'A2'2A'7E'8F'11'64'1C'96'BC'72'E4'7D'8A'88'
32'DF'56'0D'C3'ED'2D'8B'BE'A3'CD'5A'21'BE'15'9D'
B3'8A'63'47'32'06'80'E4'8C'14'20'24'50'B7'24'9F'
B6'1A'54'5A'BC'59'D9'6F'AD'8F'C4'8E'B2'64'F0'4A'
03'74'43'2B'11'6A'5E'12'F6'D6'77'56'6A'CB'15'C9'
C1'81'93'00'ED'ED'89'E6'24'B7'21'02'

DF'DF' : CIF identifier

08'3C' : CH_ID + Size[CU] -> MSB 6 bit is a Sub-channel ID and others 10 bit is a data size

0x08 0x3C = 00001000 00111100

Therefore, 000010 (0x02) is a sub-channel ID, 00 00111100(0x3C) is a data size

0x3C[CU] = 0x3C X 8 [byte] = 480 [byte].

The CIF data size is 480[byte] excluding 0xDF, 0xDF, 0x08 and 0x3C.

According to the set MSL of DATA_IF Control Register to MSB_FIRST or LSB_FIRST, byte order is different which read from AP in case of Parallel interface. (Refer to cmc521Endian's function of the API document)

2. TS data in Parallel interface

DF'DF'04'CC'47'41'00'19'00'02'B0'97'00'01'FD'00'
00'E1'14'F0'66'1D'64'11'01'02'60'00'4F'01'0C'23'
41'04'03'2F'00'02'23'00'04'04'16'02'0D'00'00'FF'
00'00'08'00'00'00'08'00'05'07'30'A0'70'14'00'0F'
0F'06'10'00'C6'00'01'5F'90'00'00'00'00'21'00'00'
00'00'03'03'26'00'01'24'00'04'04'0D'02'05'00'00'
FF'00'00'08'00'00'00'08'00'06'10'00'C6'00'01'5F'
90'00'00'00'00'21'00'00'00'00'03'13'E1'11'F0'04'
1E'02'00'02'13'E1'12'F0'04'1E'02'00'01'12'E1'13'
F0'04'1E'02'00'03'12'E1'14'F0'04'1E'02'00'04'5E'
0D'3E'2B'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
DF'DF'04'CC'47'41'11'19'00'04'B0'29'00'00'FD'00'
00'C0'C0'92'00'00'00'A4'DE'DE'E8'8E'E4'DE'EA'E0'
00'13'00'12'E2'09'10'A0'8A'01'79'81'30'2A'01'FF'
00'B3'AF'54'16'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'

DF'DF' : CIF identifier
08'3C' : CH_ID[7:2] + Size[CU]
TS(Video data) is also CIF data, so identifier is 0xDF 0xDF.
CH_ID value is valid, but the size value is not.
MPEG TS data size is 188 byte and Header size is 4 byte, so total data length is 192 byte (4 byte + 188 byte)

3. FIC data in Parallel interface

'05'00'E0'41'24'34'FF'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'01'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'11'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'31'
0D'01'13'48'88'18'04'00'89'74'09'74'89'74'0F'22'
F1'E0'04'15'01'C0'12'F1'E0'04'11'01'58'06'00'71'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'F1'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'01'F1'
60'08'22'F1'E0'
04'12'01'58'0A'06'03'00'40'3C'10'01'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'03'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'07'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'0F'F1'
FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'1F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'3F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'7F'F1'

'FIC buffer full interrupt' occurs per 384 byte as FIC data.
To know FIC CRC value read from FIC_CRC_REG register whenever interrupt occurs.

4.. CIF data in Serial interface

DF'DF'08'3C'FF'FC'94'44'
34'75'66'44'43'44'31'21'11'12'49'24'00'00'00'A8'
BA'1C'C7'80'00'00'10'03'0C'41'04'CF'45'54'96'55'
85'D5'61'57'DA'7D'A6'D9'5D'85'D8'76'07'5F'71'C6'
DD'81'D7'E0'79'F7'9F'72'07'DC'8E'58'24'96'19'63'
7E'58'A0'AA'79'2A'9E'49'A7'8E'78'E8'9A'2A'67'8A'
BA'67'AE'89'F5'51'41'9A'61'A7'3E'07'B2'A3'15'44'
B1'B4'91'00'E0'99'AE'6C'5E'65'9D'45'72'7B'34'55'
79'1B'B6'43'8B'9A'29'23'44'20'E5'58'13'C5'5A'0D'
33'B1'62'36'E2'68'77'11'3B'5D'91'37'3D'ED'8C'2C'
33'6D'A8'76'A0'5C'C6'DD'B4'D4'94'A4'5A'A4'AD'C5'
3A'EF'85'99'44'E5'C1'AE'D2'36'88'1A'06'51'4D'08'
60'2A'1C'0F'
DF'D0'08'3C'BC'3E'99'9A'49'1F'84'37'1D'05'33'B4'
CC'D9'C8'74'7E'CD'6B'5B'52'59'AD'D9'21'26'98'4A'
1C'CA'2D'EB'E2'65'AB'09'22'EC'A4'D5'62'3C'69'1D'
5C'D6'E5'F3'2E'6F'96'74'4C'6D'06'ED'74'B2'DE'47'
92'63'99'5F'24'D5'56'8C'0C'5B'76'A8'1D'3D'4E'F9'
92'3D'22'B3'59'87'2D'37'38'B1'C4'A6'6B'06'36'36'
B5'D4'60'74'46'E7'22'F6'CD'4A'BB'34'87'E9'C0'FE'
68'B2'5A'66'2F'B4'1A'D6'05'45'66'9E'F3'25'56'A9'
40'3E'A0'9B'D8'EE'B4'7D'2C'9C'25'CB'10'96'69'17'
76'13'09'97'36'50'37'BB'57'55'35'57'32'59'38'A9'
1E'B1'A8'26'B6'B9'AD'23'9A'93'9D'A0'1E'EB'0F'88'
B6'89'76'26'CE'78'80'A1'4C'86'5B'85'
DF'D0'08'3C'9C'1A'9E'35'
93'80'00'1C'BB'93'E1'2E'93'D1'7C'50'B7'2C'12'EB'
80'78'A2'2A'7E'8F'11'64'1C'96'BC'72'E4'7D'8A'88'
32'DF'56'0D'C3'ED'2D'8B'BE'A3'CD'5A'21'BE'15'9D'
B3'8A'63'47'32'06'80'E4'8C'14'20'24'50'B7'24'9F'
B6'1A'54'5A'BC'59'D9'6F'AD'8F'C4'8E'B2'64'F0'4A'
03'74'43'2B'11'6A'5E'12'F6'D6'77'56'6A'CB'15'C9'
C1'81'93'00'ED'ED'89'E6'24'B7'21'02'*00'f3'0f'c8'* -> (0x00<<8|0xf3):BER (0x0F<<8|0xc8):EPM_RSLT CIF_CNT (last 4 byte)
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00' -> The rest is filled with Zero.
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

```
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'
```

All data is transferred by per188byte in case of Serial Interface. Except Video channel, CIF identifier of the first 188 byte in all CIF data is 0xDF 0xDF, and after that CIF identifier is 0xDF, 0xD0 until get to 0xDF 0xDF.

5. TS(Video)data in Serial interface

```
47'41'00'19'00'02'B0'97'00'01'FD'00'
00'E1'14'F0'66'1D'64'11'01'02'60'00'4F'01'0C'23'
41'04'03'2F'00'02'23'00'04'04'16'02'0D'00'00'FF'
00'00'08'00'00'00'08'00'05'07'30'A0'70'14'00'0F'
0F'06'10'00'C6'00'01'5F'90'00'00'00'00'21'00'00'
00'00'03'03'26'00'01'24'00'04'04'0D'02'05'00'00'
FF'00'00'08'00'00'00'08'00'06'10'00'C6'00'01'5F'
90'00'00'00'00'21'00'00'00'00'03'13'E1'11'F0'04'
1E'02'00'02'13'E1'12'F0'04'1E'02'00'01'12'E1'13'
F0'04'1E'02'00'03'12'E1'14'F0'04'1E'02'00'04'5E'
0D'3E'2B'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
47'41'11'19'00'04'B0'29'00'00'FD'00'
00'C0'C0'92'00'00'00'A4'DE'DE'E8'8E'E4'DE'EA'E0'
00'13'00'12'E2'09'10'A0'8A'01'79'81'30'2A'01'FF'
00'B3'AF'54'16'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'FF'
```

Transfer as a MPEG2 packet type.

6. FIC data in Serial interface

CF'CF'00'60'05'00'E0'41'24'34'FF'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'01'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'11'FF'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'31'00'64'0F'FF'00'00'00'00'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
CF'CF'04'60'
0D'01'13'48'88'18'04'00'89'74'09'74'89'74'0F'22'
F1'E0'04'15'01'C0'12'F1'E0'04'11'01'58'06'00'71'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'F1'
FF'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'01'F1'
00'5D'0F'FF'00'00'00'00'00'00'00'00'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
CF'CF'08'60'08'22'F1'E0'
04'12'01'58'0A'06'03'00'40'3C'10'01'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'03'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'07'F1'FF'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'0F'F1'00'73'0F'FF' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'
CF'CF'0C'60'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'1F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'3F'F1'FF'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'7F'F1'00'9E'0F'FF'00'00'00'00' -> (0x00<<8|0x64):BER (0x0F<<8|0xFF):BAND3 CRC
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'
00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'00'

CF'CF' : FIC data Identifier
0C'60' : continuous count + data length
Continuous count of FIC data increase in order 0x00, 0x04, 0x08 and 0x0C.
The 0x60 indicates a length of FIC data (96byte). FIC data is transferred by per 188byte include a part of FIB data.

Two FIC parsing method
(1)Available parsing per 96 byte whenever receiving FIC data.,
(2)Available execute parsing 384byte at one time after received in order 0x00, 0x04, 0x08 and 0x0C(continuous count).

TAIL_ON of DIF_CTL register set to '1' then FIC stream data(188byte) include BER and CRC. BER is combination of 101st , 102nd data, and CRC values is combination of 103rd , 104th data.
If CRC value is 0xFFF, it means FIC stream data is valid in Band III.
When TAIL_ON of DIF_CTL register set to '1', do not calculate CRC check in FIB parsing because CRC value change in to CRC result value by ADMTV316.
IF you want to calculate the value of the software, have to TAIL_ON of DIF_CTL register reset to '0'.

SPI (Serial Peripheral Interface)

1. Motorola SPI

Motorola SPI is designed to control clock polarity and clock phase, define MSB byte and transfer sequence. Figure 9 and 10 show individual waveform. Each setting mode can be controlled with register.

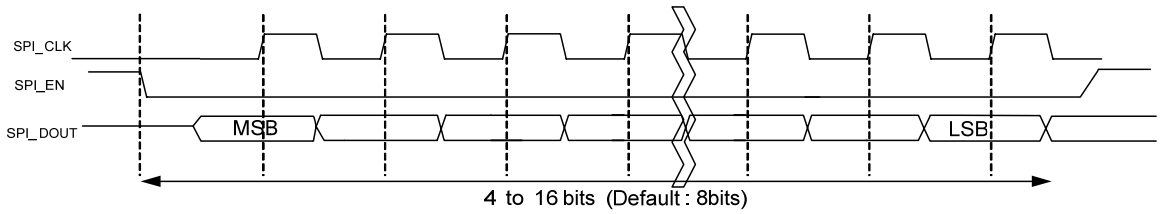


Figure 8. SPH=0 Waveform

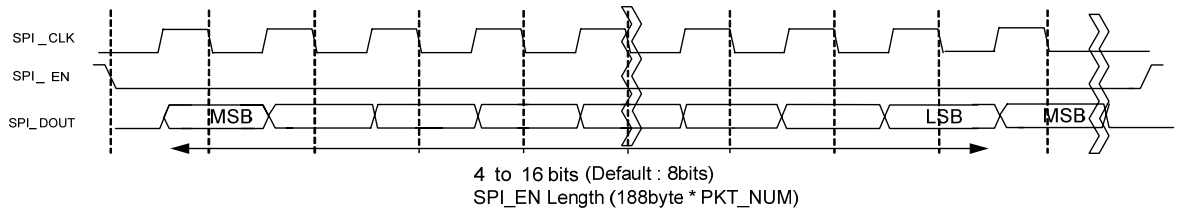


Figure 9. SPH=1 Waveform

2. Texas Instruments SSF

Texas Instruments SSF (Synchronous Serial Frame) supports large part of TI AP format. It uses the same signaling for clock polarity, clock phase and MSB/LSB first control as those of Motorola SPI, but different signaling for EN.

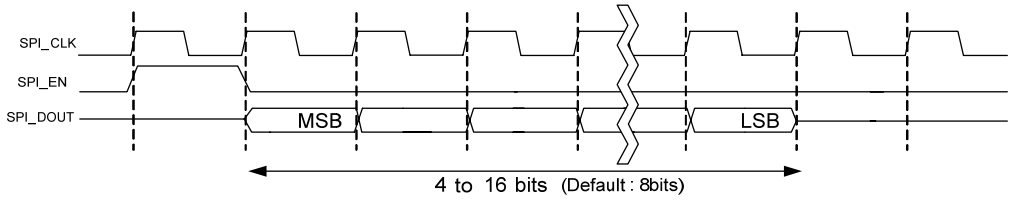


Figure 10. Single Transfer

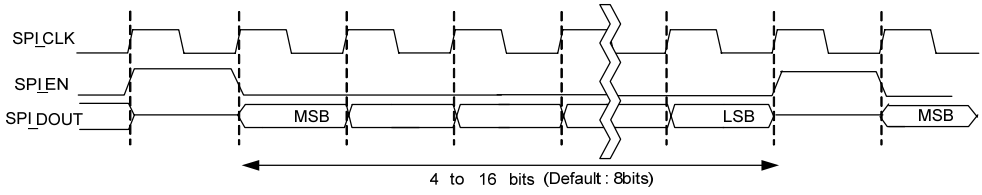


Figure 11. Continuous Transfer

3. Configuration SPI Mode

(1) Demand Mode

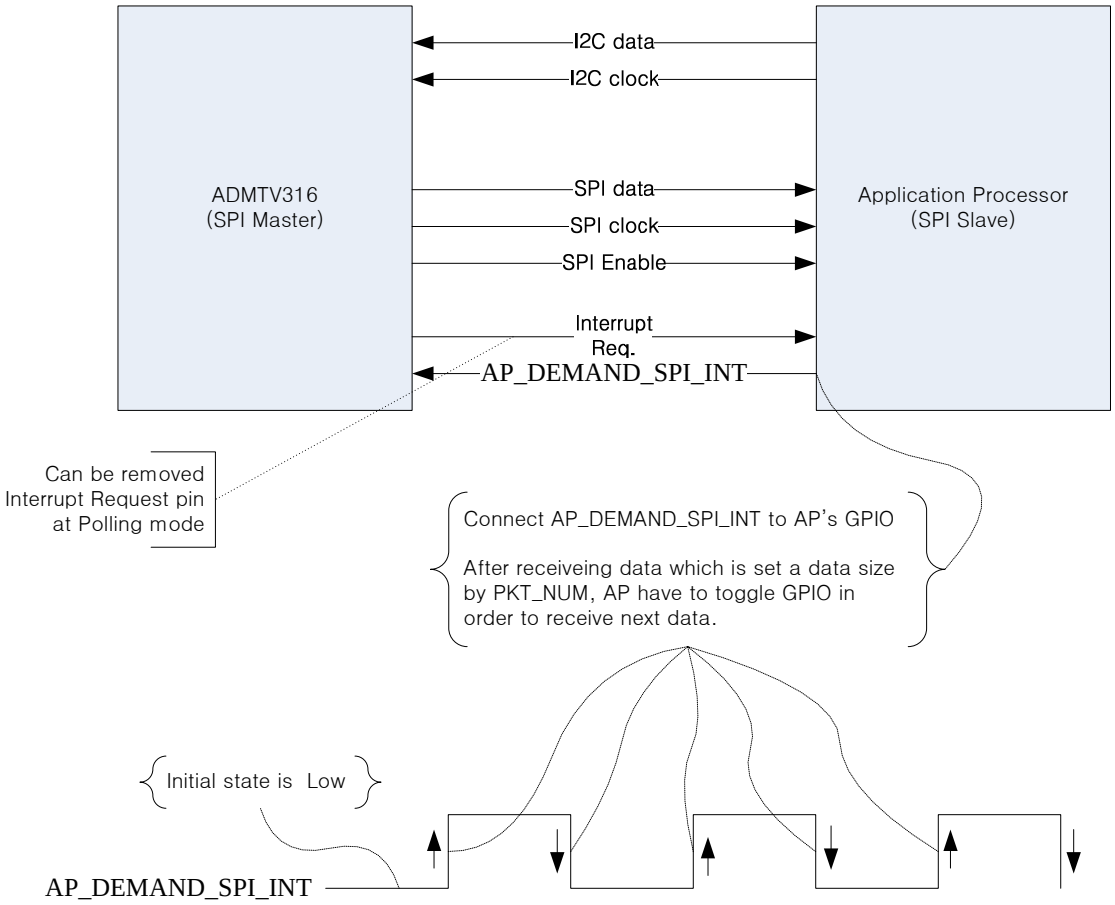


Figure 13. SPI_Demand mode

AP operates as a SPI slave at SPI Demand mode.

Whenever AP delivers AP's status to ADMTV316 through AP_DEMAND_SPI_INT toggle, then ADMTV316 transmit data. Refer to Figure 13. AP will be assign GPIO pin in order to AP_DEMAND_SPI_INT and its pin set to initial Low.

Need to set Register for Demand mode.

A. Set DEMADN_MODE to '1'
B. Set REG_DEMADN_ON to '0' (Set REG_DEMADN_ON to '1' in PIP mode)
C. GPIO pin of AP, which connected AP_DEMADN_SPI_INT, set 'L' from initial state.

(2) Slave Mode

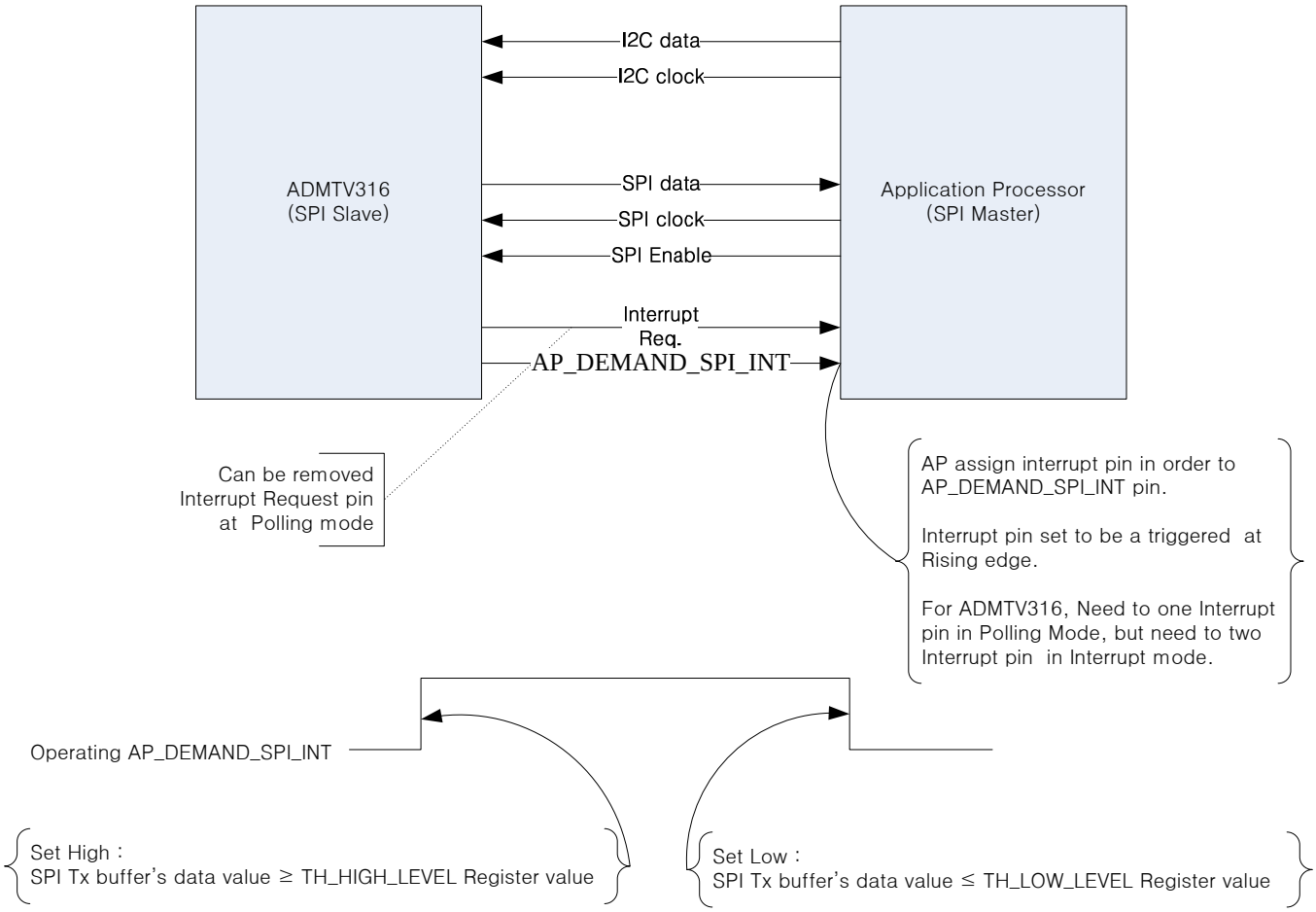


Figure 14. SPI_Slave mode

AP_DEMAND_SPI_INT change to high when Tx buffer's data value becomes above TH_HIGH_LEVEL Register value, and change to low when Tx buffer's data value becomes below TH_LOW_LEVEL Register value. After receiving data as same as TH_HIGH_LEVEL register values, then AP stops SPI Clock signal to ADMTV316.

AP_DEMAND_SPI_INT connect to AP's External Interrupt pin, and Interrupt pin set to be a triggered at rising edge.

PKT_NUM register is set to '0' in Slave Mode. It doesn't support PIP(Pitcher In Pitcher) in Slave mode.

(3) Master Mode

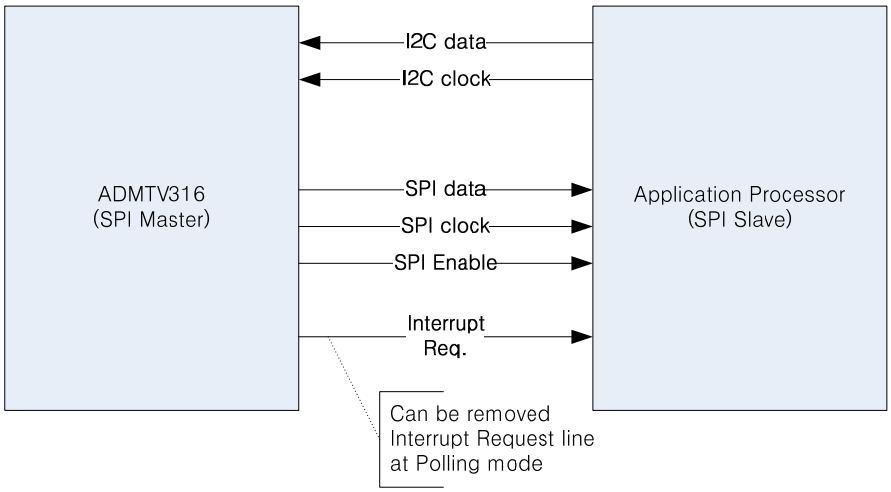


Figure 15. SPI_Master mode

SPI data transmit repeatedly as same as PKT_NUM register values, and has interval as same as PCK_INTV register value.

PCK_INTV register setting need to have a time for received data processing time in AP.

PiP (Picture in Picture)

PiP operation is implemented through single channel by using time dividing format of signal coming from demodulators. In this case, each demodulator is identified from header information pre-defined by S/W setting.

Sequence of PiP operation

In order to operate demodulator without data loss, the following sequence is mandatory.

1. PiP master On(PiP master setting sequence when operated in PiP mode)
   (1) DATA_IF_CR – Serial mode selection
   (2) SIF_CR – PiP master, Reg_demand, PiP_mode, Demand_mode, Half_mode, SPI_on
   (3) REG_DEMAND – ON
   (4) SPI_CR
   (5) SPI_PAD_CTRL – SPI_PAD_CTRL_EN, SPI_PAD_OEn (1'b0)
   (6) SIF_ON
2. PiP slave On (SPI operating sequence when operated in PiP Slave mode)
   (1) DATA_IF_CR
   (2) SIF_CR - PiP slave, PiP_mode, Demand_mode, Half_mode, SPI_on
   (3) PIP_STATE Read - update check
   (4) SPI_CR
   (5) SPI_PAD_CTRL
   (6) SIF_ON
3. PiP slave Off (a slave off sequence in PiP mode for operating one channel in PiP mode)
   (1) SIF_OFF

(2) SIF_CR – PiP OFF

(3) PIP_STATE Read – update check

(4) DATA_IF_CR – Serial mode off

(5) SW_RESET

Power-down Sequence in PIP mode

1. PiP OFF
2. Check PIP OFF register update
3. SW_ RESET
4. Power_ OFF

NOTES: Channel off in PIP mode without power down can be executed regardless of operating sequence and manual control.

Parallel I/F

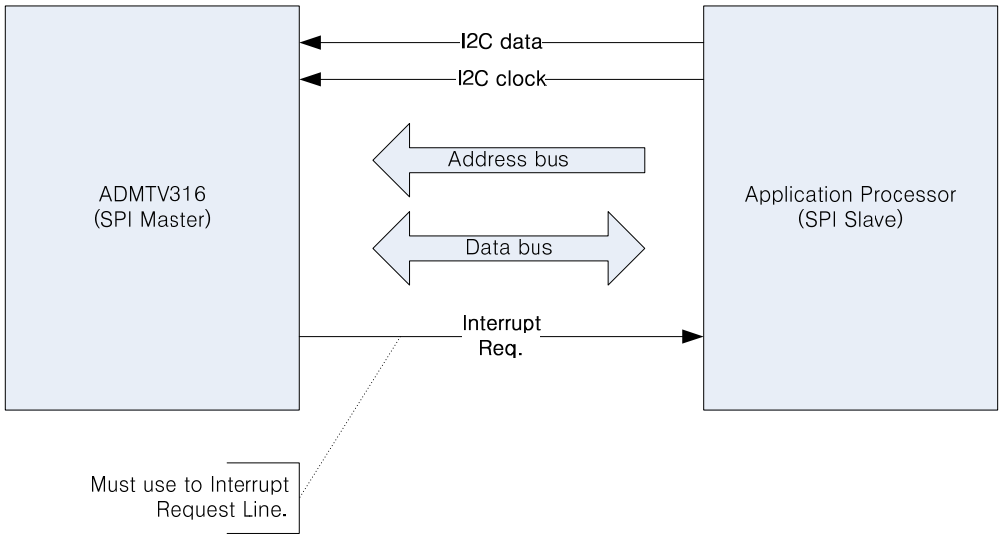


Figure 16. Parallel I/F

In case of Parallel Interface, it uses I2C to access to register Read/Write of RF block.

When CIF/FIC buffer is full with CIF/FIC data, CIF/FIC interrupt occurs via interrupt line and then AP reads data from FIC_MEM_READ and CIF_MEM_READ register as same as size set in CIF_TOTAL_CNT and FIC_TOTAL_CNT register

There are three method of CIF Buffer Interrupt : 'CIF buffer full interrupt' has occurred by DIF_INT_SRC_SEL bit of the DATA_IF Control register.

1. The buffer data of ADMTV316 has become above value of TH_HIGH_LEVEL register.
2. Gather one data packet of Sub-channel.
3. Use to both of 1,2 ways.

Register Description of Base-Band Part [Base address : ADMTV316 Base + 0x180]

Address [6:0]	Type	Name	Description	Default Value
			SW_RESET Register	
0x00 [0]	W	**SW_RESET**	OUT_BUF / SIF Block Software Reset	-
			DATA_IF Control Register	
0x02 [11]	R/W	**FIC/CIF_OFF_SYNC_UPDATE**	Updated FIC/CIF OFF by iCH_CHG 0 : Real time update register 1 : use Syncupdate	0x0
0x02 [10]	R/W	**SERL_PARL_SEL**	OUT_BUF / SIF block Clock Enable Signal. 0 : OUT_BUF Operating Clock Enable 1 : SIF Block Clock Enable	0x0
0x02 [9:8]	R/W	**INT_SRC_SEL**	Interrupt Source Select 0 : 'Ch change' has became a 'Int src' by TDEINT. 1 : When it was a above data of High Threshold level, 'Sub Channel End' has became a 'Int src'. 2 : Use to all interrupt source	0x0
0x02 [7]	R/W	**TAIL_ON**	TAIL information 0 : Output only data information 1 : Output BER, CRC, CIF Counter etc…	0x0
0x02 [6]	R/W	**FM_DMB_SEL**	Input Source select 0 : Input select through DMB_DEC 1 : Input select through FM_DEMOD	0x0
0x02 [5]	R/W	**MLS16**	Switch MSB 16bit and LSB 16bit 0 : MSB(16bit) First, LSB(16bit) Last 1 : LSB First, MSB Last	0x0
0x02 [4]	R/W	**MLS**	Switch MSB 8bit and LSB 8bit 0 : MSB(8bit) First, LSB(8bit) Last 1 : LSB First, MSB Last	0x0
0x02 [3:2]	R/W	**FIC MODE**	FIC Size Setting 00 : 384 byte 01 : 96 byte 10 : 128 byte 11 : 192 byte	0x00
0x02 [1]	R/W	**FIC_OFF**	NOT Transfer FIC Data 0 : Transfer FIC Data 1 : Not transfer FIC Data	0x1
0x02 [0]	R/W	**CIF_OFF**	NOT Transfer CIF Data 0 : Transfer CIF Data 1 : Not transfer CIF Data	0x0
			DATA_HEADER	
0x04[15:0]	R/W	**FIC_HEADER**	DATA_IF FIC Header Register	0xCFCF
0x06[15:0]	R/W	**DMB_HEADER**	DATA_IF DMB Header Register	0xDFDF
0x08[15:0]	R/W	**DAB_HEADER**	DATA_IF DAB Header Register	0xDFDF
0x0A[15:0]	R/W	**EPM_HEADER**	DATA_IF EPM Header Register	0xEFEF
			THRESHOLD LEVEL	
0x0C [15:0]	R/W	**TH_HIGH_LEVEL**	Serial I/F : High Threshold level of the SPI INT signal Parallel I/F : above Level, Occurs Interrupt by Sub Channel end Signal	0x758
0x0E [15:0]	R/W	**TH_LOW_LEVEL**	Low Threshold level of the SPI INT signal	0x3AC
			PIF DATA READ	

0x10 [15:0]	R	**FIC_MEM_READ**	Read to FIC Data from DATA_IF_RAM0	0x0000
0x12 [15:0]	R	**CIF_MEM_READ**	Ready to CIF data from DATA_IF_RAM1	0x0000
			DATA Counter Register	
0x14 [12:0]	R	**CIF_TOTAL_CNT**	Total Data Packet from CIF Buffer(per 2byte) 16bit access read CIF_TOTAL_CNT	0x0000
0x16 [12:0]	R	**CIF_DMB0_CNT**	Total DMB0 Data Packet from CIF Buffer	0x0000
0x18 [12:0]	R	**CIF_DMB1_CNT**	Total DMB1 Data Packet from CIF Buffer	0x0000
0x1A [12:0]	R	**CIF_DMB2_CNT**	Total DMB2 Data Packet from CIF Buffer	0x0000
0x1C [12:0]	R	**CIF_DMB3_CNT**	Total DMB3 Data Packet from CIF Buffer	0x0000
0x1E [12:0]	R	**FIC_TOTAL_CNT**	Total FIC Data from FIC Buffer (per byte) 16bit access read FIC_TOTAL_CNT/2	0x0000
			SIF_ON Register	
0x20 [0]	R/W	**SIF_ON**	SIF Block On/Off Select 0 : SIF OFF Mode 1 : SIF ON	0x0
			SIF Control Register (Default : 16'h00A0)	
0x22 [15:12]	R/W	**RESERVED**	-	0x00
0x22 [11]	R/W	**PiP_MASTER**	PiP REQ signal generation 0 : PiP Slave 1 : PiP Master	0x0
0x22 [10]	R/W	**DEMAND_MODE_SYNC_UPDATE**	Updated DEMAND mode via PKT_END 0 : real time updated register 1 : use Sync-update	0x0
0x22 [9]	R/W	**HEADER_AND_OFF**	Change continuously Header ID 0 : Change Header ID ex) first header ID 0xDF 0xDF, next header ID 0xDF 0xD0 1 : No change Header ID ex) first header ID 0xDF 0xDF, next header ID 0xDF 0xDF	0x0
0x22 [8]	R/W	**REG_DEMAND_ON**	Used Register Demand 0 : Useless 1 : Available control Demod via Register	0x0
0x22 [7]	R/W	**PIP_MODE**	PIP MODE 0 : Not PIP 1 : PIP	0x0
0x22 [6]	R/W	**MS**	Select Master / Slave Mode of SPI 0 : Master 1 : Slave	0x0
0x22 [5]	R/W	**SPI_STB_POL**	Determine the polarity of Strobe(enable) signal of SPI 0 : Active low 1 : Active high	0x0
0x22 [4]	R/W	**DEMAND_MODE**	Demand Input Use or Not 0 : Packet data transfer without Demand 1 : Demand Mode, Transfer start via Demand Signal	0x0
0x22 [3]	R/W	**RESYNC_ON**	Automatically synchronize at RESYNC 0 : Reported without Sync 1 : Synchronizing after RESYNC	0x0
0x22 [2]	R/W	**SPI_HOLD**	Occurs to Data Hold request to set 0 : SPI Go on 1 : SPI Stop and Data Hold	0x0
0x22 [1]	R/W	**HALF_MODE**	Select Transfer Data Size 0 : Data transfer per 16 bit 1 : Data transfer per 8 bit(16bit divide 2) (DSS have to set 8bit)	0x1
0x22 [0]	R/W	**SPI_ON**	FIC Header Insert On/Off 0 : Parallel to Serial Transfer Block Off 1 : Parallel to Serial Transfer	0x1

			SIF Packet Control Register (Default : 16'h0107)	
0x24 [4]	R/W	**TS_PKT**	Transfer per MPEG-TS Packet 0 : Transfer per 192 byte 1 : Transfer per 188 byte	0x01
0x24 [3:0]	R/W	**PKT_NUM**	Set Packet Size When Packetizing 0 : Immediate transfer without Packetinzing 1 ~ 15 : transfer per 1~15 tie	0x0A
			SIF Packet Interval Register (Default : 16'h0107)	
0x26 [15:0]	R/W	**PCK_INTV**	Serial Packet transfer the case of the minimum spacing between Packet (= PCK_INTV * 1/ Baud rate)	0x0400
			SPICR Register (Default : 16'h0107)	
0x28 [15:8]	R/W	**SCR**	Serial clock rate. The SCR is used to generate the transmission and receive bit rate. Baud rate = F(CLK) / 2*(1+SCR) default Baud rate = 24.576 / 4 = 6.144 MHz	0x01
0x28 [7]	R/W	**SPH**	SSPCLKOUT phase control 0 : no clock shift with data 1 : half clock shift with data	0x0
0x28 [6]	R/W	**SPO**	SSPCLKOUT polarity control 0 : first edge – rising 1 : first edge - falling	0x0
0x28 [5:4]	R/W	**FRF**	Frame format select 00 : Motorola SPI 01 : TI SSF 10 : Reserved 11 : Reserved	0x0
0x28 [3:0]	R/W	**DSS**	TX Data size select 0000~0010 : Reserved 0011 : 4-bit data 0100 : 5-bit data 0101 : 6-bit data 0110 : 7-bit data 0111 : 8-bit data 1000 : 9-bit data 1001 : 10-bit data 1010 : 11-bit data 1011 : 12-bit data 1100 : 13-bit data 1101 : 14-bit data 1110 : 15-bit data 1111 : 16-bit data	0x7
			PTR Register	
0x2A [11:0]	R	**SIF_WR_PTR**	Memory WRITE point to the instruction register on Serial Data transfer mode	0x0
0x2C [11:0]	R	**SIF_RD_PTR**	Memory READ point to the instruction register on Serial Data transfer mode	
			PIP_STATE Register	
0x2E [11:0]	R	**PIP_UPDATE**	Check to updated on/off of PIP_MODE	
			ERROR Register (1'h0)	
0x32 [1]	R	**Overflow ERROR**	PIF Memory Overflow 0 : No Error 1 : Error Detection	-
0x32 [0]	R	**RESYNC ERR**	SIF Sync Error 0 : No Error 1 : Error Detection	-
0x34 [0]	W	**RESYNC ERR CLEAR**	Error Clear register	-
			FIC_RD_ADDR_READ Register (Default : 8'h00)	
0x36 [7:0]	R/W	**FIC_RD_ADDR**	FIC Memory Read Address	0x00
			DEMAND INTERVAL COUNTER Register	
0x38 [12:0]	R/W	**DEMAND_INTV_CNT**	Holding SPI bus as value of counter	0x0

			REGISTER DEMAND	
0x3A [0]	W	**REG_DEMAND**	Swap to Demand Value	-
			SPI PAD CONTROL Register	
0x3C [1]	R/W	**SPI_PAD_CTRL_EN**	SPI(CLK, EN, DATA) PAD Control Enable 0 : PAD control via SPI 1 : Control via Register value	0x0
0x3C [0]	R/W	**SPI_PAD_OEn**	SPI PAD OEn signal 0 : Output 1 : Input	0x0

APB SUB-SYSTEM

SYSTEM ARCHITECTURE

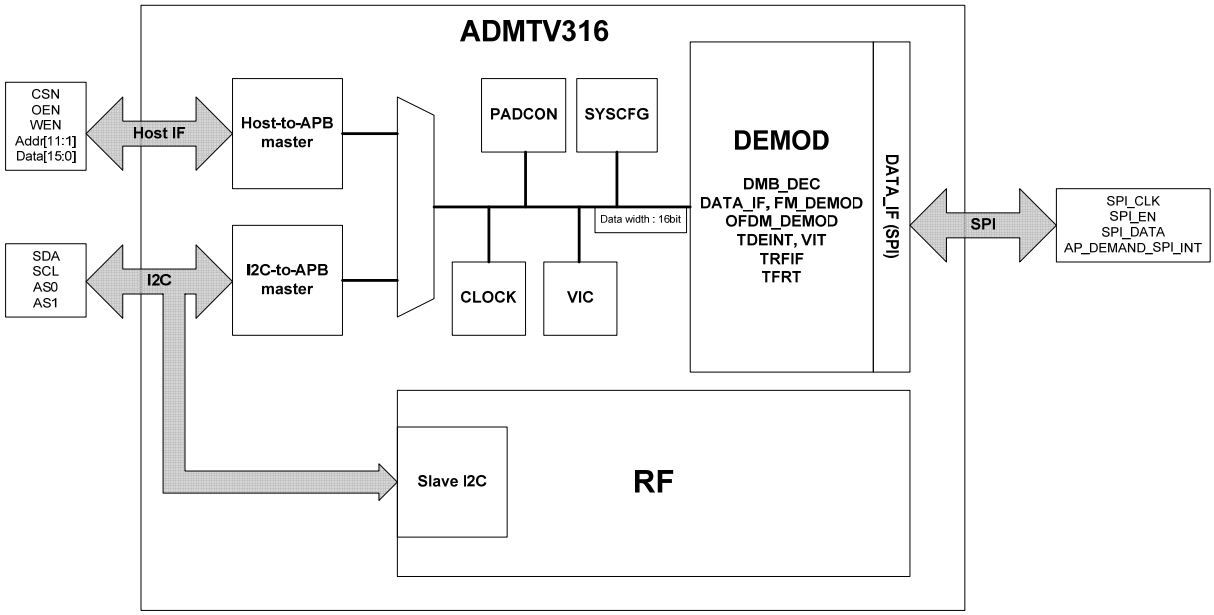


Figure 12. ADMTV316 System Architecture

ADDRESS MAP

Table 12. APB Sub-System Address Map

Start address [9:0]	End address [9:0]	Description	Size: Half word (2 Byte)
		PSEL_CLK: Clock top	
0×000	0×07F	CLK_TOP	64 Half word
		PSEL_SYSTEM: VIC, SYSCFG, PADCON	
0×080	0×09F	VIC	16 Half word
0×0A0	0×0BF	SYSCFG	16 Half word
0×0C0	0×0DF	PADCON	16 Half word
0×0E0	0×0FF	Reserved	16 Half word
		PSEL_DEC: MT_DEC	
0×100	0×17F	MT_DEC	64 Half word
		PSEL_DATA_IF: DATA_IF, FM_DEMOD	
0×180	0×1BF	DATA_IF	32 Half word
0×1C0	0×1FF	FM_DEMOD	32 Half word
		PSEL_OFDM_DEMOD: OFDM_DEMOD	
0×200	0×27F	OFDM_DEMOD	64 Half word
		PSEL_TDEINT: TDEINT, VIT	
0×280	0×2BF	TDEINT	32 Half word
0×2C0	0×2FF	VIT	32 Half word
		PSEL_TRFIF: TRFIF	
0×300	0×37F	TFRIF	64 Half word
		PSEL_TFRT: TFRT	
0×380	0×3FF	TFRT	64 Half word

NOTES:
The above address values are referenced to [9:0] and they are addressed by AP.

AP CONNECTION DIAGRAM

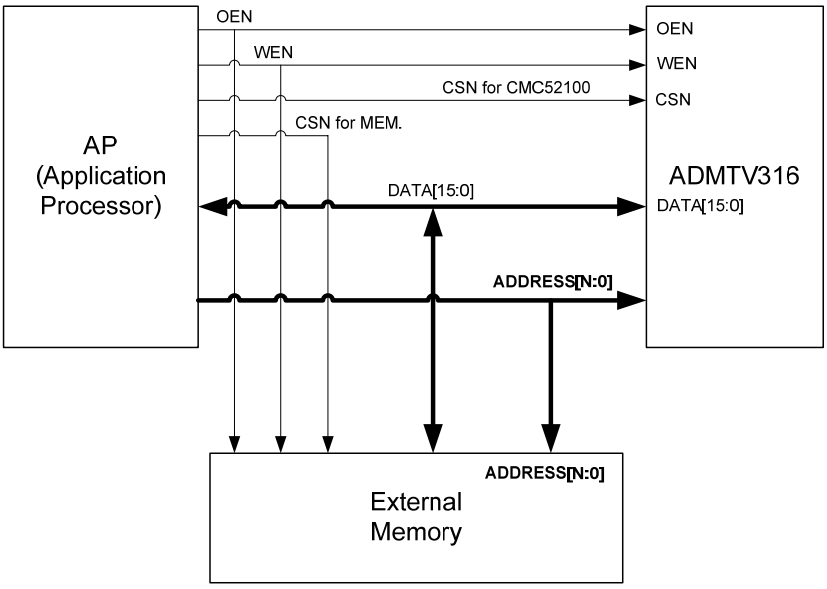


Figure 13. Host Interface Connection Diagram

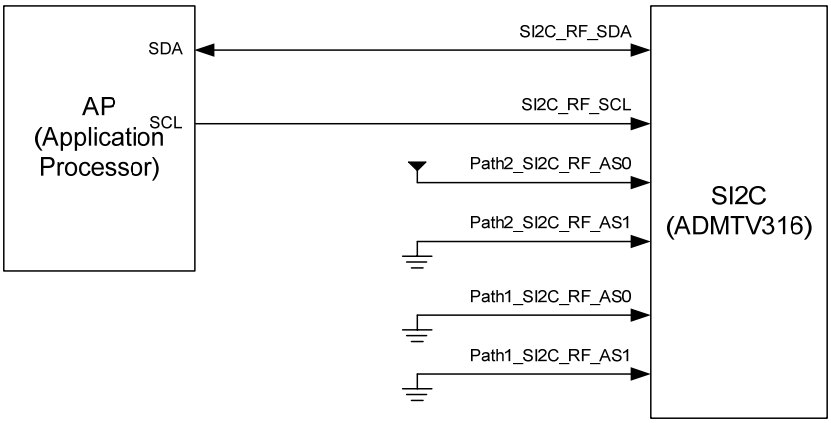


Figure 14. I²C Interface Connection Diagram (2 PIP Package)

APB SUB-SYSTEM COMPONENTS

ADMTV316 is a basic CPUless system that has no internal processor and operates with control signals from CPU of AP. It has an APB master block which converts asynchronous memory interface (Host interface) signal or slave I²C interface (SI²C) signal coming from AP to APB interface signals. MCU of AP can access to all of ADMTV316 registers through this interface.

There are 2-types of access modes in as:

- Normal mode 1: AP accesses to ADMTV316 by Host interface. (See mode table.)

- Normal mode 2: AP accesses to ADMTV316 by SI²C interface. (See mode table.)

Users can select freely one of these modes, which is most suitable for his application purpose. However, internal RF blocks of ADMTV316 can be accessible by SI²C interface only. For stable access by Host interface from AP, there should be timing margin as shown in figure 13.

In this timing diagram, CSB can operate normally only when HOST_ADDR[11:10] has the same value as AS1 and AS0, i.e., HOST_ADDR[11:10] = {AS1, AS0}

Host Interface

- Async. Memory (SRAM) interface
- Mode pin set to normal mode 1.
- 16bit access (half word) only

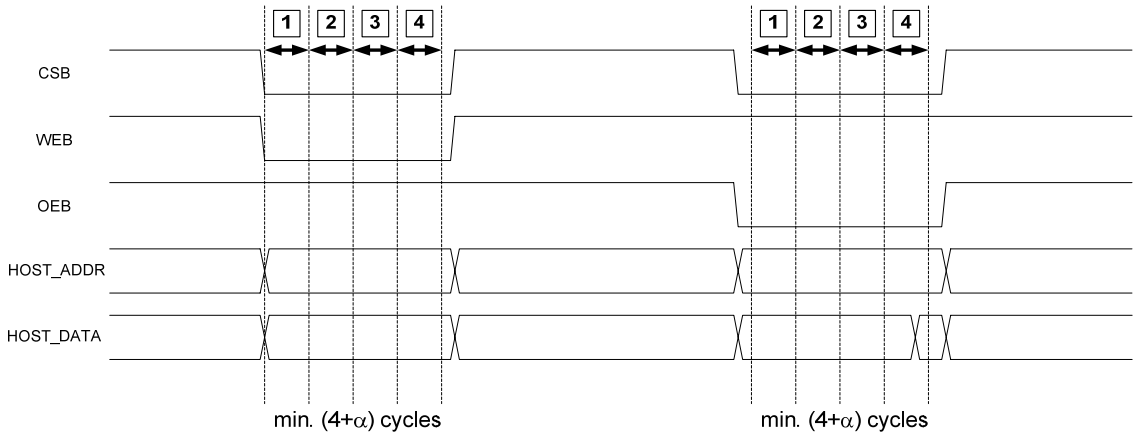


Figure 15. Read/Write Access Timing Diagram

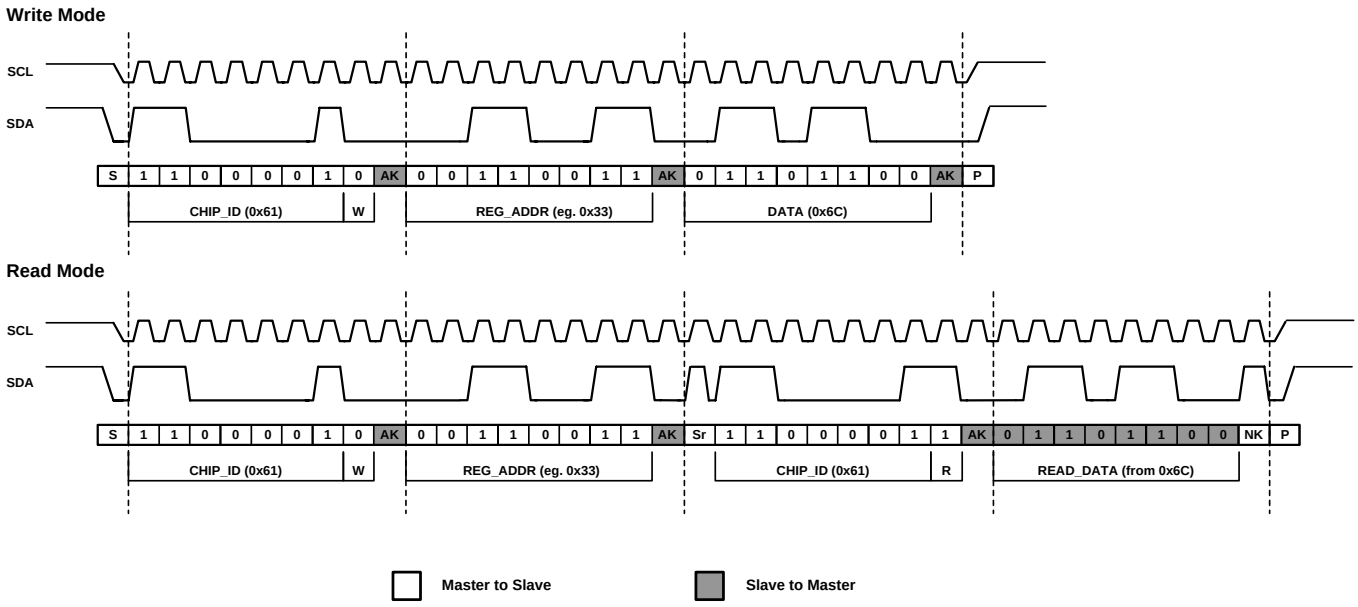
SI²C Interface

- Slave only interface
- Mode pin set to normal mode 2.
- Supports both of standard mode (100 kbps) and fast mode (400 kbps)
- Baseband I²C features
  - Slave address length = 6 bits.
  - MSB 4bits (A5 ~ A2) value = b1010. LSB 2 bits (A1 ~ A0) is obtained from primary input (AS1, AS0).
  - Register address = 9bits.
  - I²C basic functional combinations are 2-byte write-access, 2-byte read-access and multiple write-accesses.
- RF Tuner I²C features
  - Slave address length = 7 bits.
  - MSB 4bits (A6 ~ A0) value = b1100001 (0×61)
  - Register address = 8 bits.
  - I²C basic functional combinations are 1-byte write-access, 1-byte read-access and multiple write-accesses.

I²C Timing Characteristics

(T_A = 25°C, V_{DDIO} = 3.3 V, GND = 0 V, unless otherwise noted.)

According to standard I²C specification, the CLK frequency reaches maximum 400 kHz in fast-mode and 100 kHz in standard-mode. To communicate with RF tuner, you need to comply as the following timing diagrams.



NOTES
S = Start condition, P = Stop condition, Sr = Repeated Start (Stop + Start, fast transition) condition, AK = Acknowledge: Active low, NK = Not Acknowledge: Active high, W = Write mode, R = Read mode
CMC52100-S1 needs a stop transition in the repeated start condition. Therefore, upper access condition is able to be modified on standard I²C.

Figure 16. Serial Control Port Write/ Read Mode

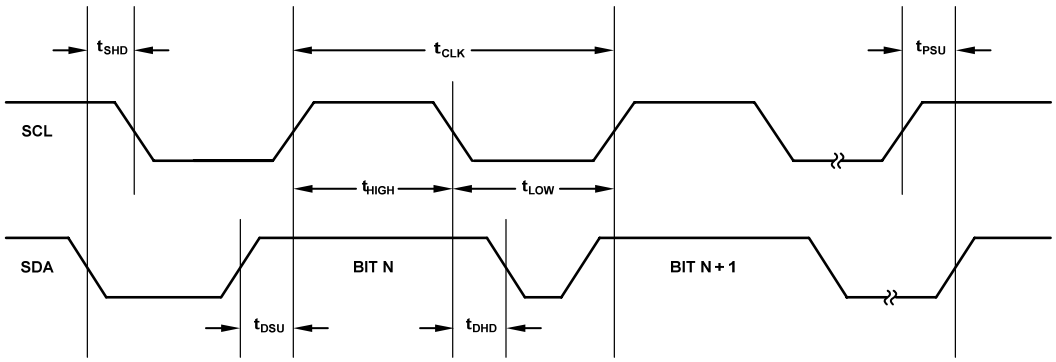


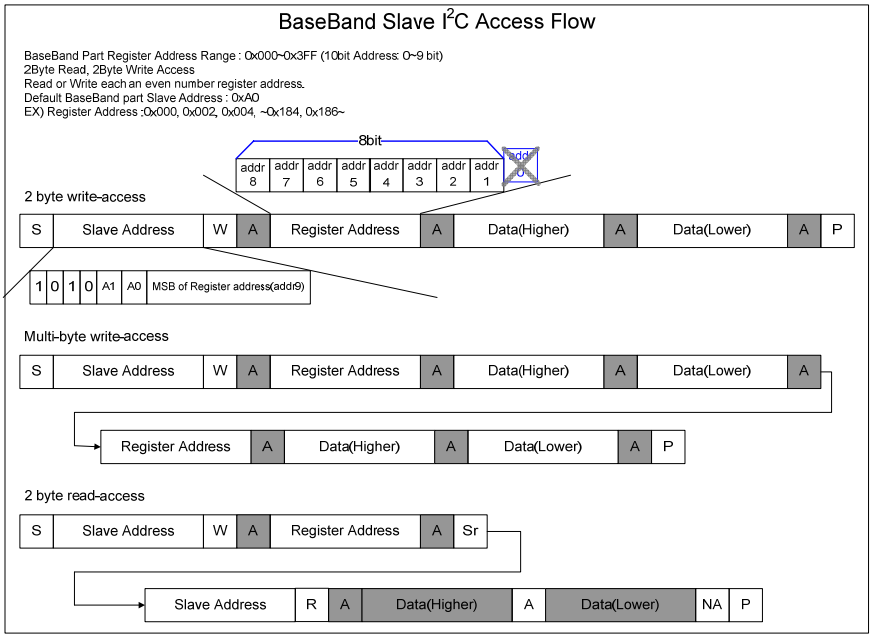
Figure 17. Serial Control Port Timing

Table 13. Serial Control Port Timing

		Standard-mode		Fast-mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Hold Time (Repeat) Start Condition[1]	t_{SHD}	4.0		0.6		µs
SCL Clock Period	t_{CLK}	0	100	0	400	kHz
HIGH Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
LOW Period of the SCL Clock	t_{LOW}	4.7		1.3		µs
Set-up Time for STOP Condition	t_{PSU}	4.0		0.6		µs

		Standard-mode		Fast-mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Data Set-up Time	t_{DSU}	250		100[2]		ns
Data Hold Time for I²C Bus Devices.	t_{DHD}	5.0				µs
		0[3]	3.45[4]	0[3]	0.9[4]	µs

NOTES
[1]Afer this period, the first clock pulse is generated.
[2]A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{DSU} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.
[3]A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
[4]The maximum t_{DHD} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.



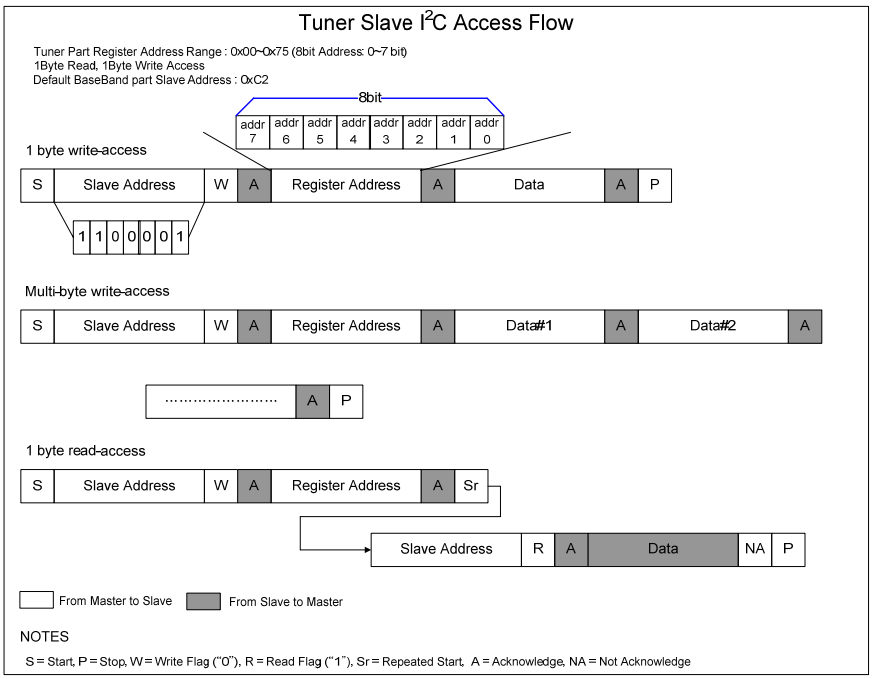


Figure 18. Functional Combination

Vectored Interrupt Controller

The VIC provides a software interface to the interrupt system. In a system with an interrupt controller, software must determine the source that is the requesting service and where its service routine is loaded. A VIC does both of these in hardware. It supplies the interrupt index of the corresponding to the highest priority requesting interrupt source.

The interrupt vector [0] has the highest priority, followed by interrupt vector [1] ~ [15]. In addition, interrupt vector0 has the higher priority than interrupt vector1. The priority of each of the vectored interrupt is programmable, enabling the order the interrupt are served in to be dynamic changing. This is done by programming the value in the vector priority registers. If multiple interrupts are set to the same-programmed priority level, the fixed hardware priority level is used to determine the order the interrupts on that level are serviced. This is also applicable when the priority registers are not programmed. Interrupt [0] has the highest hardware priority level, and interrupt [15] has the lowest. The software can control each request line to generate software interrupts.

There are 32-vectored interrupts available. Reading from the vector interrupt index register, VIC_INDEX, provides the fixed index of the interrupt sources, and the updates the interrupt priority hardware that masks out the current and any lower priority interrupt requests. Writing to the VIC_INDEX register indicates to the interrupt priority hardware that current interrupt is served, enabling the masking of lower priority or the same priority interrupts to be removed and for the interrupts to become active.

There are several features as follows.

- Support for 16 vectored interrupts
- Fixed hardware interrupt priority levels
- Programmable interrupt priority levels
- Software interrupt generation
- Raw interrupt status
- Interrupt request status

S/W setting guide for boot-up

1. Clear INT_PEND* register (mandatory)
2. Set VIC_PRIORITY_*_* register for each interrupt (not mandatory)
3. Set INTENABLE* register for each interrupt (mandatory)

Interrupt Service Routine procedure

1. Read INT_INDEX register and branch to the Interrupt Service Routine
2. Clear INT_PEND register for corresponding interrupt
3. Execute your ISR
4. Write any value to INT_INDEX register and return from the interrupt.

APPLICATIONS

SPI SCHEMATIC

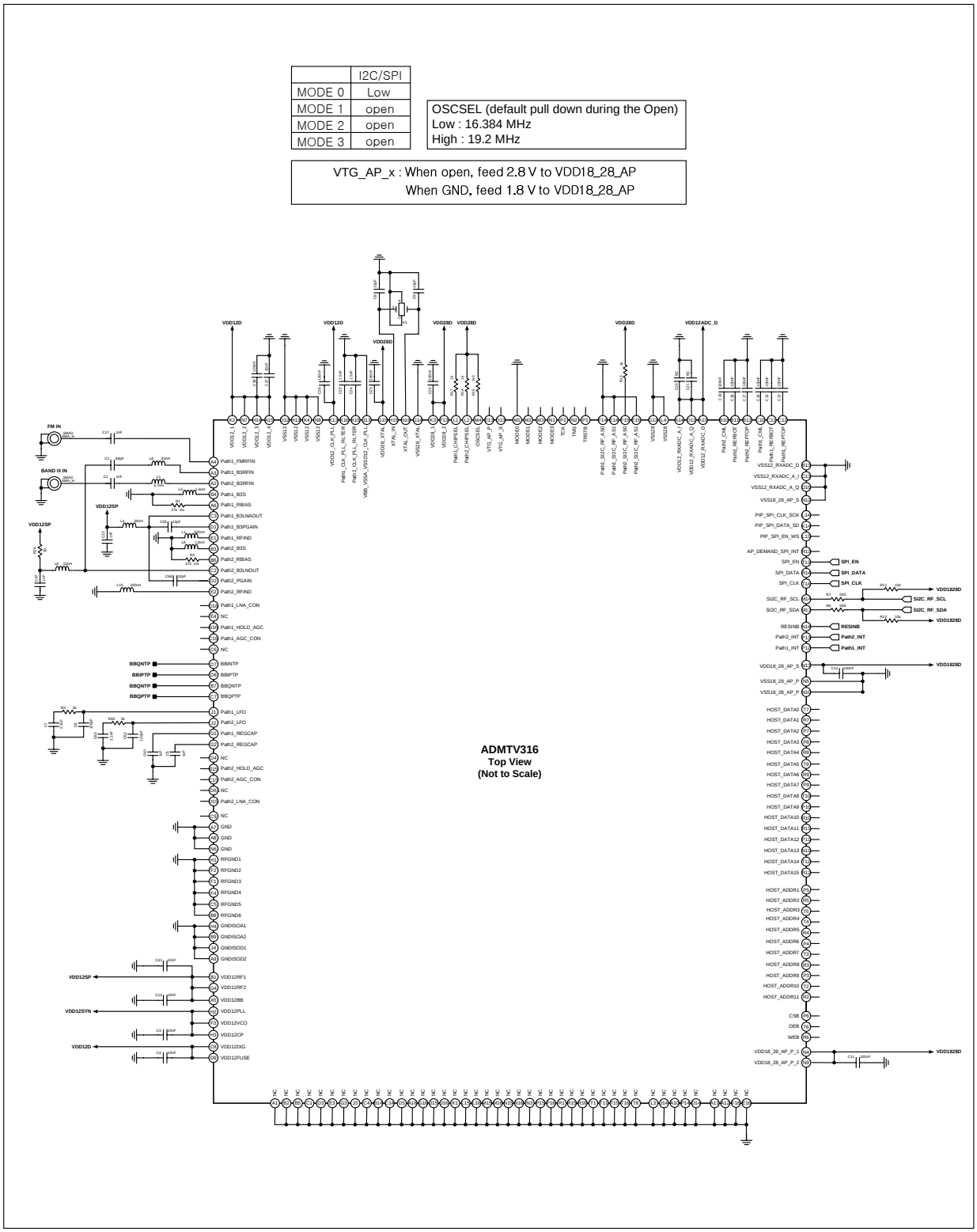


Figure 19. SPI Application Schematic

HOST MEMORY INTERFACE SCHEMATIC

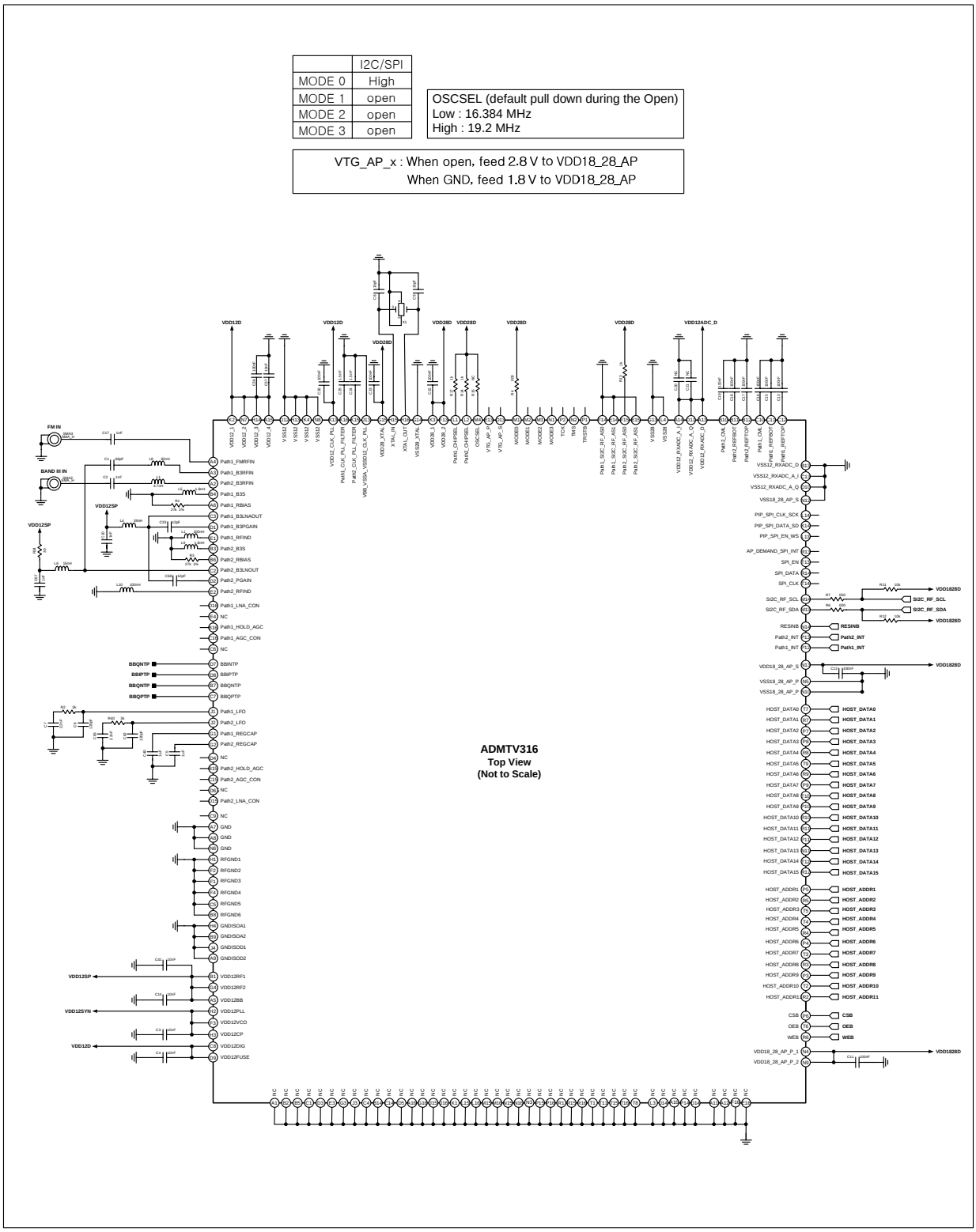


Figure 20. Host Interface Application Schematic

OUTLINE DIMENSIONS

Package

- Size: 9 × 9mm²
- Max height: 1.2 mm
- Ball Array: 16 × 16 matrix, 4 rows, 192 balls, 0.5 mm pitch

Solder Ball

- Lead-free
- 0.3 mm diameter

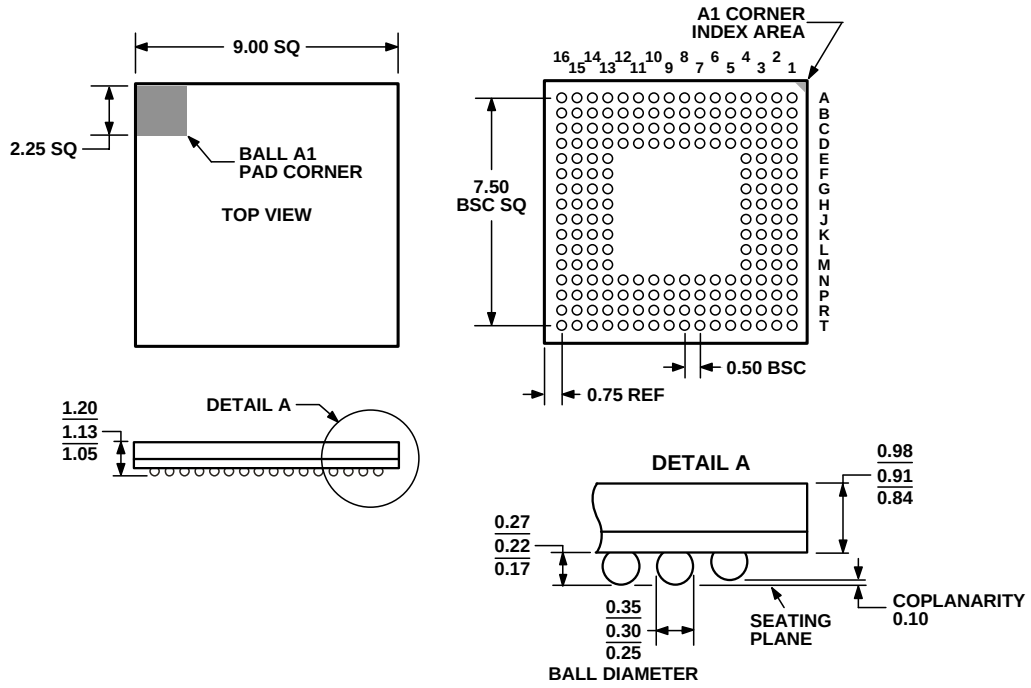


Figure 21. 192-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
9 mm × 9 mm Body
(BC-192)
Dimensions shown in millimeters

ORDERING GUIDE

PKG	Description	Ordering Guide	Marking	SAP Registration
CSP-BGA	Band-III/FM	ADMTV316ABCZRL	316A	o
Eval. Board	Evaluation Board for ADMTV316A CSP-BGA	ADMTV316AC-EB		

NOTES

PR07979-0-12/08(PrA)