UHF/S-Band Tuner IC for CMMB

Preliminary Technical Data

ADMTV800

FEATURES

- **Single-chip RF tuner IC for China Multimedia Mobile Broadcasting (CMMB) applications in UHF and S-Band**
  - **UHF (470 MHz to 862 MHz)**
  - **S-Band (2635 MHz to 2660 MHz)**
- **Zero-IF architecture**
- **Low noise figure**
  - **UHF: 3 dB**
  - **S-Band: 5.5 dB**
- **Supports 2, 8 MHz signal bandwidth**
- **Typical AGC dynamic range: -102 dBm to +10 dBm**
- **Low power consumption in continuous mode**
  - **UHF: 94 mW**
  - **S-Band: 113 mW**
- **On-chip features include**
  - **Power-on-Reset**
  - **Fast switching fractional-N PLL**
  - **Low phase noise and wide frequency range VCO**
  - **PLL loop filter**
  - **Bandwidth-adjustable low-pass filter**
  - **Reference clock output for demodulators**
- **Integrated baseband PGA for direct connection to digital demodulators**
- **Noise/linearity optimization through internal RFAGC loop**
- **Adjustable take-over point**
- **I²C serial bus interface**
- **Small 24-lead lead frame chip scale package (LFCSP) (4 mm × 4 mm)**
- **Small wafer level chip scale package (WLCSP)**
- **Minimal external components**
  - **7 ea for dual-band**

APPLICATIONS

CMMB mobile and portable TV receivers

FUNCTIONAL BLOCK DIAGRAM

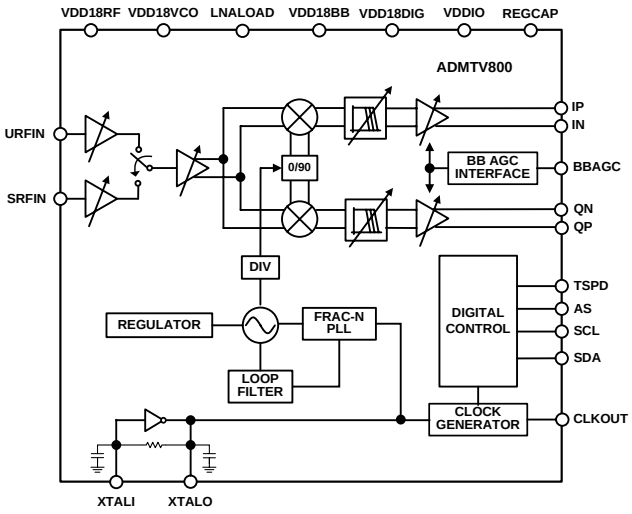

Figure 1

GENERAL DESCRIPTION

The ADMTV800 is a highly integrated CMOS zero-IF conversion tuner IC for China Multimedia Mobile Broadcasting (CMMB). The part includes dual RF input bands, UHF and S-band. The building blocks of the ADMTV800 include LNA, RFPGA, I/Q downconversion mixer, bandwidth adjustable low-pass filter, baseband PGA and fractional-N frequency synthesizer with fully integrated VCO and PLL loop filter. The on-chip low phase noise VCO, along with the high resolution fractional-N frequency synthesizer makes in-band phase noise low enough for mobile TV applications.

By using very small package size (LFCSP, WLCSP), the ADMTV800 is the best solution for CMMB application especially for mobile phones, notebook PCs, PDAs, etc. where low power consumption is critical. The part has an I²C serial bus interface.

Rev. PrA

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SPECIFICATIONS [TBD]

DC ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
1.8 V Supply Voltage (VDD18RF, VDD18VCO, LNALOAD, VDD18BB, VDD18DIG)	V_{DD18}	1.7	1.8	1.9	V
I/O Supply Voltage (VDDIO)	V_{DDIO}	1.7	2.8	3.6	V
BBAGC Input Voltage	V_{BBAGC}	0		3.6	V
BBAGC Input Current	I_{BBAGC}	-10		10	µA
LNACON Output Voltage at enable mode (LFCSP)	V_{LNACON}	1.7	1.8	1.9	V
LNACON Output driving Current at enable mode (LFCSP)	I_{LNACON}		18		mA
DIGITAL INPUT/OUTPUT PINS (TSPD, AS, SCL, SDA, CLKOUT)					
Maximum Low Input Voltage	V_{IL}			$0.3 \times V_{DDIO}$	V
Minimum High Input Voltage	V_{IH}	$0.7 \times V_{DDIO}$			V
Maximum Low Output Voltage	V_{OL}			$0.4 \times V_{DDIO}$	V
Minimum High Output Voltage	V_{OH}	$V_{DDIO} - 0.4$			V
High Level Input Current ($V_{IN} = V_{DDIO}$)	I_{IH}	-10		10	µA
Low Level Input Current (V_{IN} = GND)	I_{IL}	-10		10	µA
UHF POWER CONSUMPTION					
1.8 V Analog Current Consumption	$I_{DD18AUHF}$		50		mA
1.8 V Digital Current Consumption	$I_{DD18DUHF}$		1		mA
I/O Digital Current Consumption	$I_{DDIOUHF}$		1		mA
Power-Down Current Consumption	I_{PDUHF}		1		µA
Total Power Consumption	P_{UHF}		94		mW
S-BAND POWER CONSUMPTION					
1.8 V Analog Current Consumption	$I_{DD18AS\text{-}BAND}$		61		mA
1.8 V Digital Current Consumption	$I_{DD18DS\text{-}BAND}$		1		mA
I/O Digital Current Consumption	$I_{DDIOS\text{-}BAND}$		1		mA
Power-Down Current Consumption	$I_{PDS\text{-}BAND}$		TBD		µA
Total Power Consumption	$P_{S\text{-}BAND}$		113		mW

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD18} = 1.8 V, VDDIO = 2.8 V, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
REFERENCE CRYSTAL OR CLOCK INPUT FREQUENCY	f_{CLK}	13		40	MHz
UHF CHARACTERISTICS					
RF Frequency Range	f_{UHF}	470		862	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1		
Typical AGC Dynamic Range	P_{IN}	-102		10	dBm
Noise Figure @ Maximum Gain	NF				dB
In-Band Two-Tone IMD3 (U/D)[1]	$IMD3_{IN}$		TBD		dBc
Out-of-Band IIP3[2]	$IIP3_{OUT}$		TBD		dBm
3 dB Cutoff Frequency[3]	f_{3dB}	1		4	MHz
Stop Band Attenuation[4]	SBA		TBD		dBc
LO Phase Noise (SSB @ 100 kHz Offset)	PN_{100k}		-99		dBc/Hz
Baseband Output Amplitude V p-p, Single	V_{OUTAC}		500	700	mV
BB Output Pins (QP, QN, IN, IP)					
Minimum Load Resistance, Differential	$R_{L\ MIN}$	2			kΩ
Maximum Load Capacitance, Differential	$C_{L\ MAX}$		TBD		pF
Output DC Voltage	V_{OUTDC}		0.9		V
S-BAND CHARACTERISTICS					
RF Frequency Range	$f_{S\text{-}BAND}$	2635		2660	MHz
RF Input Impedance	Z_{IN}		50		Ω
Input VSWR	VSWR		2:1		
Typical AGC Dynamic Range	P_{IN}		TBD		dBm
Noise Figure @ Maximum Gain	NF		5.5		dB
In-Band Two-Tone IMD3 (U/D)[1]	$IMD3_{IN}$		TBD		dBc
Out-of-Band IIP3[2]	$IIP3_{OUT}$		TBD		dBm
3 dB Cutoff Frequency[3]	f_{3dB}	1		4	MHz
Stop Band Attenuation[4]	SBA		TBD		dBc
LO Phase Noise (SSB @ 100 kHz Offset)	PN_{100k}		TBD		dBc/Hz
Baseband Output Amplitude V p-p, Single	V_{OUTAC}		500	700	mV
Baseband Output Pins (QP, QN, IN, IP)					
Minimum Load Resistance, Differential	$R_{L\ MIN}$	2			kΩ
Maximum Load Capacitance, Differential	$C_{L\ MAX}$		TBD		pF
Output DC Voltage	V_{OUTDC}		0.9		V

[1] For RF input power, P_{IN} < −30 dBm, f1 = f2 = 200 kHz frequency offset.
[2] For RF input power, P_{IN} = −80 dBm, two-tone interferer power = −35 dBm, f1 = 13.25 MHz frequency offset, f2 = 29.25 MHz frequency offset. RFAGC: closed-loop gain control, BBAGC: external gain control.
[3] Programmable.
[4] For 4.87 MHz offset @ 4 MHz LPF cutoff.

DIGITAL TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol[1]	Min	Unit
TSPD Setup Margin	A	Don't Care	µs
Power-Up Setup Margin for V_{DD18}	B	Don't Care	µs
Power-Up Setup Margin for V_{DDIO}	C	Don't Care	µs
Setup Time for I^2C Interface	D	TBD	µs

[1] See Figure 2.

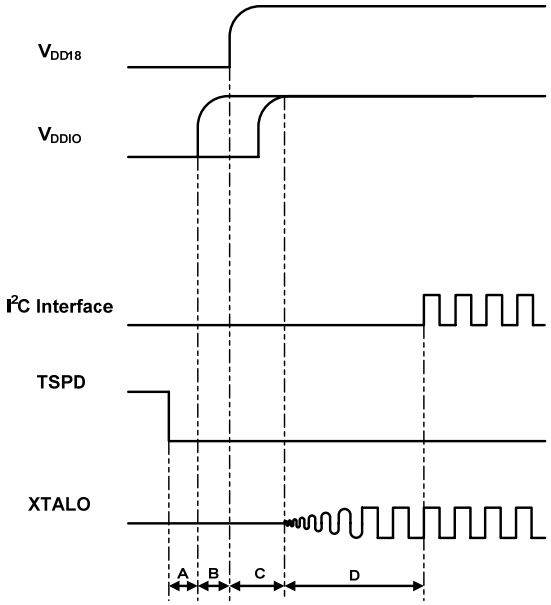


Figure 2. Digital Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
1.8 V Supply Voltage (V_{DD18})	–0.5 V to +2.1 V
I/O Supply Voltage (V_{DDIO})	–0.5 V to + 4.0 V
Analog Input Voltage	–0.5 V to V_{DD18} + 0.3 V
Digital Input Voltage	–0.5 V to V_{DDIO} + 0.5 V
Analog Output Voltage	–0.5 V to V_{DD18} + 0.3 V
Digital Output Voltage	–0.5 V to V_{DDIO} + 0.5 V
Operating Temperature Range	–45°C to +85°C
Storage Temperature Range	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

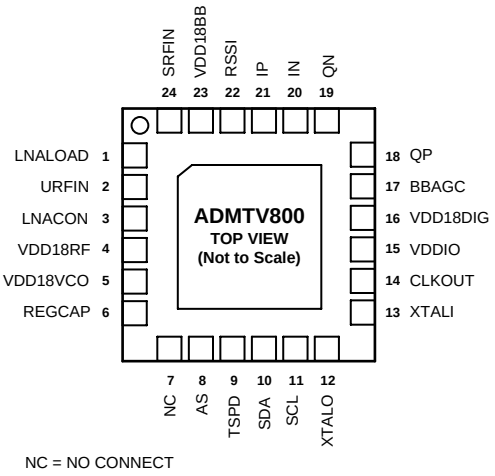


Figure 3. Pin Configuration [LFCSP]

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	I/O Type[1]	Description
1	LNALOAD	P	RF Power (1.8 V). This pin should be decoupled with a 1 nF capacitor.
2	URFIN	AI	UHF RF Input.
3	LNACON	P	S-band External LNA Power (1.8 V). External LNA gain is controlled by this pin.
4	VDD18RF	P	RF Power (1.8 V). This pin should be decoupled with a 1 nF capacitor.
5	VDD18VCO	P	VCO Power (1.8 V). This pin should be decoupled with a 1 nF capacitor.
6	REGCAP	P	Regulator output decoupling Capacitor. This pin should be decoupled with a 470 nF capacitor.
7	NC		No Connection.
8	AS	DI	Address Selection. The I^2C address can be determined by the AS pin. If AS is connected to GND, read mode address = 0xC3, write mode address = 0xC2. If AS is connected to VDDIO, read mode address = 0xC5, write mode address = 0xC4.
9	TSPD	DI	Time-Slicing Power-Down. Apply 0 V to this pin for normal operation. Apply VDDIO for time-slicing power-down.
10	SDA	DB	I^2C Data. Bidirectional pin.
11	SCL	DI	I^2C Clock.
12	XTALO	AO	Crystal Oscillator Output. Inverter buffer output.
13	XTALI	AI	Crystal Oscillator Input. Inverter buffer input.
14	CLKOUT	AO	Clock Output.
15	VDDIO	P	Wide Range I/O Power (1.8 V to 3.3 V).
16	VDD18DIG	P	Digital Power (1.8 V).
17	BBAGC	AI	BBAGC Input (0 V to 3.3V).
18	QP	AO	Quadrature-Phase Positive Output.
19	QN	AO	Quadrature-Phase Negative Output.
20	IN	AO	In-Phase Negative Output.
21	IP	AO	In-Phase Positive Output.
22	RSSI	AO	RSSI Output voltage for Adjacent channels. A 33nF capacitor should be connected as close as possible between this pin and GND.
23	VDD18BB	P	Baseband Block Power (1.8 V). This pin should be decoupled with a 100 nF capacitor.
24	SRFIN	AI	S-BAND RF Input.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DB = digital bidirectional, P = power.

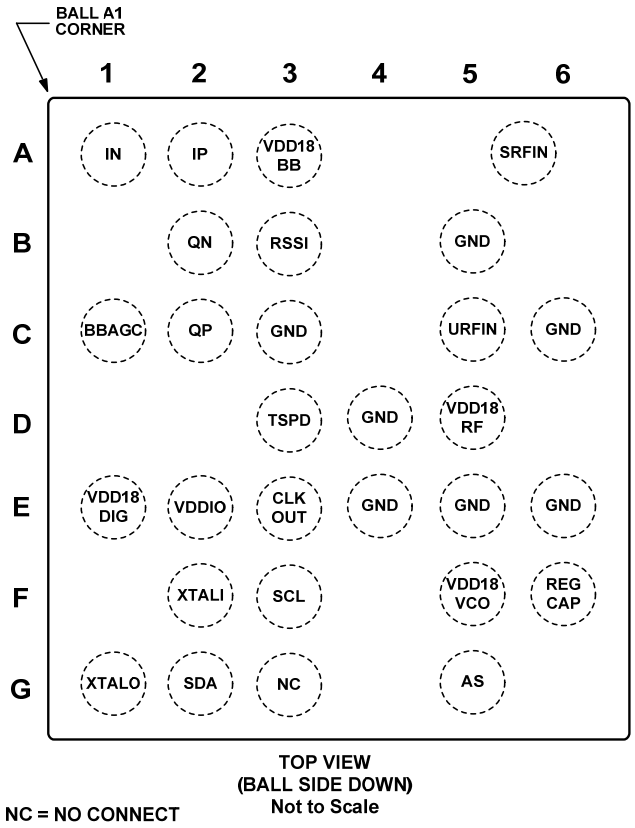


Figure 4. Pin Configuration [WLCSP]

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	I/O Type[1]	Description
A1	IN	AO	In-Phase Negative Output.
A2	IP	AO	In-Phase Positive Output.
A3	VDD18BB	P	Baseband Block Power (1.8 V). This pin should be decoupled with a 100 nF capacitor.
A5	SRFIN	AI	S-BAND RF Input.
B2	QN	AO	Quadrature-Phase Negative Output.
B3	RSSI	AO	RSSI Output voltage for Adjacent channels. A 33nF capacitor should be connected as close as possible between this pin and GND.
B5	GND	G	Connect to GND.
C1	BBAGC	AI	BBAGC Input (0 V to 3.3 V).
C2	QP	AO	Quadrature-Phase Positive Output.
C3	GND	G	Connect to GND.
C5	URFIN	AI	UHF RF Input.
C6	GND	G	Connect to GND.
D3	TSPD	DI	Time-Slicing Power-Down. Apply 0 V to this pin for normal operation. Apply VDDIO for time-slicing power-down.
D4	GND	G	Connect to GND.
D5	VDD18RF	P	RF Power (1.8 V). This pin should be decoupled with a 1 nF capacitor.
E1	VDD18DIG	P	Digital Power (1.8 V).
E2	VDDIO	P	Wide Range I/O Power (1.8 V to 3.3 V).
E3	CLKOUT	AO	Clock Output.
E4	GND	G	Connect to GND.
E5	GND	G	Connect to GND.
E6	GND	G	Connect to GND.

Pin No.	Mnemonic	I/O Type[1]	Description
F2	XTALI	AI	Crystal Oscillator Input. Inverter buffer input.
F3	SCL	DI	I^2C Clock.
F5	VDD18VCO	P	VCO Power (1.8 V). This pin should be decoupled with a 1 nF capacitor.
F6	REGCAP	P	Regulator output decoupling Capacitor. This pin should be decoupled with a 470 nF capacitor.
G1	XTALO	AO	Crystal Oscillator Output. Inverter buffer output.
G2	SDA	DB	I^2C Data. Bidirectional pin.
G3	NC		No Connection.
G5	AS	DI	Address Selection. The I^2C address can be determined by the AS pin. If AS is connected to GND, read mode address = 0xC3, write mode address = 0xC2. If AS is connected to VDDIO, read mode address = 0xC5, write mode address = 0xC4.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, DB = digital bidirectional, P = power, G = ground.

TYPICAL PERFORMANCE CHARACTERISTICS [TBD]

TERMINOLOGY

Input Third-Order Intercept (IIP3)
A figure of merit used to determine a component's or system's susceptibility to intermodulation distortion (IMD) from its third-order nonlinearities. Two unmodulated carriers at a specified frequency relationship (f1 and f2) are injected into a nonlinear system exhibiting third-order nonlinearities, producing IMD components at (2 × f1) − f2 and (2 × f2) − f1. IIP3 graphically represents the extrapolated intersection of the carrier's input power with the third-order IMD component when plotted in decibels.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa, nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n is equal to zero.

For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

Noise Figure (NF)
The degradation in SNR performance (in dB) of an IF input signal after it passes through a component or system.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Voltage Standing-Wave Ratio (VSWR)
The ratio of the amplitude of the elective field at a voltage maximum to that at an adjacent voltage minimum.

THEORY OF OPERATION

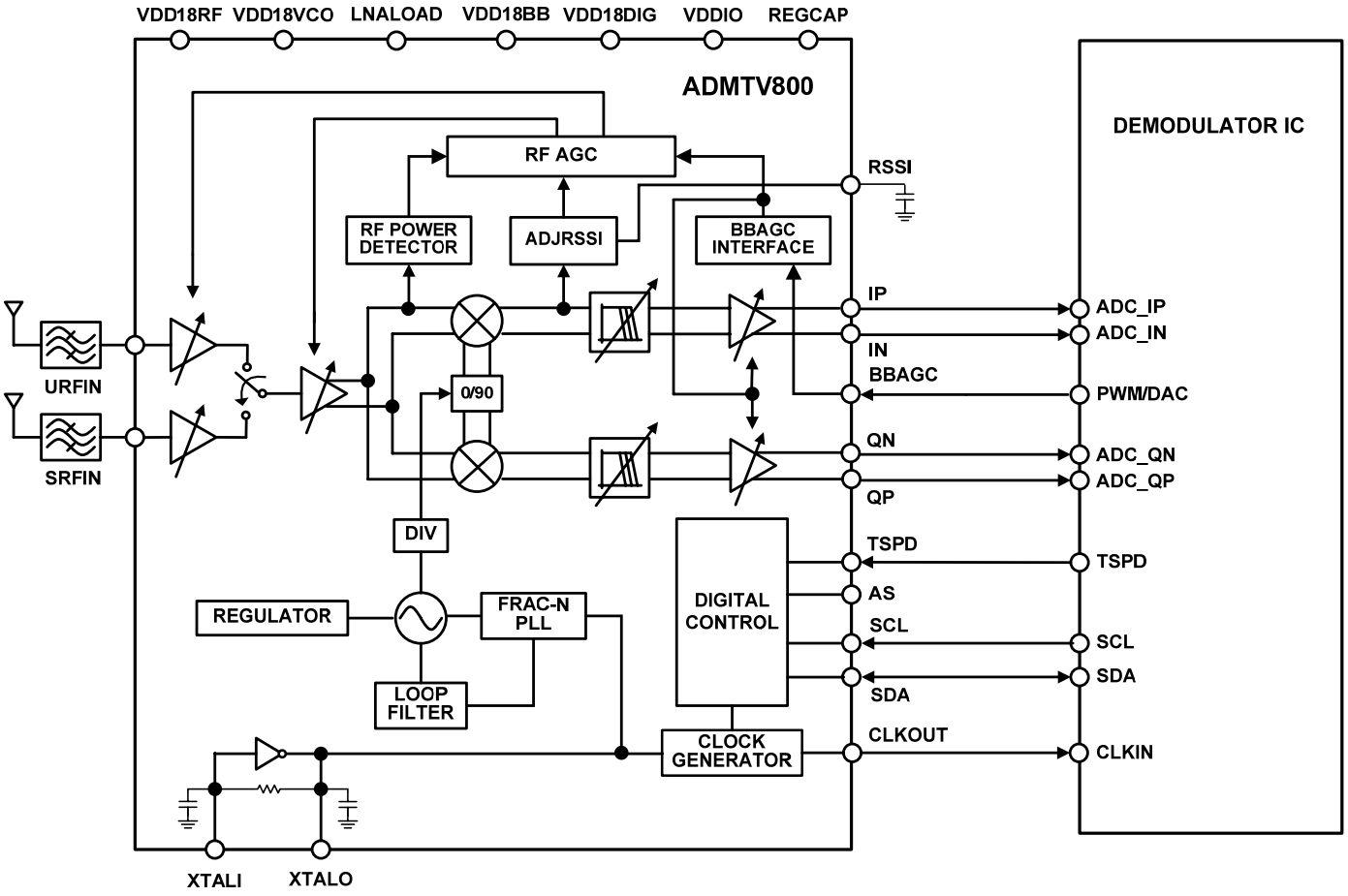


Figure 5. ADMTV800 Interface

LOW NOISE AMPLIFIER (LNA)

ADMTV800 LNA consists of two LNA, and each LNA supports UHF band (470~862 MHz) and S-band (2635~2660MHz). The LNA has 4 gain modes, which are 18 dB, 7 dB, -3 dB and -21 dB. The LNA gain state can be read from the LNAGAIN register. When LNAGAIN<1:0>=0x03, it is in high gain state, LNAGAIN<1:0>=0x10, it is in middle gain state, LNAGAIN<1:0>=0x01, it is in low gain state, and LNAGAIN<1:0>=0x00, it is in very low gain state.

RF PROGRAMMABLE GAIN AMPLIFIER (PGA)

The RFPGA has a dynamic gain range of 36 dB. RFPGA gain is controlled by digital gain code, which can be read from the RFAGC register. RFAGC register ranges from 0x00 (minimum gain) to 0x5F (maximum gain). The gain step is 0.5 dB.

I/Q DOWNCONVERTER

The I/Q downconversion mixer amplifies incoming RF signals from the RFPGA output and converts the signals to baseband.

LOCAL OSCILLATOR

Voltage Controlled Oscillator (VCO)

The ADMTV800 includes an on-chip VCO, which eliminates the need for an external LC tank. This internal VCO uses only 1.8 V and covers the UHF band (470~862 MHz) and S-band (2635~2660MHz). Along with the fractional-N PLL, this low phase noise VCO guarantees sufficient performance for mobile reception of worldwide mobile TV.

Phase Locked Loop (PLL)

The PLL synthesizer includes integrated 20-bit fractional-N PLL and integrated loop filter. Integrated loop filter eliminates extra external passive components. In addition to the integrated VCO, the ADMTV800 local oscillator consists of a Σ-Δ fractional-N PLL frequency synthesizer. The fractional-N type architecture with a high performance 20-bit Σ-Δ modulator obtains high resolution and fast switching times, as well as good phase noise.

For compensating variable VCO gain, control bits of CP_COMP<4:0> are available. Unlike integer-N type synthesizers used in other silicon tuners, Σ-Δ modulated frequency synthesizers provide the following features:

- Fast switching time.
- Ultra high frequency resolution.
- Good phase noise due to its wide bandwidth.

Using a 20 MHz crystal oscillator with a 20-bit Σ-Δ modulated fractional-N PLL exhibits a very fine frequency resolution of 19 Hz. The PLL can compensate for the frequency offset induced by such factors as the reference crystal frequency error and the temperature drift of a crystal.

The local oscillator frequency, f_{LO}, is calculated as the following equations:

$$f_{PLL} = \frac{f_{crytal}}{PLLR} \cdot \left(PLLN + \frac{PLLF}{2^{20}} \right)$$

$$f_{LO} = \frac{f_{PLL}}{PLLS}$$

where:
PLLN is the integer divide value selected by the PLLN register.
PLLF is the fractional divide value selected by the PLLF register.

PLLR is the reference crystal frequency divide ratio selected by PLLR register.
PLLS is selected by the divide ratio between LO frequency and PLL frequency (see the PLL Setting section for more information).

BASEBAND PROGRAMMABLE GAIN LOW-PASS FILTER (LPF) AND AGC

The baseband block contains a programmable gain LPF and output buffer. The 6th order BB LPF's cutoff frequency supports 2 MHz and 8 MHz signal bandwidth modes and 6 dB to 60 dB programmable gain by 0.25 dB step size. To compensate the LPF cutoff frequency variation, the automatic tuning circuit is included. The BB AGC controls the final output amplitude.

AUTOMATIC GAIN CONTROL (AGC)

The ADMTV800 LNA has a 4-step gain control with dynamic range of 39 dB.

- The RFPGA has a dynamic gain range of 36 dB, and it is controlled by the RFAGC register. The register value is from 0x00 (minimum gain) to 0x5F (maximum gain). The RFAGC consists of an LNA and an RFPGA. The RFAGC dynamic range is 75 dB.
- Baseband gain is determined by the digital gain setting which can be read via the GVBB register.

With these two dynamic ranges (RFAGC = 75 dB and BBAGC = 54 dB), the ADMTV800 dynamic range is larger than 100 dB. For more information about the RFAGC and BBAGC, see the RFAGC Setting and BBAGC Setting sections.

The recommended output amplitude of the ADMTV800 is from 300 mV to 700 mV (peak-to-peak voltage at each I/Q output pin). At 500 mV amplitude, the ADMTV800 exhibits its best performance.

RF POWER DETECTOR AND ADJACENT RECEIVED SIGNAL STRENGTH INDICATOR (ADJRSSI)

The operating range of the RFAGC and BBAGC is divided by the take-over point (TOP). The BBPGA is controlled by the BBAGC voltage from the demodulator. The demodulator generates the BBAGC voltage by measuring I and Q signal level of the tuner output. When the RF input level is getting lower than the TOP, demodulator increases BBPGA gain by rising BBAGC voltage.

When the RF input level is higher than the TOP, the RFPGA operates. As the RF input level increases, RFPGA gain decreases. RF input level of the opposite direction makes RFPGA gain increased. In the middle of the RFPGA operation range, the LNA on/off operation occurs, and this operation expands the dynamic range of the RFAGC block.

I²C INTERFACE AND CLOCK CONTROL

The ADMTV800 uses the I²C bus interface. The serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus. Each device is recognized by a unique address and can operate as either a master or slave, depending on the function of the device.

POWER-DOWN MODES

The ADMTV800 has two power-down modes.

Software Power-Down

The ADMTV800 has a software power-down mode controlled by the SWPD registers (Address 0x2E, Address 0x2F and 0x30).

Time-Slicing Power-Down

The ADMTV800 also supports a time-slicing power-down mode. TSPD controls time-slicing power-down according to register setting (Address 0x30, Address 0x31 and Address 0x32). During time-slicing power down mode, each block can be selected to be on or off according to the register setting.

APPLICATIONS INFORMATION

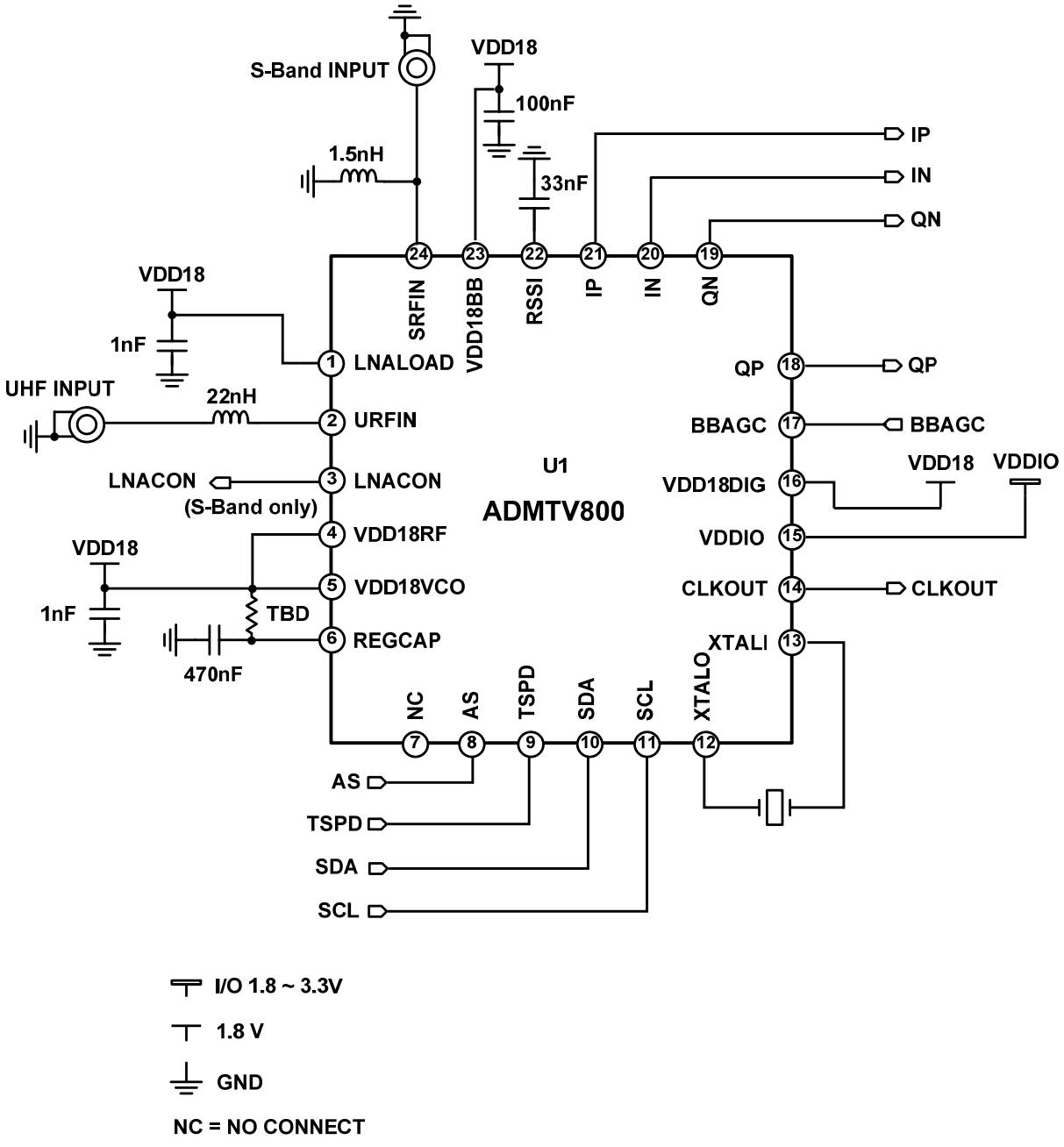


Figure 6. Typical Application Circuit for Dual Band
[4 mm x 4 mm, 24-LFCSP]

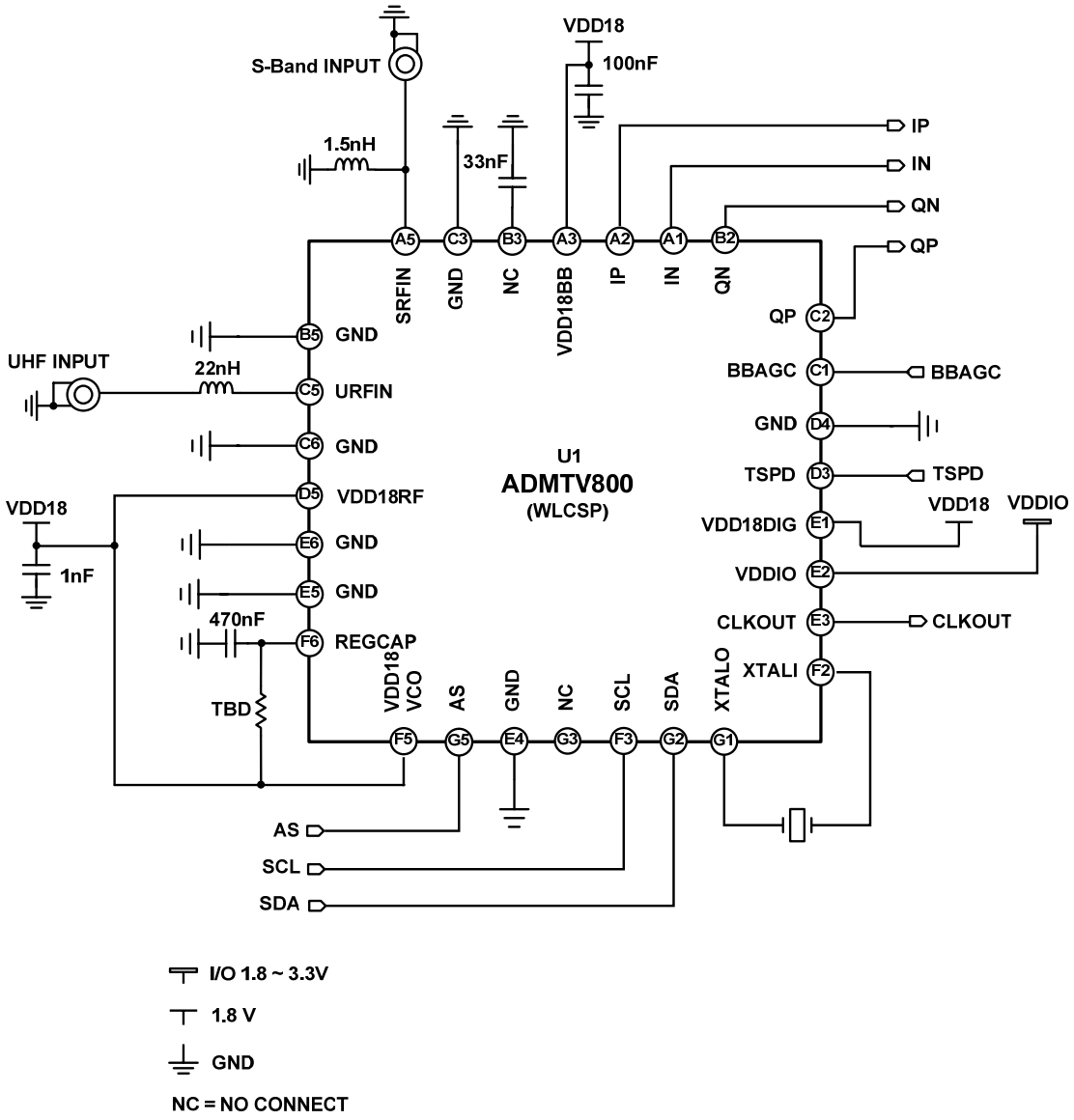


Figure 7. Typical Application Circuit for Dual Band [WLCSP]

RF INPUT STAGE

The ADMTV800 requires RF impedance matching application circuit. The RF impedance matching components should be located as close as possible to the chip (see Figure 8). RF impedance matching values can be changed to optimize RF performance.

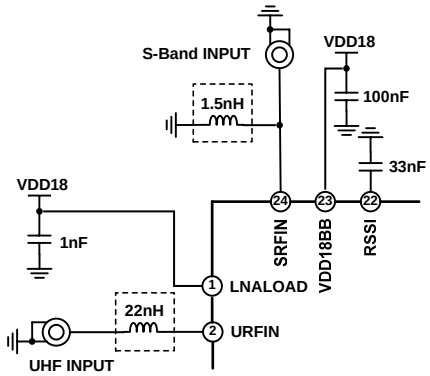


Figure8. RF Input Stage

VCO BIAS/BYPASS CAPACITORS

The ADMTV800 has integrated VCOs/PLLs for LO frequency generation. By using bypass capacitors, these VDD18 power lines should be isolated from noisy power sources. The bypass capacitor of VDD18 power rejects high frequency noise in the power supply. These bypass capacitors should be located as close as possible to chip and GND (see Figure 9).

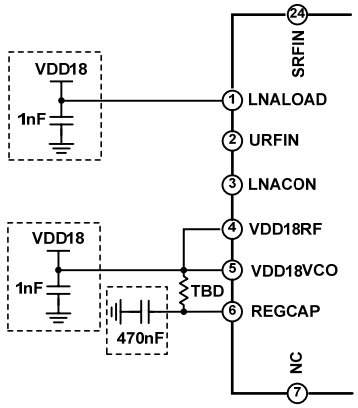


Figure9. VCO Bias/Bypass Capacitors

DIGITAL INTERFACE— SDA/SCL

The ADMTV800 is controlled by the I²C communication protocol. The serial data (SDA) and serial clock (SCL) carry information between the devices connected with the bus interface. SDA and SCL facilitate bidirectional communication between the ADMTV800 and the master at clock frequency up to 400 kHz. In addition, 10 kΩ pull-up resistors are integrated on chip for the demodulator interface (see Figure10).

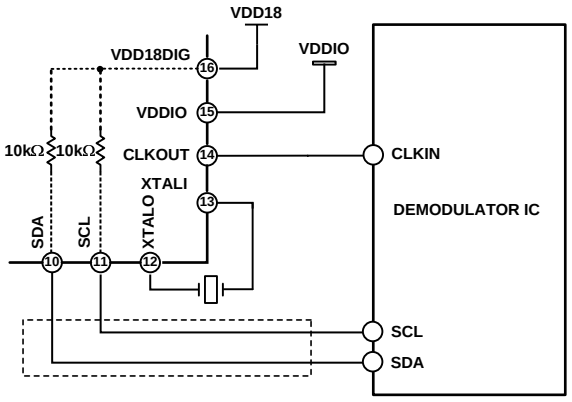


Figure10. I²C Interface

ISOLATION FROM REFERENCE CLOCK'S HARMONICS AND DIGITAL PARTS

The digital parts should be isolated from the RF input of the ADMTV800 by careful PCB design (see Figure11).

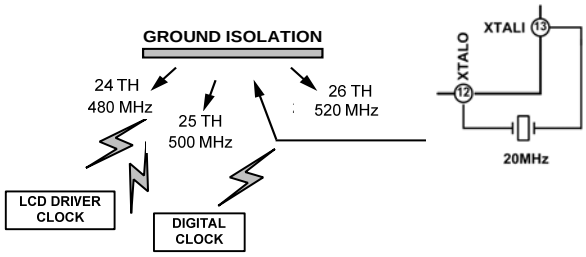


Figure11. Isolation from Noises

BBAGC INTERCONNECTIONS

The ADMTV800 supports three BBAGC modes, which are analog mode, analog PWM mode and digital PWM mode from demodulator's PWM output signal which contains gain control information without external components (see Figure 12).

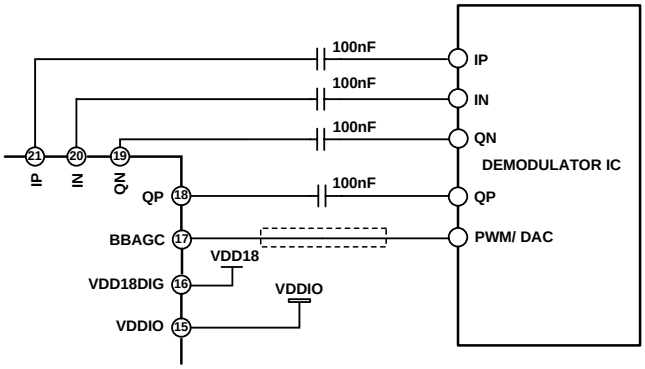


Figure12. AGC Connection

Usually demodulator has AGC block which result is expressed as 1-bit PWM type signal. However, some demodulators feed D/A converted analog signal. Most of these feedback signals are accomplished by open-collector or open-drain scheme. Nevertheless, the ADMTV800 can accompany with any type of

demodulator using PCB line connection that just enough by changing its own register setting. In the case of demodulator feedback signal is PWM signal type, the ADMTV800 has pull-up resister and internal low-pass filtering block to handle PWM feedback signal by direct connection to demodulator. According to demodulator, a PWM signal is various. For these reasons, the ADMTV800 has two PWM signal processing methods, which are digital PWM and analog PWM mode**.**

Thus, the ADMTV800 supports every PWM output signal type of demodulator without external components.

1. Digital PWM mode

The ADMTV800 has a digital moving average filter. This filter can find the wanted baseband gain control value. This mode does not require additional blocks between demodulator and ADMTV800. 1-bit PWM signal can be directly filtered out by tuning averaged data number of digital filter.

2. Analog PWM mode

Digital moving average filter only PWM signal processing can suffer from noise issues even though tuning number of averaged data. Therefore, the ADMTV800 also has internal analog low-pass filter for improving wanted baseband gain control value quality. The analog PWM mode employs cascaded analog low-pass filter and digital moving average filter. In this case, internal 8-bit A/D converter is used between analog low-pass filter and digital filter on chip. In the other case of demodulator feedback signal is Analog mode (D/A converted analog signal), by using pull-up resistor and analog buffer, the ADMTV800 can find wanted BB gain control value in case of analog type feedback signal processing. This mode does not use digital moving average filter, but analog low-pass filter and A/D converter. The mode changing is easily accomplished by register tuning.

XIN/XOUT INTERCONNECTIONS

The ADMTV800 supports crystal and temperature-controlled crystal oscillator (TCXO) for using a reference clock. When using a crystal, XTALI and XTALO pins are connected to crystal unit. A 1 MΩ feedback resistor and 8 pF load capacitors are integrated on chip. (see Figure 13).

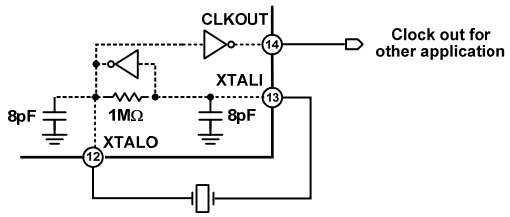


Figure13. X-TAL Application

It is highly recommended to inquire an optimized oscillator application from crystal vendors.

The stability also depends on the demodulator's carrier tracking performance.

Target Frequency (MHz)	13 ~ 40
Load Capacitor (pF) on chip	8
Maximum ESR (ohm)	TBD
Temperature Stability (ppm)	± 30

In addition, the default setting of CLKOUT port at power-on state is the crystal frequency divided by 1. For example, if the crystal frequency is 20 MHz, then clock output frequency is 20 MHz when the chip is started after just power-on state.

In case of using a temperature-controlled crystal oscillator (TCXO), it should be interfaced to the ADMTV800 via Pin XTALI with a DC block capacitor of 10 nF.

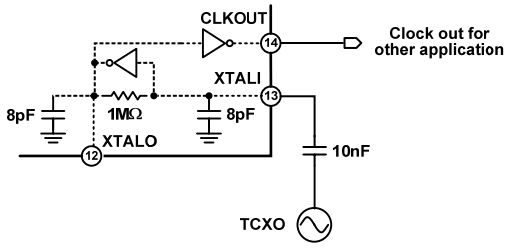


Figure14. TCXO Application

It is also highly recommended to inquire an optimized oscillator application from TCXO vendors. TCXO output amplitude must be larger than 500 mV p-p. The stability also depends on the demodulator's carrier tracking performance.

It is also noted that default frequency of CLKOUT port at power-on state is the TCXO frequency divided by 1. For example, if the TCXO frequency is 20 MHz, then clock output frequency is 20 MHz when the chip is started after just power-on state.

REFERENCE CLOCK SELECTION

ADMTV800 supports reference clocks as below. Table7 shows PLLR register selection.

Table 7. PLLR selection according to crystal oscillator

Crystal oscillator	PLLR<3:0>
13 MHz to 22 MHz	0x01
23 MHz to 40 MHz	0x10

PLL SETTING

As stated in the

Local Oscillator section, the ADMTV800 local oscillator (LO) consists of a VCO and a Σ-Δ fractional-N PLL. The ADMTV800 supports a wide range of LO frequencies as shown in Table 8. when using 20 MHz reference clock .When changing LO frequencies, users must calculate the PLLN and PLLF register values manually. The Manual PLL Setting Procedure section outlines the steps to adjust these two registers.

Table 8. Register Value Selection[1]

VCOBANDU<1:0>: VCO core frequency shift			
LO Frequency	**VCOBANDU <1:0>**	**PLLS (Dec)**	**PLLR <3:0 >**
470 MHz to 600 MHz	0x0	1	0x01
600 MHz to 940 MHz	0x3	1	0x01
2635 MHz to 2660 MHz	0x3	0.5	0x01

[1] The LO frequency is gained by dividing the PLL frequency by the division ratio according to the PLLS

Manual PLL Setting Procedure

To set the f_{LO} manually, use the following procedure:

1. Reset the tuner.
2. Select the f_{LO} to be oscillated.
3. Select the VCOBANDU<1:0> register value according to the f_{LO} selection in Table 8.
4. The PLLS value is decided by LO frequency.
5. Use the PLLR value, which has a default of 1 if you use 20 MHz reference clock.
6. Determine the PLLN and PLLF register values by calculating the following equations:

$$f_{PLL} = \frac{f_{crytal}}{PLLR} \cdot \left(PLLN + \frac{PLLF}{2^{20}} \right)$$

$$f_{LO} = \frac{f_{PLL}}{PLLS}$$

where:

PLLN is the integer divide value selected by the PLLN register.
PLLF is the fractional divide value selected by the PLLF register.

PLLR is the reference crystal frequency divide ratio selected by PLLR register.
PLLS is selected by the divide ratio between LO frequency and PLL frequency (see the PLL Setting section for more information).

Solving these equations gives one equation consisting of the PLLN and PLLF variables. PLLN is an integer value, and PLLF is a fractional value multiplied by 2^{20}.

For example, if the desired f_{LO} = 2647.5 MHz and crystal oscillator frequency = 20 MHz,

$$f_{PLL} = \frac{20\,\text{MHz} \times \left(\text{PLLN} + \left(\frac{\text{PLLF}}{2^{20}} \right) \right)}{1}$$

$$f_{LO} = \frac{f_{PLL}}{PLLS} = \frac{f_{PLL}}{0.5} = 2647.5\text{MHz}$$

$$f_{PLL} = 1323.75\text{MHz}$$

$$1323.75\ \text{MHz} = \frac{20\,\text{MHz} \times \left(PLLN + \left(\frac{PLLF}{2^{20}} \right) \right)}{1}$$

$$\frac{1323.75}{20} = \left(PLLN + \left(\frac{PLLF}{2^{20}} \right) \right)$$

$$66.1875 = PLLN + \frac{PLLF}{2^{20}}$$

The PLLN and PLLF values are as follows:

$PLLN = 66 \rightarrow PLLN = 0x42$
$PLLF = 0.1875 \times 2^{20} = 196608 \rightarrow PLLF = 0x30000$

RFAGC SETTING

The ADMTV800 has dual RF/BB AGC loops. The RF AGC loop is controlled internally, and the BB AGC loop is come from demodulator. Digitally controlled RF gain is based on internal RF power detector, ADJ RSSI value and BB PGA gain control value which comes from demodulator. RF and baseband PGA block gain can also be set manually for test purposes.

RF Gain Setting (Automatic and Manual Gain Control)

The ADMTV800 RFAGC has two gain control mode, automatic gain control and manual gain control. When RFAGCSEL<1:0> is 0x0, (This is a default setting) RFAGC operates as automatic control mode. For flexibility of RF gain control, the LNA could be controlled independently by changing RFAGCSEL<1:0>.

RFAGC SEL <1:0>	**Description**
0x0	Fully automatic RF gain control
0x1	Automatic gain control of LNA, Manually control of remained RF blocks
0x2	Manually control of LNA gain, Automatic gain control of remained RF blocks
0x3	Fully manual RF gain control

LNAGAIN_I2C<1:0> and RFAGC_I2C<6:0> express LNA gain and remained RF block gain, respectively. These manually set gains will be asserted according to the RFAGC<1:0>.

BB GAIN SETTING

For automatic gain control of BB PGA, the ADMTV800 supports three BBAGC mode, digital PWM mode, analog PWM mode and analog mode. Furthermore, the ADMTV800 can set BB PGA gain via manual gain control register setting.

Automatic BB PGA Gain Setting

By default, BB PGA is under analog PWM mode. To utilize the BBAGC demodulator feedback signal at this mode,

1. Set GVBBSEL<0> to 0x0
2. Connect the demodulator feedback of BBAGC to the ADMTV800 directly (Pin 17)

Digital PWM mode is enabled by changing BBAGCMODE_SEL<0> as '1'. There is no difference of PCB connection as changing PWM mode from analog PWM to digital PWM mode. To confront with demodulators that have open-collector or open-drain output, the ADMTV800 has internal pull-up resistors for removing external component. In this case,

1. Set GVBBSEL<0> to 0x0
2. Set R_BBAGC_PU<2:0> to the desired value. (Refer the I2C map table in detail)
3. Connect the BBAGC of demodulator feedback to the ADMTV800 directly (Pin 17)

The ADMTV800 contains analog R-C filter for analog PWM mode. R_BBAGCLPF<2:0> and C_BBAGCLPF<2:0> can tune the cut-off frequency. Specific R-C values are depicted in I2C map table.

On the other hand analog mode requires different register settings are required for handling of analog mode as follows.

1. Set GVBBSEL<0> to 0x0
2. Set SEL_BBAGCIN_AMODE<0> to 0x1 (Default setting is 0x0)
3. Connect the BBAGC of demodulator feedback to the ADMTV800 directly. (Pin 17)

Same pull-up resistors, R_BBAGC_PU<2:0> can be set according to the demodulator condition which is alike digital and analog PWM mode signal processing.

Manual Gain Setting

At first gain control mode must be changed for manual gain setting. When GVBBSEL<0> is '1' then BB PGA gain control is manual mode. Then, BB PGA gain is easily tuned by changing GVBB_I2C<7:0>.

1. Set GVBBSEL<0> to 0x1
2. Set GVBB_I2C<7:0> to the desired value (0x00 to 0xD7)

TAKE-OVER POINT (TOP) TUNING

According to the take-over point (TOP), $P_{IN,TOP}$, RF and BB AGC operation can be optimized by considering various tuner performances. If the $P_{IN,TOP}$ is decreased, tuner linearity is improved, but tuner output SNR which comes from thermal noise are degraded. When $P_{IN,TOP}$ is increased, tuner's performance vice versa. The $P_{IN,TOP}$ is defined as follows.

$$P_{IN,TOP} = P_{Dem.Goal} - G_{V,RF,Max} - G_{V,BBPGA}$$

where:

$P_{Dem.Goal}$: Wanted input signal power level of demodulator as dBm unit.

$G_{V,RF,Max}$: Maximum RF gain as dB unit.

$G_{V,BBPGA}$: BB PGA gain as dB unit.

$G_{V,RF,Max}$ value is decided by RFAGC_MAX<6:0> register setting. The ADMTV800 can generate 42dB RF gain which is the highest value. BB PGA gain, $G_{V,BBPGA}$ is directly related when manual gain control mode by tuning GVBB_I2C<7:0>. There is simple relationship between $G_{V,BBPGA}$ and BB PGA control word, GVBB<7:0>.

$$G_{V,BBPGA}[dB] = \frac{1}{4}GVBB\ <7:0> +6$$

Then, GVBB_I2C<7:0> can control BB PGA gain from 6dB to 60dB according to the equation. However, when automatic gain control mode, $G_{V,BBPGA}$ is determined by GVBBREF_H<7:0> and GVBBREF_L<7:0> registers. GVBBREF_H<7:0> and GVBBREF_L<7:0> mean a upper and a lower bound of $G_{V,BBPGA}$, respectively. If GVBB<7:0> after BB AGC loop were

$$GVBB<7:0>=\frac{GVBBREF\_H<7:0>+GVBBREF\_L<7:0>}{2}$$

then, $G_{V,BBPGA}$ can be expressed as

$$G_{V,BBPGA}\ [dB] = \frac{1}{4}\left(\frac{GVBBREF\_H<7:0>+GVBBREF\_L<7:0>}{2}\right)+6$$

Consequently, GVBBREF_H<7:0> and GVBBREF_L<7:0> register tuning can change the $P_{IN,TOP}$ point based on the addressed expression.

TSPD CONTROL SIGNAL INVERTING

The ADMTV800 time-slicing power-down (TSPD) control signal polarity can be inverted on demand of the user.

TSPDPOL<0>	Status
0x0	Normal
0x1	Inverse

POWER-DOWN CONTROL

The ADMTV800 has two power-down modes: time-slicing power-down (TSPD pin), and software power-down (SWPD register settings).

Recovery time from power-down depends on the PLL lock time and the demodulator's AGC response.

- If the TSPD pin is high and a TSPDxxx block register (Address 0x30, Address 0x31, and Address 0x32) is high, the xxx block is powered down.

- If a SWPDxxx block register is high, the xxx block register (Address 0x2E, Address 0x2F and Address 0x30) is powered down.

In case of time-slicing power-down, all blocks including the crystal oscillator block are powered down. Therefore, all digital parameters are stored as they were before power-down.

After being powered on by the TSPD pin, the tuner does not need to operate the VCO searching loop and automatic gain control.

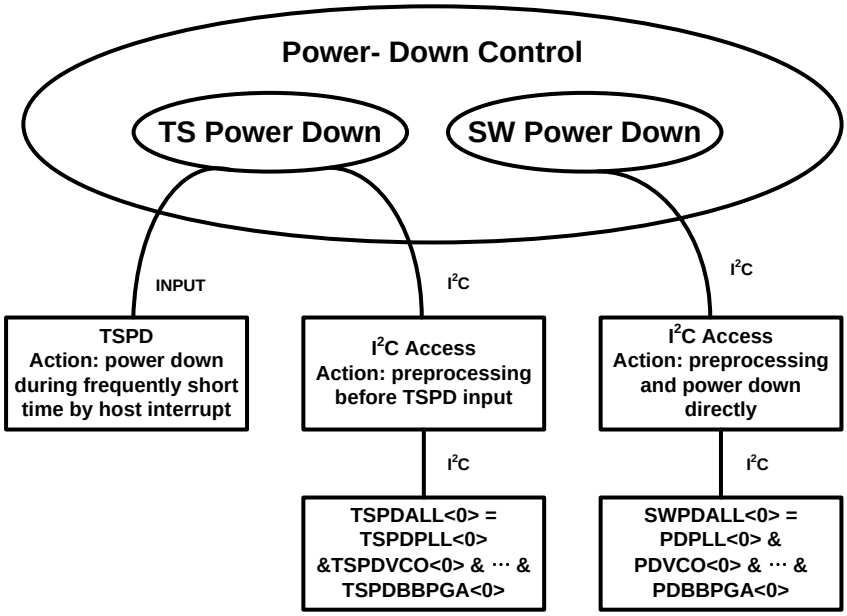


Figure15. Two Power-Down Modes

I²C OPERATION

The ADMTV800 is controlled by an I²C data bus and is compatible with both standard and fast mode formats. The data and clock are fed on the SDA and SCL lines, respectively, as defined by the I²C bus format. The device can either accept data in the write-mode, or send data in the read-mode. The LSB of the address byte sets the device into write-mode if it is low and read mode if it is high.

I²C READ/WRITE ADDRESS

Table 9. I²C Read Address

Address Select Pin (AS)	MSB							LSB	Address (Hex)
Low	1	1	0	0	0	0	1	1	0xC3
High	1	1	0	0	0	1	0	1	0xC5

Table 10. I²C Write Address

Address Select Pin (AS)	MSB							LSB	Address (Hex)
Low	1	1	0	0	0	0	1	0	0xC2
High	1	1	0	0	0	1	0	0	0xC4

I²C BUS FORMAT

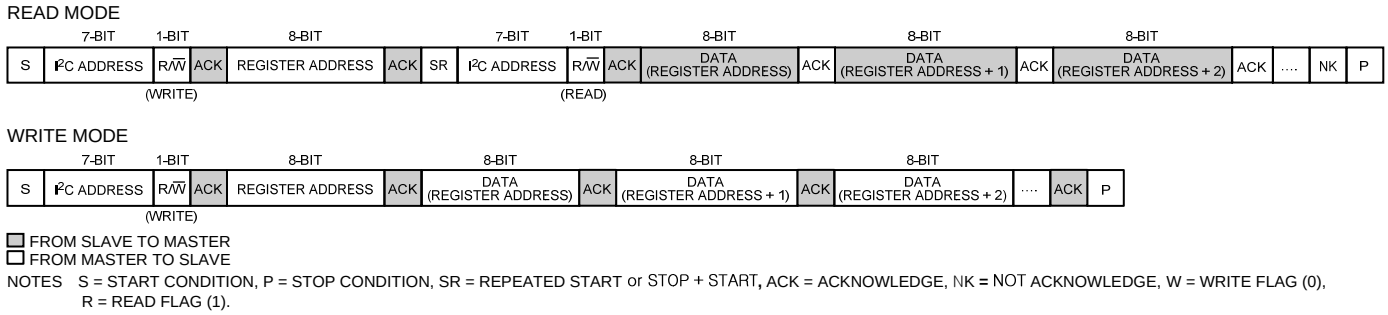
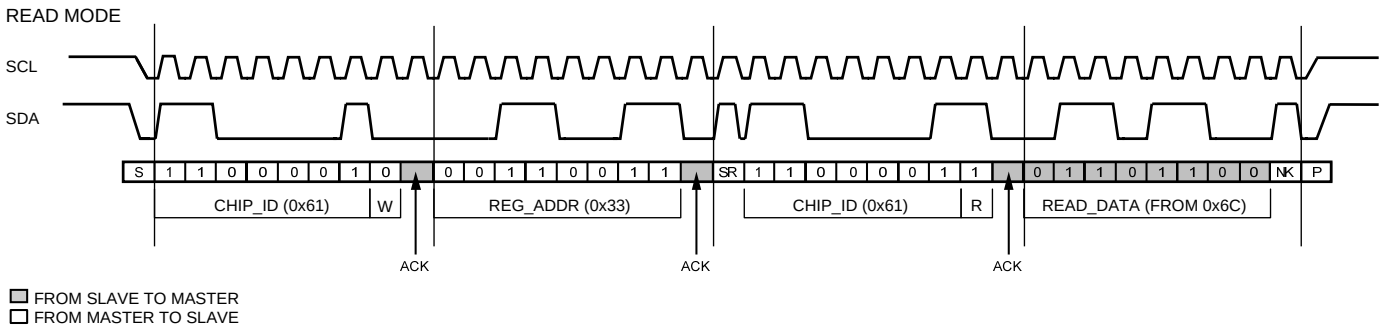


Figure 16. I²C Bus Format

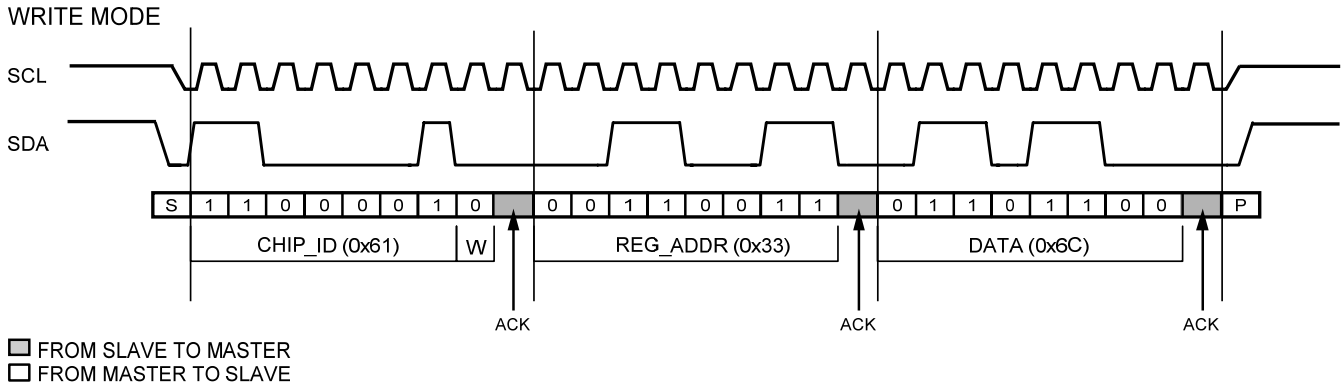
I²C TIMING CHARACTERISTICS

According to standard I²C specification, the clock frequency reaches its maximum 400 kHz in fast-mode and 100 kHz in standard-mode. To communicate with RF tuner, users need to comply with the conditions in this section.



NOTES
1. S = START CONDITION, P = STOP CONDITION, SR = REPEATED START CONDITION or STOP + START CONDITION
   ACK = ACKNOWLEDGE: ACTIVE LOW, NK = NOT ACKNOWLEDGE: ACTIVE HIGH, W = WRITE MODE, R = READ MODE.
2. ADMTV803 MEETS THE DEMANDING PERFORMANCE SPECIFICATION OF I²C COMBINED MODE. THEREFORE, UPPER ACCESS CONDITION IS ABLE TO BE MODIFIED ON STANDARD I²C.

Figure 17. Serial Control Port Read Mode



NOTES
1. S = START CONDITION, P = STOP CONDITION, ACK = ACKNOWLEDGE: ACTIVE LOW, W = WRITE MODE, R = READ MODE,
2. ADMTV803 MEETS THE DEMANDING PERFORMANCE SPECIFICATION OF I^2C COMBINED MODE. THEREFORE, UPPER ACCESS CONDITION IS ABLE TO BE MODIFIED ON STANDARD I^2C.

Figure 18. Serial Control Port Write Mode

Serial Control Port Timing

T_A = 25°C, V_{DDIO} = 2.8 V, GND = 0 V, unless otherwise noted.

Table 11. I^2C Serial Control Timing

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Hold Time (Repeat) Start Condition[1]	t_{SHD}	4.0		0.6		µs
SCL Clock Period	t_{CLK}	0	100	0	400	kHz
High Period of the SCL Clock	t_{HIGH}	4.0		0.6		µs
Low Period of the SCL Clock	t_{LOW}	4.7		1.3		µs
Setup Time for Stop Condition	t_{PSU}	4.0		0.6		µs
Data Setup Time	t_{DSU}	250		100[2]		ns
Data Hold Time for I^2C Bus Devices	t_{DHD}	5.0				µs
		0[3]	3.45[4]	0[3]	0.9[4]	

[1] After this period, the first clock pulse is generated.
[2] A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but the $t_{DSU} \geq 250$ ns requirement must then be met. This automatically occurs if the device does not stretch the low period of the SCL signal (t_{LOW}).
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
[4] The maximum t_{DHD} needs to be met only when the device does not stretch the low period of the SCL signal (t_{LOW}).

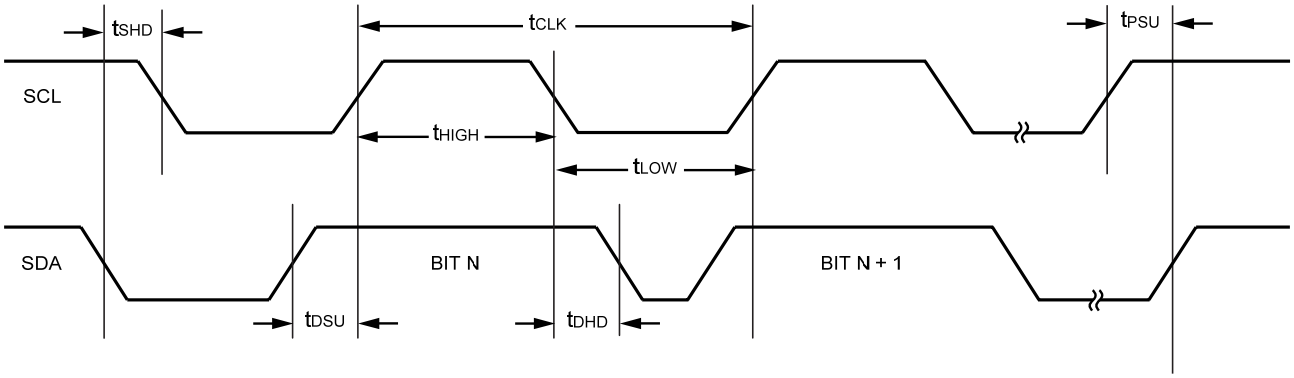


Figure 19. Serial Control Port Timing

I²C REGISTER MAP

Table 12. Register Listing

Addr (Hex)	Type	Parameter	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
0x00	R	CHIPID	CHIPID1<7:0>							
0x01	R	CHIPID0	CHIPID0<7:0>							
0x02	R	SPLITID	SPLITID<7:0>							
0x03	R	RFAGC	BLANK	RFAGC<6:0>						
0x04	R	BBAGC	GVBB<7:0>							
0x05	R	RFAGC /LNA	BLANK				CH_FLAG_OUT<1:0>		LNAGAIN<1:0>	
0x06	R	VCO	BLANK	VCORG<6:0>						
0x07	R	VCO	BLANK	CONVCOU<5:0>						LOCK
0x08	R	VCO	BLANK		CONVCOS<5:0>					
0x09	R	ADC	BLANK	RV<5:0>						CTUNE<8>
0x0A	R	CTUNE	CTUNE<7:0>							
0x0B	R	ADC	PWRDETD<7:0>							
0x0C	R	ADC	ADJRSSID<7:0>							
0x0D	R	ADC	BBAGCD<7:0>							
0x0E	R	ADC	TMPSNSD<7:0>							
0x0F	R	ADC	VTUNED<7:0>							
0x15	R	I/Q DC OFFSET	IOFS<11:8>				QOFS<7:4>			
0x21	R/W	SOFTRESETB	BLANK							SOFTRESETB
0x22	R/W	LNA	LNABAND	RESERVED						
0x23	R/W	LNA	ICONLNA_NORM<3:0>				ICONLNA_SENS<3:0>			
0x24	R/W	LNA/LPF	ICONLNA_ACR<3:0>				MODE1: CMMB 8M	MODE2: CMMB 2M	RESERVED	RESERVED
0x25	R/W	PLL	RESERVED						PLLN<9:8>	
0x26	R/W	PLL	PLLN<7:0>							
0x27	R/W	PLL	PLLF<19:12>							
0x28	R/W	PLL	PLLF<11:4>							
0x29	R/W	PLL	PLLF<3:0>				PLLR<3:0>			
0x2A	R/W	PLL/BBAGC	RST_PLL	RESERVED	RESERVED	SEL_BBAGC IN_AMODE	RESERVED	R_BBAGC_PU<2:0>		
0x2D	R/W	BBAGC	BBAGC MODE_ SEL	POL_BBAGC	ADC_BP_ SEL	RESERVED	AVGCNT_SET<3:0>			
0x2E	R/W	SWPD	SWPDLNA	SWPD EXTLNA	SWPDMIX	SWPDBB	SWPDVCO	SWPDLDO	SWPDPLL	SWPDBGR
0x2F	R/W	SWPD	SWPD PDET	SWPD ADJRSSI	SWPDADC	SWPDBBAG CANALOG	SWPD DCOSDAC	SWPDCTUNE	SWPD RTUNE	SWPD TMPSNS
0x30	R/W	SWPD/TSPD	SWPDDIG	SWPD CLKDRV	SWPDOSC	TSPDLNA	TSPD EXTLNA	TSPDMIX	TSPDBB	TSPDVCO
0x31	R/W	TSPD	TSPDLDO	TSPDPLL	TSPDBGR	TSPDPDET	TSPD ADJRSSI	TSPDADC	TSPDBBAGC ANALOG	TSPDDCOS DAC
0x32	R/W	TSPD/DIVID ER CLOCK OUTPUT	TSPD CTUNE	TSPDRTUNE	TSPDTMPSNS	TSPDDIG	TSPD CLKDRV	TSPDOSC	DIVCLKDRV<1:0>	
0x3B	R/W	MIXER/LNA	RESERVED	MIXSELBGR	MIXGAIN BOOST	RESERVED				
0x3C	R/W	MIXER/PWR. DETECTOR	CALPWD	ICONPWD<2:0>			MIXCTUNE<3:0>			

Addr (Hex)	Type	Parameter	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0
0x4A	R/W	LPF	BQC<7:0>							
0x4C	R/W	RFAGC/VCO	DETENA	ICONDIV1<2:0>			ADJENA	ICONDIV2<2:0>		
0x4D	R/W	TSPD/VCO	TSPDPOL	ICONBUF<2:0>			RESERVED	ICONTOPLL<2:0>		
0x4F	R/W	VCO	RESERVED						VCOBANDU<1:0>	
0x54	R/W	PLL	RESERVED			CP_COMP<4:0>				
0x57	R/W	RTUNE	ENRTUNE	RESERVED						
0x5B	R/W	BBAGC	GVBBSEL	RESERVED						
0x7D	R/W	LNA	LNAGAIN_I2C<1:0>		RESERVED					
0x7E	R/W	RFAGC	RFAGCSEL<1:0>		RESERVED					
0x85	R/W	BBAGC	GVBB_I2C<7:0>							
0x87	R/W	RFAGC	BLANK	RFAGC_I2C<6:0>						
0x89	R/W	PWR. DETECTOR	BLANK		PWD_DCOSDAC<5:0>					

NOTES
The RESERVED bits are not supposed to be changed.
R: Read only.
R/W: Read and Write.

DETAILED REGISTER DESCRIPTIONS

Table 13. Read Only Register

Address (Hex)	Bit(s)	Name	Description
0x00	<7:0>	CHIPID1<7:0>	Chip ID.
0x01	<7:0>	CHIPID0<7:0>	Chip ID.
0x02	<7:0>	SPLITID<7:0>	Chip split ID.
0x03	<6:0>	RFAGC<6:0>	RFAGC gain state value.
0x04	<7:0>	GVBB<7:0>	BBAGC gain control (0.25dB Step). <7:0> = 0x00: minimum gain. <7:0> = 0xD7: maximum gain.
0x05	<3:2> <1:0>	CH_FLAG_OUT<1:0> LNAGAIN<1:0>	Channel state flag output. <1:0> = 0x0: normal state. <1:0> = 0x1: sensitivity state. <1:0> = 0x2: ACR state. LNA gain state. <1:0> = 0x0: very low gain. <1:0> = 0x1: low gain. <1:0> = 0x2: middle gain. <1:0> = 0x3: high gain.
0x06	<6:0>	VCORG<6:0>	VCO varactor diode operation range (varactor switch). <6:0> = 0x00: lowest frequency of VCO oscillation. <6:0> = 0xFF: highest frequency of VCO oscillation.
0x07	<6:1> <0>	CONVCOU<5:0> LOCK<0>	Bias level in VCO bias (UHF). PLL lock indicator. <0> = 0x0: PLL is unlocked. <0> = 0x1: PLL is locked.
0x08	<5:0>	CONVCOS<5:0>	Bias level in VCO bias (S-band).
0x09	<6:1> <0>	RV<5:0> CTUNE<8>	Internal RTUNE setting value. Calculated C TUNE setting value.
0x0A	<7:0>	CTUNE<7:0>	Calculated C TUNE setting value.
0x0B	<7:0>	PWRDETD<7:0>	A-to-D converted output of power detector voltage
0x0C	<7:0>	ADJRSSID<7:0>	A-to-D converted output of ADJRSSI voltage.
0x0D	<7:0>	BBAGCD<7:0>	A-to-D converted output of BBAGC voltage after internal RC filtering.
0x0E	<7:0>	TMPSNSD<7:0>	A-to-D converted output of temperature sensor.
0x0F	<7:0>	VTUNED<7:0>	A-to-D converted output of VCO's tuning voltage .
0x15	<7:0>	IOFS<11:8> QOFS<7:4>	I/Q DC offset setting value.

Table 14. Read/Write Register

Address (Hex)	Bit(s)	Name	Description
			SOFTRESETB
0x21	<0>	SOFTRESETB<0>	RF-IC reset. Software resetb input. <0> = 0x0: resets all registers.
			LNA/MIXER
0x22	<7>	LNABAND<0>	LNA band selection. <0> = 0x0: UHF <0> = 0x1: S-band
0x3B	<6>	MIXSELBGR<0>	Mixer Bias current selection. <0> = 0x0: PTAT current <0> = 0x1: BGR current
	<5>	MIXGAINBOOST<0>	Mixer Gain manual control. <0> = 0x0: default <0> = 0x1: 6dB gain increase
0x3C	<3:0>	MIXCTUNE<3:0>	Mixer trans-impedance amplifier 1st order low pass filter capacitor tuning control. <3:0> = 0x0: BW maximum <3:0> = 0xF: BW minimum
			BASEBAND
0x24	<3>	MODE1<0>: CMMB 8M	LPF cutoff frequency selection. <0> = 0x1: Mode1 (MODE2<0> = 0x0)
	<2>	MODE2<0> : CMMB 2M	LPF cutoff frequency selection. <0> = 0x1: MODE2 (MODE1<0> = 0x0)
0x3D	<5:3>	STG2_Q_CAL<2:0>	Biquad LPF 2nd stage Q control.
	<2:0>	STG3_Q_CAL<2:0>	Biquad LPF 3rd stage Q control.
0x4A	<7:0>	BQC<7:0>	Cap. bank value after Fc tuning. This value can be changed by Fc tuning.
			VCO/PLL
0x25	<1:0>	PLLN<9:8>	PLL feedback divider integer words.
0x26	<7:0>	PLLN<7:0>	PLL feedback divider integer words.
0x27	<7:0>	PLLF<19:12>	PLL feedback divider fractional words.
0x28	<7:0>	PLLF<11:4>	PLL feedback divider fractional words.
0x29	<7:4>	PLLF<3:0>	PLL feedback divider fractional words.
	<3:0>	PLLR<3:0>	PLL reference divider integer value.
0x2A	<7>	RST_PLL<0>	PLL reset. <0>= 0x1: Reset <0>= 0x0 : Release
0x4B	<1:0>	VARCONU<1:0>	Varactor cap control for Kvco variation <1:0> = 0x0: Kvco max <1:0> = 0x3: Kvco min
0x4C	<6:4>	ICONDIV1<2:0>	Current control of div2_first (PLL & UHF & S-band path). <2:0> = 0x0: min <2:0> = 0x7: max
	<2:0>	ICONDIV2<2:0>	Current control of div2_second(S-band LO path). <2:0> = 0x0: min <2:0> = 0x7: max
0x4D	<6:4>	ICONBUF<2:0>	Current control of buf(UHF & S-band path). <2:0> = 0x0: min <2:0> = 0x7: max
	<2:0>	ICONTOPLL<2:0>	Current control of pll_buffer(PLL path).

			<2:0> = 0x0: min, <2:0> = 0x7: max
0x4F	<1:0>	VCOBANDU<1:0>	VCO core frequency range selection <1:0> = 0x0: low freq. <1:0> = 0x3: high freq.
0x54	<4:0>	CP_COMP<4:0>	In PLL loop filter, capacitor setting value for adjustable loop bandwidth
			RF POWER DETECTOR
0x3C	<7>	CALPWD<0>	Power Detector DC Offset Calibration mode. <0> = 0x0: stop calibration <0>= 0x1: calibration
0x89	<5:0>	PWD_DCOSDAC<5:0>	6-bit input of Power Detector DC offset Calibration DAC.
			BBAGC INTERFACE
0x2A	<4>	SEL_BBAGCIN_AMODE<0>	AGC input selection mode at ADC mode. <0>= 0x0 : pwm signal is connected to analog AGC LPF <0>= 0x1 : analog signal which is buffered by analog buffer is connected to analog AGC LPF
	<2:0>	R_BBAGC_PU<2:0>	Pull up resistor value control. <2:0> = 0x0 : open <2:0> = 0x1 : 10 k Ohm <2:0> = 0x2 : 7.07 k Ohm <2:0> = 0x3 : 5 k Ohm <2:0> = 0x4 : 3.5 k Ohm <2:0> = 0x5 : 2.5 k Ohm <2:0> = 0x6 : 1.77 k Ohm <2:0> = 0x7 : 1.25 k Ohm
			BBAGC
0x2D	<7>	BBAGCMODE_SEL<0>	Selection bit to determine the BBAGC mode. <0>=0x0: ADC mode <0>=0x1: PWM mode
	<6>	POL_BBAGC<0>	Polarity inverting bit of PWM input signal. <0>=0x0: Proportional PWM signal duty cycle <0>=0x1: Inverse proportional PWM signal duty cycle
	<5>	ADC_BP_SEL<0>	Selection bit. <0>=0x0: Average filter output <0>= 0x1: Bypassing ADC input when '1' asserted
	<3:0>	AVGCNT_SET<3:0>	To set the averaging date number of BBAGC average filter (Maximum value = 0xA) Number of averaged data = 2^(AVGCNT_SET + 1 + 8 * BBAGCMODE_SEL)
0x5B	<7>	GVBBSEL<0>	GVBB decoder selection bit. <0>=0x0: GVBB decoded output <0>=0x1: GVBB_I2C value
0x85	<7:0>	GVBB_I2C<7:0>	Manual setting value for GVBB.
			RF AGC
0x4C	<7>	DETENA<0>	Data enable bit to using A-to-D converted of RF power detector data for RFAGC internal calculation.
	<3>	ADJENA<0>	Data enable bit from ADJ RSSI.
0x7D	<7:6>	LNAGAIN_I2C<1:0>	Manual control LNA gain value.
0x7E	<7:6>	RFAGCSEL<1:0>	Selection bit. <1:0>=0x0: Calculated LNA gain code, Calculated RFAGC value <1:0>=0x1: Calculated LNA gain code, Manually asserted RFAGC value <1:0>=0x2: Manually asserted LNA gain code, Calcuated RFAGC value <1:0>=0x3: Manually asserted LNA gain code, Manually asserted RFAGC value
0x87	<6:0>	RFAGC_I2C<6:0>	Manual control RFAGC value.
			RTUNE
0x57	<7>	ENRTUNE<0>	Rbias resistor tuning circuit enable. <0>=0x0:disable

			<0>=0x1:enable
		CLOCK OUTPUT DRIVER	
0x32	<1:0>	DIVCLKDRV<1:0>	Divider for clock output driver. <1:0>=0x0: Output = master clock <1:0>=0x1: Output = master clock / 2 <1:0>=0x2: Output = master clock / 4
		POWER_CTRL	
0x23	<7:4>	ICONLNA_NORM<3:0>	UHF & S-band LNA current control bits of normal mode operation.
	<3:0>	ICONLNA_SENS<3:0>	UHF & S-band LNA current control bits of sensitivity mode operation.
0x24	<7:4>	ICONLNA_ACR<3:0>	UHF & S-band LNA current control bits of ACR mode operation.
		SOFTWARE POWER DOWN	
0x2E	<7>	SWPDLNA<0>	Software power down of LNA. <0>=0x0: power on <0>=0x1: power down
	<6>	SWPDEXTLNA<0>	Software power down of external LNA. <0>=0x0: power on <0>=0x1: power down
	<5>	SWPDMIX<0>	Software power down of mixer. <0>=0x0: power on <0>=0x1: power down
	<4>	SWPDBB<0>	Software power down of baseband. <0>=0x0: power on <0>=0x1: power down
	<3>	SWPDVCO<0>	Software power down of VCO. <0>=0x0: power on <0>=0x1: power down
	<2>	SWPDLDO<0>	Software power down of LDO. <0>=0x0: power on <0>=0x1: power down
	<1>	SWPDPLL<0>	Software power down of PLL. <0>=0x0: power on <0>=0x1: power down
	<0>	SWPDBGR<0>	Software power down of BGR. <0>=0x0: power on <0>=0x1: power down
0x2F	<7>	SWPDPDET<0>	Software power down of RF power detector. <0>=0x0: power on <0>=0x1: power down
	<6>	SWPDADJRSSI<0>	Software power down of ADJRSSI. <0>=0x0: power on <0>=0x1: power down
	<5>	SWPDADC<0>	Software power down of ADC. <0>=0x0: power on <0>=0x1: power down
	<4>	SWPDBBAGCANALOG<0>	Software power down of BBAGC analog part. <0>=0x0: power on <0>=0x1: power down
	<3>	SWPDDCOSDAC<0>	Software power down of DC offset DAC. <0>=0x0: power on <0>=0x1: power down
	<2>	SWPDCTUNE<0>	Software power down of CTUNE. <0>=0x0: power on <0>=0x1: power down
	<1>	SWPDRTUNE<0>	Software power down of RTUNE. <0>=0x0: power on

			<0>=0x1: power down
	<0>	SWPDTMPSNS<0>	Software power down of temperature sensor. <0>=0x0: power on <0>=0x1: power down
0x30	<7>	SWPDDIG<0>	Software power down of digital (clock gating). <0>=0x0: power on <0>=0x1: power down
	<6>	SWPDCLKDRV	Software power down of clock driver. <0>=0x0: power on <0>=0x1: power down
	<5>	SWPDOSC	Software power down of crystal oscillator. <0>=0x0: power on <0>=0x1: power down
			TIME-SLICING POWER DOWN
0x30	<4>	TSPDLNA<0>	Time-slicing power down of LNA. <0>=0x0: power on <0>=0x1: power down
	<3>	TSPDEXTLNA<0>	Time-slicing power down of external LNA. <0>=0x0: power on <0>=0x1: power down
	<2>	TSPDMIX<0>	Time-slicing power down of mixer. <0>=0x0: power on <0>=0x1: power down
	<1>	TSPDBB<0>	Time-slicing power down of baseband. <0>=0x0: power on <0>=0x1: power down
	<0>	TSPDVCO<0>	Time-slicing power down of VCO. <0>=0x0: power on <0>=0x1: power down
0x31	<7>	TSPDLDO<0>	Time-slicing power down of LDO. <0>=0x0: power on <0>=0x1: power down
	<6>	TSPDPLL<0>	Time-slicing power down of PLL. <0>=0x0: power on <0>=0x1: power down
	<5>	TSPDBGR<0>	Time-slicing power down of BGR. <0>=0x0: power on <0>=0x1: power down
	<4>	TSPDPDET<0>	Time-slicing power down of RF power detector. <0>=0x0: power on <0>=0x1: power down
	<3>	TSPDADJRSSI<0>	Time-slicing power down of ADJRSSI. <0>=0x0: power on <0>=0x1: power down
	<2>	TSPDADC<0>	Time-slicing power down of ADC. <0>=0x0: power on <0>=0x1: power down
	<1>	TSPDBBAGCANALOG<0>	Time-slicing power down of BBAGC analog part. <0>=0x0: power on <0>=0x1: power down
	<0>	TSPDDCOSDAC<0>	Time-slicing power down of DC offset DAC <0>=0x0: power on <0>=0x1: power down
0x32	<7>	TSPDCTUNE<0>	Time-slicing power down of CTUNE. <0>=0x0: power on

			<0>=0x1: power down
	<6>	TSPDRTUNE<0>	Time-slicing power down of RTUNE. <0>=0x0: power on <0>=0x1: power down
	<5>	TSPDTMPSNS<0>	Time-slicing power down of temperature sensor. <0>=0x0: power on <0>=0x1: power down
	<4>	TSPDDIG<0>	Time-slicing power down of digital (clock gating). <0>=0x0: power on <0>=0x1: power down
	<3>	TSPDCLKDRV<0>	Time-slicing power down of clock driver. <0>=0x0: power on <0>=0x1: power down
	<2>	TSPDOSC<0>	Time-slicing power down of crystal oscillator. <0>=0x0: power on <0>=0x1: power down
0x4D	<7>	TSPDPOL<0>	TSPD polarity change. 0 : normal. 1 : inverse. <0>=0x0: normal <0>=0x1: inverse

NOTES
R: Read only.
R/W: Read and Write.

OUTLINE DIMENSIONS

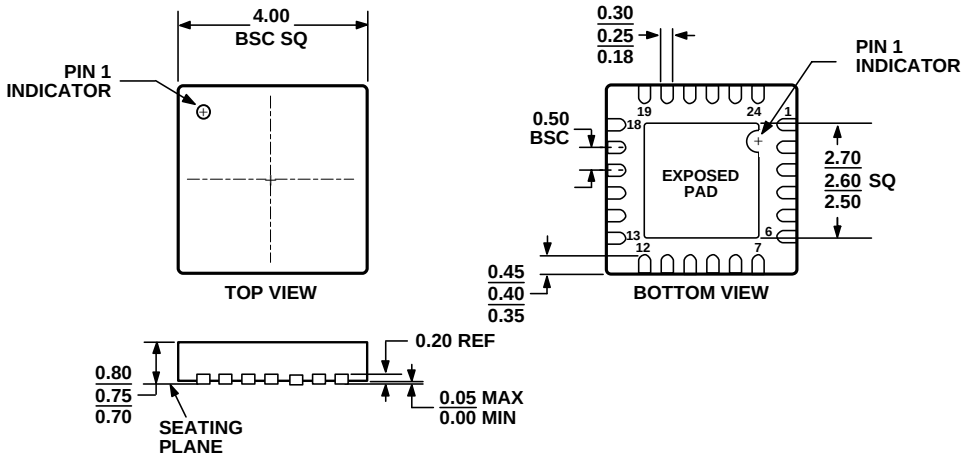
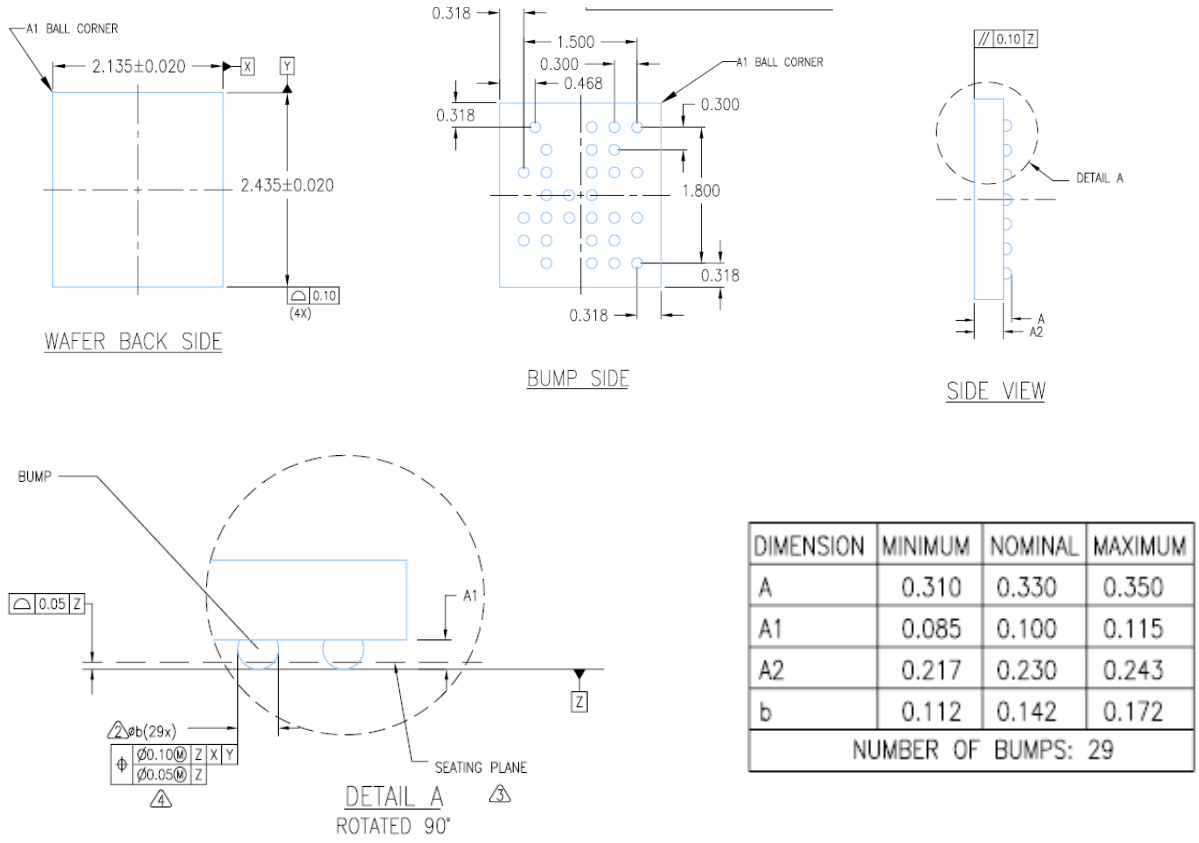


Figure 20. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body Dimensions
shown in millimeters



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.310	0.330	0.350
A1	0.085	0.100	0.115
A2	0.217	0.230	0.243
b	0.112	0.142	0.172
NUMBER OF BUMPS: 29			

Figure 21. 29-Bump Wafer Level Chip Scale Package [WLCSP]
2.135 mm × 2.435 mm Body Dimensions
shown in millimeters

ORDERING GUIDE [TBD]