

SUMMARY

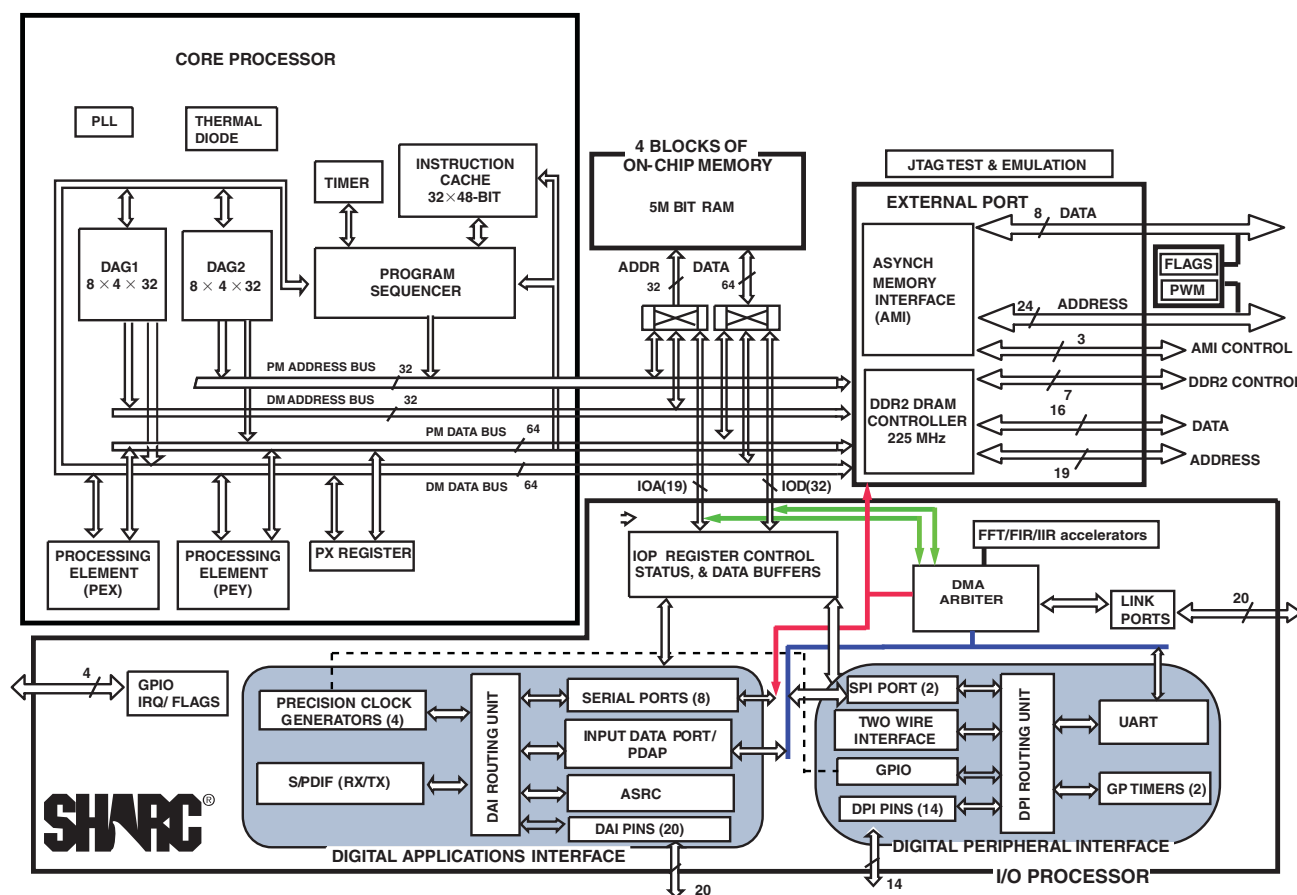
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High performance 32-bit/40-bit floating point processor
optimized for high performance audio processing
Single-instruction, multiple-data (SIMD) computational
architecture

On-chip memory—5 Mbits of on-chip RAM

Code compatible with all other members of the SHARC family
The ADSP-21469 is available with a 450 MHz core instruction
rate with unique audiocentric peripherals such as the digital
applications interface, serial ports, precision clock
generators, S/PDIF transceiver, asynchronous sample rate
converters, input data port, and more.

For complete ordering information, see [Ordering Guide on Page 55](#).



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Figure 1. Functional Block Diagram

Rev. PrA

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KEY FEATURES—PROCESSOR CORE

At 450 MHz core instruction rate, the ADSP-21469 performs at 2.7 GFLOPS/900 MMACs

5 Mbits on-chip, RAM for simultaneous access by the core processor and DMA

DDR2 DRAM interface (16-bit) operating at maximum frequency of half the core clock frequency

Dual data address generators (DAGs) with modulo and bit-reverse addressing

Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing

VISA (variable instruction size) execution support

Single instruction multiple data (SIMD) architecture provides:

- Two computational processing elements
- Concurrent execution
- Code compatibility with other SHARC family members at the assembly level

Parallelism in buses and computational units allows:

- Single cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch

Transfers between memory and core at a sustained 7.2 Gbytes/second bandwidth at 450 MHz core instruction rate

FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention

FIR/IIR accelerators perform dedicated FIR/IIR filtering with high-performance, fixed- and floating-point processing capabilities

In the ADSP-21469, the program sequencer can execute code directly from external memory bank 0 (SRAM, as well as DDR2 DRAM). This allows more options to a user in terms of code and data storage.

New opcodes of 16 and 32 bits are supported in addition to the existing 48 bit opcodes. Variable Instruction Set Architecture (VISA) execution from external DDR2 DRAM memory is also supported.

INPUT/OUTPUT FEATURES

Two 8-bit wide link ports can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional programmable ports having eight data lines, an acknowledge line and a clock line. Link ports can operate at a maximum frequency of 166 MHz.

DMA controller supports:

- 36 DMA channels for transfers between ADSP-21469 internal memory and a variety of peripherals
- DMA transfers at peripheral clock speed, in parallel with full-speed processor execution

External port provides glueless connection to 16-bit wide synchronous DDR2 DRAM using a dedicated DDR2 DRAM controller, and 8-bit wide asynchronous memory devices using asynchronous memory interface (AMI)

Programmable wait state options (for AMI): 2 to 31 DDR2_CLK cycles

Delay-line DMA engine maintains circular buffers in external memory with tap/offset based reads

16-bit data access for synchronous DDR2 DRAM memory at 450 MHz

8-bit data access for asynchronous memory at 75 MHz (Max)

4 memory select lines allows multiple external memory devices

Digital audio interface (DAI) includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, and a signal routing unit

Digital peripheral interface (DPI) includes, two timers, one UART, and two SPI ports, and a two-wire interface port

Outputs of PCG's A and B can be routed through DAI pins

Outputs of PCG's C and D can be driven on to DAI as well as DPI pins

Eight dual data line serial ports that operate at up to 56.25 Mbps on each data line — each has a clock, frame sync, and two data lines that can be configured as either a receiver or transmitter pair

TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110

Up to 16 TDM stream support, each with 128 channels per frame

Companding selection on a per channel basis in TDM mode

Input data port (IDP), configurable as eight channels of serial data or seven channels of serial data and up to a 20-bit wide parallel data channel

Signal routing unit provides configurable and flexible connections between the various peripherals and the DAI/DPI components

4 independent asynchronous sample rate converters (ASRC). Each converter has separate serial input and output ports, a de-emphasis filter providing up to -128 dB SNR performance, stereo sample rate converter and supports left-justified, I2S, TDM, and right-justified modes and 24-, 20-, 18-, and 16-audio data word lengths.

2 muxed flag/IRQ lines

1 muxed flag/IRQ /MS pin

1 muxed flag/Timer expired line /MS pin

S/PDIF-compatible digital audio receiver/transmitter supports EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards

Left-justified, I2S or right-justified serial data input with 16-, 18-, 20- or 24-bit word widths (transmitter)

Pulse-width modulation provides:

- 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms

PLL has a wide variety of software and hardware multiplier/divider ratios

Thermal diode to monitor die temperature

Available in 19 mm by 19 mm PBGA package (see [Ordering Guide on Page 55](#))

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GENERAL DESCRIPTION

The ADSP-21469 SHARC processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The ADSP-21469 is source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. However, the enhanced modify instruction of ADSP-21469 has a different opcode as compared to previous SHARCs. The ADSP-21469 is a 32-bit/40-bit floating point processors optimized for high performance audio applications with its large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1. ADSP-21469 SHARC Features

Feature	Description
Frequency	450 MHz
Core	5-stage pipeline
Internal RAM	5 Mbits
DDR2 Memory Interface	max half core frequency
DDR2 Memory Bus Width	16-bits
Direct DMA from SPORTs to external memory	Yes
FIR/IIR/FFT accelerators	Yes
IDP	Yes
Serial Ports	8
ASRC (channels)	8
UART	1
DAI and DPI	20/14 pins
Link ports	2
S/PDIF transceiver	1
AMI interface with 8-bit support	Yes
SPI	2
TWI	Yes
Package	324-ball, 19 mm x 19 mm PBGA

As shown in the functional block diagram on Page 1, the ADSP-21469 uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the ADSP-21469 processor achieves an instruction cycle time of 2.22 ns at 450 MHz. With its SIMD computational hardware, the ADSP-21469 can perform 2.7 GFLOPS running at 450 MHz.

Table 2 shows performance benchmarks for the ADSP-21469.

Table 2. ADSP-21469 Benchmarks (at 450 MHz)

Benchmark Algorithm	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	20.44 μ s
FIR Filter (per Tap) ¹	1.11 ns
IIR Filter (per Biquad) ¹	4.43 ns
Matrix Multiply (Pipelined)	
$[3 \times 3] \times [3 \times 1]$	10.0 ns
$[4 \times 4] \times [4 \times 1]$	17.78 ns
Divide (y/x)	6.67 ns
Inverse Square Root	10.0 ns

¹ Assumes two files in multichannel SIMD mode

The ADSP-21469 continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram of the ADSP-21469 on Page 1 illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Two programmable interval timers with external event counter capabilities
- On-chip SRAM
- JTAG test access port

The block diagram of the ADSP-21469 on Page 1 also illustrates the following architectural features:

- DMA controller
- Digital applications interface that includes four precision clock generators (PCG), an S/PDIF-compatible digital audio receiver/transmitter with four independent asynchronous sample rate converters, an input data port (IDP) with eight serial ports, eight serial interfaces, a 20-bit parallel input port (PDAP), and a flexible signal routing unit (DAI SRU).

- Digital peripheral interface that includes two timers, one UART, two serial peripheral interfaces (SPI), a 2-wire interface (TWI), and a flexible signal routing unit (DPI SRU).

FAMILY CORE ARCHITECTURE

The ADSP-21469 is code compatible at the assembly level with the ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21469 shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x SIMD SHARC processors, as detailed in the following sections.

SIMD Computational Engine

The ADSP-21469 contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the ADSP-21469 enhanced Har-

vard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21469 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see [Figure 1 on page 1](#)). With the ADSP-21469's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21469 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-21469's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21469 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21469 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture

In addition to supporting the standard 48-bit instructions from previously existing SHARC family of processors, the ADSP-21469 will support new instructions of 16 and 32 bits in addition to the existing 48 bit instructions. This feature, called Variable Instruction Size Architecture (VISA), is based on dropping redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer will now support fetching these 16-bit and 32-bit instructions as well in addition to the standard 48-bit instructions, both from internal as well as external memory. Source modules will need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

FFT Accelerator

FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention.

FIR/IIR Accelerators

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

MEMORY

The ADSP-21469 adds the following architectural features to the SIMD SHARC family core.

On-Chip Memory

The ADSP-21469 contains 5 Mbits of internal RAM. Each block can be configured for different combinations of code and data storage (see [Table 3 on Page 6](#)). Each memory block supports

single-cycle, independent accesses by the core processor and I/O processor. The ADSP-21469 memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The ADSP-21469's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory map in [Table 3](#) displays the internal memory address space of the ADSP-21469.

Table 3. ADSP-21469 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	Extended Precision Normal or Instruction Word (48 bits)	Normal Word (32 bits)	Short Word (16 bits)
BLOCK 0 RAM 0x0004 9000–0x0004 EFFF	BLOCK 0 RAM 0x0008 C000–0x0009 3FFF	BLOCK 0 RAM 0x0009 2000–0x0009 DFFF	BLOCK 0 RAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0005 8FFF	Reserved 0x0009 E000–0x000B 1FFF	Reserved 0x0009 E000–0x000B 1FFF	Reserved 0x0013 C000–0x0016 3FFF
BLOCK 1 RAM 0x0005 9000–0x0005 EFFF	BLOCK 1 RAM 0x000A C000–0x000B 3FFF	BLOCK 1 RAM 0x000B 2000–0x000B DFFF	BLOCK 1 RAM 0x0016 4000–0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 3FFF	BLOCK 2 RAM 0x000C 0000–0x000C 5554	BLOCK 2 RAM 0x000C 0000–0x000C 7FFF	BLOCK 2 RAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 3FFF	BLOCK 3 RAM 0x000E 0000–0x000E 5554	BLOCK 3 RAM 0x000E 0000–0x000E 7FFF	BLOCK 3 RAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

The 48-bit space section describes what this address range looks like to an instruction that retrieves 48 bit memory.

The 32-bit section describes what this address range looks like to an instruction that retrieves 32 bit memory.

EXTERNAL MEMORY

The external port on the ADSP-21469 SHARC provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers: the 16-bit DDR2 DRAM controller for connection of industry-standard synchronous DRAM devices, while the second is an 8-bit asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non DDR2 DRAM external memory address space is shown in [Table 4](#).

External Memory Execution

In the ADSP-21469, the program sequencer can execute code directly from external memory bank 0 (SRAM, as well as DDR2 DRAM). This allows more options to a user in terms of code and data storage. With external execution, programs run at slower speeds since 48-bit instructions are fetched in parts from a 16-bit external bus coupled with the inherent latency of fetching instructions from DDR2 DRAM. VISA mode and SIMD mode accesses are supported for DDR2 space. However, external memory execution from DDR2 space is different for VISA and non-VISA mode. Fetching instructions from external memory generally takes 1.5 peripheral clock cycles per instruction.

DDR2 Support

The ADSP-21469 supports a 16-bit DDR interface operating at a maximum frequency of half the core clock. Execution from external memory is supported. External memory up to 2 Gbits can be supported. Delay line DMA functionality supported.

DDR2 DRAM Controller

The DDR2 DRAM controller provides an 16-bit interface to up to four separate banks of industry-standard DDR2 DRAM devices. Fully compliant with the DDR2 DRAM standard, each bank can have its own memory select line (DDR2_CS3-DDR2_CS0), and can be configured to contain between 32M bytes and 256M bytes of memory. DDR2 DRAM external memory address space is shown in [Table 5](#).

A set of programmable timing parameters is available to configure the DDR2 DRAM banks to support memory devices.

Table 4. External Memory for Non DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000 – 0x00FF FFFF
Bank 1	16M	0x0400 0000 – 0x04FF FFFF
Bank 2	16M	0x0800 0000 – 0x08FF FFFF
Bank 3	16M	0x0C00 0000 – 0x0CFF FFFF

Table 5. External Memory for DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap. In case of 32-bit wide external memory, two 48-bit instructions will be stored in three 32-bit wide memory locations. For example, if 2k instructions are placed in 32-bit wide external memory starting at the bank 0 normal-word base address 0x0030 0000 (corresponding to instruction address 0x0020 0000) and ending at address 0x0030 0BFF (corresponding to instruction address 0x0020 07FF), then data buffers can be placed starting at an address that is offset by 3k 32-bit words (for example, starting at 0x0030 0C00).

Asynchronous Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

The asynchronous memory controller is capable of a maximum throughput of TBD Mbps using a TBD MHz external bus speed. Other features include 8 to 32-bit packing and unpacking, booting from bank select 1, and support for delay line DMA.

Shared External Memory

The ADSP-21469 processor supports connecting to common shared external DDR2 memory with other ADSP-21469 processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to TBD processors.

Bus arbitration is accomplished through the $\overline{BR6}$ -I signals and the priority scheme for bus arbitration is determined by the setting of the RPBA pin. [Table 6 on Page 12](#) provides descriptions of the pins used in multiprocessor systems.

INPUT/OUTPUT FEATURES

The ADSP-21469 I/O processor provides 36 channels of DMA, as well as an extensive set of peripherals. These include a 20 lead digital applications interface, which controls:

- Eight serial ports
- S/PDIF receiver/transmitter
- Four precision clock generators
- Input data port/parallel data acquisition port
- Four asynchronous sample rate converters

The ADSP-21469 processor also contains a 14 lead digital peripheral interface, which controls:

- Two general-purpose timers
- Two serial peripheral interfaces
- One universal asynchronous receiver/transmitter (UART)
- An I²C[®]-compatible 2-wire interface
- Two PCGs (C and D) can also be routed through DPI

DMA Controller

The ADSP-21469's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21469's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Thirty-six channels of DMA are available on the ADSP-21469, 16 via the serial ports, eight via the input data port, two for the UART, two for the SPI interface, two for the external port, two for memory-to-memory transfers, two for the link port, two for the FFT/IIR/FIR accelerator.

Programs can be downloaded to the ADSP-21469 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-21469 processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The ADSP-21469 processor provides scatter/gather DMA functionality.

This allows processor DMA reads/writes to/from non-contiguous memory blocks.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DSP DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in [Figure 1](#).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes eight serial ports, four precision clock generators (PCG), S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the ADSP-21469 core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the ADSP-21469's serial ports.

Serial Ports

The ADSP-21469 features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 56.25 Mbps. Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I²S mode
- Packed I²S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I²S protocols (I²S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I²S channels (using two stereo devices) per serial port, with a maximum of up to 32 I²S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I²S modes, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ -law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter and Synchronous/Asynchronous Sample Rate Converter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphasic encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I²S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

The sample rate converter (ASRC) contains four ASRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The ASRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-21469 SHARC processor contains two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the ADSP-21469 SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21469 SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The ADSP-21469 SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The ADSP-21469 processor provides a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from ($f_{\text{PCLK}}/1,048,576$) to ($f_{\text{PCLK}}/16$) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, auto-baud detection is supported.

Timers

The ADSP-21469 has a total of three timers: a core timer that can generate periodic software interrupts and two general purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables both general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I²C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

Link Ports

Two 8-bit wide link ports can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional ports having eight data lines, an acknowledge line and a clock line. Link ports can operate at a maximum frequency of 166 MHz.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-21469 boots at system power-up from an 8-bit EPROM via the external port, link port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOTCFG2–0) pins (see [Table 8 on Page 15](#)).

The “Running Reset” feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and DDR2 DRAM controller, or performing a Boot. The functionality of the CLKOUT/RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the *ADSP-21469 SHARC Processor Hardware Reference* for the ADSP-21469 Processors.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}), external (V_{DD_EXT}), and analog (V_{DD_A}/V_{SS_A}) power supplies. The internal and analog supplies must meet the V_{DD_INT} specification for the 450 MHz device. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (V_{DD_A}) powers the processor’s internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the V_{DD_A} pin. Place the filter components as close as possible to the V_{DD_A}/V_{SS_A} pins. For an example circuit, see [Figure 2](#). (A recommended ferrite chip is the muRata BLM18AG102SN1D). To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and V_{SS} . Use wide traces to connect the bypass capacitors to the analog power (V_{DD_A}) and ground (V_{SS_A}) pins. Note that the V_{DD_A} and V_{SS_A} pins

specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the V_{SS_A} pin should connect directly to digital ground (V_{SS}) at the chip.

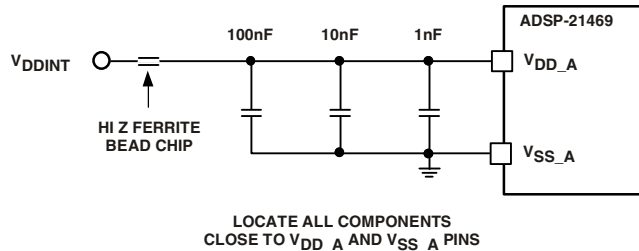


Figure 2. Analog Power (V_{DD_A}) Filter Circuit

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21469 processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-21469 processor is supported with a complete set of CROSSCORE[®] software and hardware development tools, including Analog Devices emulators and VisualDSP++[®] development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21469 processor.

EZ-KIT Lite Evaluation Board

For evaluation of the processors, use the EZ-KIT Lite[®] board being developed by Analog Devices. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and com-

mands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite[®] evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++[®] development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a stand-alone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, non-intrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21469 architecture and functionality. For detailed information on the ADSP-21469 family core architecture and instruction set, refer to the *ADSP-21469 SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of [Table 6](#):

A = asynchronous, I = input, O = output, S = synchronous,
(A/D) = active drive, (O/D) = open drain, and T = three-state,
(pd) = pull-down resistor, (pu) = pull-up resistor.

Table 6. Pin List

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
AMI_ADDR ₂₃₋₀	O/T	✓		High-Z/ driven low (boot)	External Address. The ADSP-21469 outputs addresses for external memory and peripherals on these pins. The data pins can be multiplexed to support the PDAP (I) and PWM (O). After reset, all AMI_ADDR ₂₃₋₀ pins are in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the AMI_ADDR ₂₃₋₀ pins for parallel input data.
AMI_DATA ₇₋₀	I/O/T	✓		High-Z	External Data. The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I), FLAGS (I/O) and PWM (O). After reset, all AMI_DATA pins are in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the AMI_DATA ₃₁₋₈ pins for parallel input data.
DAI_P ₂₀₋₁	I/O with fixed weak pull-up on input path ^{1,2}	✓		High-Z	Digital Applications Interface Pins. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P ₂₀₋₁ pins.
DPI_P ₁₄₋₁	I/O with fixed weak pull-up only on input path ^{1,2}	✓		High-Z	Digital Peripheral Interface. These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P ₁₄₋₁ pins.
AMI_ACK	I (pu)	✓			Memory Acknowledge (AMI_ACK). External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
AMI_RD	O/T	✓		High-Z	AMI Port Read Enable. AMI_RD is asserted whenever the ADSP-21469 reads a word from external memory. AMI_RD has fixed internal pull-up resistor ^{1,2} .
AMI_WR	O/T	✓		High-Z	External Port Write Enable. AMI_WR is asserted when the ADSP-21469 writes a word to external memory. AMI_WR has fixed internal pull-up resistor ^{1,2} .
DDR2_ADDR ₁₈₋₀	O/T		✓	High-Z/ Driven low	DDR2 Address pins. Connect in following sequence to the DDR2: Addr [18]–BA2, Addr [17]–BA1, Addr [16]–BA0, Addr [15:0]–Addr [15:0]. Unused pin may be left floating.
DDR2_CAS	O/T		✓	High-Z/ Driven high	DDR2 Column Address Strobe. Connect to <u>DDR2_CAS</u> pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CKE	O/T		✓	High-Z/ Driven low	DDR2 Clock Enable Output to DDR2. Active high signal. Connect to DDR2 CKE signal.

Table 6. Pin List (Continued)

Name	Type	LVTTTL	SSTL18	State During and After Reset	Description
DDR2_CS ₃₋₀	O/T		✓	High-Z/ Driven high	DDR2 Chip Select. All commands are masked when $\overline{\text{DDR2_CS}}_{3-0}$ is driven high. $\overline{\text{DDR2_CS}}_{3-0}$ are decoded emory address lines. Each $\overline{\text{DDR2_CS}}_{3-0}$ lines select the corresponding bank.
DDR2_DATA ₁₅₋₀	I/O/T		✓	High-Z	DDR2 Data In/Out. Connect to corresponding DDR2_DATA pins.
DDR2_DM ₁₋₀	O/T		✓	High-Z/ Driven high	DDR2 Input Data Mask. Mask for the DDR2 write data if driven high. Sampled on both edges of DDR2_DQS at DDR2 side. DM0 corresponds to DDR2_DATA [7:0] and DM1 corresponds to DDR2_DATA [15:8].
DDR2_DQS ₁₋₀ $\overline{\text{DDR2_DQS}}_{1-0}$	I/O/T (Differential)		✓	High-Z	Data Strobe. Output with Write Data. Input with Read Data. DQS0 corresponds to DDR2_DATA [7:0] and DQS1 corresponds to DDR2_DATA [15:8]
DDR2_RAS	O/T		✓	High-Z/ Driven high	DDR2 Row Address Strobe. Connect to DDR2_RAS pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_WE	O/T		✓	High-Z/ Driven high	DDR2 Write Enable. Connect to DDR2_WE pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform
DDR2_CLK0, $\overline{\text{DDR2_CLK}}_0$, DDR2_CLK1, $\overline{\text{DDR2_CLK}}_1$	O/T (Differential)		✓	High-Z/ driven low	DDR2 Clock. Free running, minimum frequency not guaranteed during reset.
DDR2_ODT	O/T		✓	High-Z/ Driven low	DDR2 On Die Termination. ODT pin when driven high (along with other requirements) enables the DDR2 termination resistances.
MS ₀₋₁	O/T	✓		High-Z	Memory Select Lines 0–1. These lines are asserted (low) as chip selects for the corresponding banks of external memory on the AMI interface. The $\overline{\text{MS}}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{\text{MS}}_1$ pin can be used in EPORT/FLASH boot mode. For more information, see the <i>ADSP-21469 SHARC Processor Hardware Reference for the ADSP-21469 Processors</i> .
FLAG[0]/IRQ0	I/O	✓		High-Z	FLAG0/Interrupt Request0.
FLAG[1]/IRQ1	I/O	✓		High-Z	FLAG1/Interrupt Request1.
FLAG[2]/IRQ2/MS2	I/O	✓		High-Z	FLAG2/Interrupt Request2/Async Memory Select2.
FLAG[3]/TIMEX P/ MS3	I/O	✓		High-Z	FLAG3/Timer Expired/Async Memory Select3.
LDAT0[7:0] LDAT1[7:0]	I/O	✓		High-Z	Link Port Data (Link Ports 0-1).
LCLK0 LCLK1	I/O	✓		High-Z	Link Port Clock (Link Ports 0-1).
LACK0 LACK1	I/O	✓		High-Z	Link Port Acknowledge (Link Port 0-1).
THD_P	I				Thermal Diode Anode
THD_M	O				Thermal Diode Cathode
TDI	I (pu)	✓			Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a fixed internal pull-up resistor ^{1, 2} .
TDO	O /T	✓		High-Z	Test Data Output (JTAG). Serial scan output of the boundary scan path.
TMS	I (pu)	✓			Test Mode Select (JTAG). Used to control the test state machine. TMS has a fixed internal pull-up resistor ^{1, 2} .
TCK	I (pu)	✓			Test Clock (JTAG). Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21469.

Table 6. Pin List (Continued)

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
$\overline{\text{TRST}}$	I (pu)	✓			Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21469. $\overline{\text{TRST}}$ has a fixed internal pull-up resistor ^{1, 2} .
EMU	O/T (pu)	✓		High-Z	Emulation Status. Must be connected to the ADSP-21469 Analog Devices DSP Tools product line of JTAG emulators target board connector only. EMU has a fixed internal pull-up resistor ^{1, 2} .
CLK_CFG ₁₋₀	I	✓			Core to CLKIN Ratio Control. These pins set the start up clock frequency. See Table 9 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
BOOT_CFG ₂₋₀	I	✓			Boot Configuration Select. These pins select the boot mode for the processor. The BOOTCFG pins must be valid before reset is asserted. See Table 8 for a description of the boot modes.
$\overline{\text{RESET}}$	I (pu)	✓			Processor Reset. Resets the ADSP-21469 to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
XTAL	O	✓			Crystal Oscillator Terminal. Used in conjunction with CLKIN to drive an external crystal.
CLKIN	I	✓			Local Clock In. Used in conjunction with XTAL. CLKIN is the ADSP-21469 clock input. It configures the ADSP-21469 to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21469 to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
CLKOUT/ $\overline{\text{RESETOUT}}$ / RUNRSTIN	I/O (pu)	✓			Clock Out/Reset Out/Running Reset In. The functionality can be switched between the PLL output clock and reset out by setting Bit 12 of the PMCTL register. The default is reset out. This pin also has a third function as RUNRSTIN. The functionality of which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the <i>ADSP-21469 SHARC Processor Hardware Reference for the ADSP-21469 Processors</i> .
BR ₆₋₁	I/O	✓		High-Z/ Driven low	Bus request. Bus request pins for external DDR2 bus arbitration.
RPBA	I	✓			Rotating priority bus arbitration.
ID ₂₋₀	I	✓			Chip ID

¹ Pull-up/pull-down resistor can not be enabled/disabled and the value of the pull-up/pull-down resistor cannot be programmed.² Range of fixed pull-up resistor can be between 26k-63kΩ. Range of fixed pull-down resistor can be between 31k-85kΩ.

DATA MODES

The address and data pins of the external memory interface are muxed (using bits in the SYSCCTL register) to support the external memory interface data (input/output), the PDAP (input only), and the FLAGS (input/output). [Table 7](#) provides the pin settings.

Table 7. Function of Data Pins

DATA PIN MODE	AMI_ADDR [23:8]	AMI_ADDR [7:0]	AMI_DATA [7:0]
000	AMI_ADDR [23:0]		AMI_DATA [7:0]
001	Reserved		
010	Reserved		
011	FLAGS/PWM [15–0]	FLAGS [15–0]	
100	Reserved		
101	PDAP (DATA + CTRL)		FLAGS [7–0]
110	Reserved		
111	Three-state all pins		

BOOT MODES

Table 8. Boot Mode Selection

BOOTCFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI user boot (for 8-bit Flash boot)
011	Reserved
100	Link Port 0 Boot
101	Reserved

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

For details on processor timing, see [Timing Specifications](#) and [Figure 4 on Page 19](#).

Table 9. Core Instruction Rate/ CLKIN Ratio Selection

CLKCFG1–0	Core to CLKIN Ratio
00	6:1
01	32:1
11	Reserved
10	16:1

SPECIFICATIONS

OPERATING CONDITIONS

Parameter ¹	Description	Min	Max	Unit
V _{DD_INT}	Internal (Core) Supply Voltage	TBD ²	TBD ²	V
V _{DD_EXT}	External (I/O) Supply Voltage	3.14	3.46	V
V _{DD_DDR2} ³	DDR2 Controller Supply Voltage	1.71	1.89	V
V _{REF}	DDR2 Reference Voltage	0.84	0.96	V
V _{IH} ⁴	High Level Input Voltage @ V _{DD_EXT} = max	2.0	3.6	V
V _{IL} ⁴	Low Level Input Voltage @ V _{DD_EXT} = min	-0.3	0.8	V
V _{IH_CLKIN} ⁵	High Level Input Voltage @ V _{DD_EXT} = max	TBD	TBD	V
V _{IL_CLKIN} ⁵	Low Level Input Voltage @ V _{DD_EXT} = min	TBD	TBD	V
V _{IL_DDR2}	Low Level Input Voltage	-0.3	V _{REF} - 0.12	V
V _{IH_DDR2}	High Level Input Voltage	V _{REF} + 0.13	V _{DD_DDR2} + 0.3	V
T _{JUNCTION}	Junction Temperature 208-Lead PBGA @ T _{AMBIENT} 0°C to +70°C	0	125	C

¹Specifications subject to change without notice.

²The expected value is 1.1V and initial customer designs should design with a programmable regulator that can be adjusted from 0.95V to 1.15V +/-50mV

³Applies to DDR2 signals.

⁴Applies to input and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, FLAG3-0, DAI_Px, DPI_Px, $\overline{\text{SPIDS}}$, BOOTCFGx, CLKCFGx, CLKOUT ($\overline{\text{RUNRSTIN}}$), $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$.

⁵Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter ¹	Description	Test Conditions	Min	Typical	Max	Unit
V_{OH}^2	High Level Output Voltage	@ $V_{DD_EXT} = \min$, $I_{OH} = -1.0 \text{ mA}^3$	2.4			V
V_{OL}^2	Low Level Output Voltage	@ $V_{DD_EXT} = \min$, $I_{OL} = 1.0 \text{ mA}^3$			0.4	V
$I_{OH_DDR2}^4$	Output Source DC Current	@ $V_{OH_DDR2} (DC) = V_{DD_DDR2} - 0.28 \text{ V}$	TBD			mA
$I_{OL_DDR2}^4$	Output Sink DC Current	@ $V_{OL_DDR2} (DC) = 0.28$			TBD	mA
$I_{IH}^{5,6}$	High Level Input Current	@ $V_{DD_EXT} = \max$, $V_{IN} = V_{DD_EXT} \max$			10	μA
I_{IL}^5	Low Level Input Current	@ $V_{DD_EXT} = \max$, $V_{IN} = 0 \text{ V}$			10	μA
I_{ILPU}^6	Low Level Input Current Pull-up	@ $V_{DD_EXT} = \max$, $V_{IN} = 0 \text{ V}$			TBD	μA
$I_{OZH}^{7,8}$	Three-State Leakage Current	@ $V_{DD_EXT} = \max$, $V_{IN} = V_{DD_EXT} \max$			10	μA
I_{OZL}^7	Three-State Leakage Current	@ $V_{DD_EXT} = \max$, $V_{IN} = 0 \text{ V}$			10	μA
I_{OZLPU}^8	Three-State Leakage Current Pull-up	@ $V_{DD_EXT} = \max$, $V_{IN} = 0 \text{ V}$			TBD	μA
$I_{DD_INTYP}^{9,10}$	Supply Current (Internal)	TBD			TBD	mA
$C_{IN}^{11,12}$	Input Capacitance	TBD			TBD	pF

¹ Specifications subject to change without notice.

² Applies to output and bidirectional pins: $\overline{AMI_ADDR23-0}$, $\overline{AMI_DATA7-0}$, $\overline{AMI_RD}$, $\overline{AMI_WR}$, $\overline{FLAG3-0}$, $\overline{DAI_Px}$, $\overline{DPI_Px}$, \overline{EMU} , \overline{TDO} , \overline{CLKOUT} .

³ See [Output Drive Currents on Page 50](#) for typical drive current capabilities.

⁴ Applies to $\overline{DDR2_ADDR18-0}$, $\overline{DDR2_CAS}$, $\overline{DDR2_CS3-0}$, $\overline{DDR2_DQ1-0}$, $\overline{DDR2_DM1-0}$, $\overline{DDR2_DQS1-0}$, $\overline{DDR2_DATA15-0}$, $\overline{DDR2_RAS}$, $\overline{DDR2_WE}$, $\overline{DDR2_CLK0}$, $\overline{DDR2_CLK1}$ and $\overline{DDR2_CLK1}$.

⁵ Applies to input pins: $\overline{BOOTCFGx}$, $\overline{CLKCFGx}$, \overline{TCK} , \overline{RESET} , \overline{CLKIN} .

⁶ Applies to input pins with 22.5 k Ω internal pull-ups: \overline{TRST} , \overline{TMS} , \overline{TDI} .

⁷ Applies to three-statable pins: $\overline{FLAG3-0}$.

⁸ Applies to three-statable pins with 22.5 k Ω pull-ups: $\overline{DAI_Px}$, $\overline{DPI_Px}$, \overline{EMU} .

⁹ Typical internal current data reflects nominal operating conditions.

¹⁰ See Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-21469 SHARC Processors" for further information.

¹¹ Applies to all signal pins.

¹² Guaranteed, but not tested.

PACKAGE INFORMATION

The information presented in [Figure 3](#) provides details about the package branding for the ADSP-21469 processor. For a complete listing of product availability, see [Ordering Guide on Page 55](#).



Figure 3. Typical Package Brand

Table 10. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY

	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be take to avoid performance degradation or loss of functionality.
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MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-21469 SHARC Processors” for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see [Thermal Characteristics on Page 51](#).

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in [Table 11](#) may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V _{DD_INT})	–0.3 V to +1.32V
Analog (PLL) Supply Voltage (V _{DD_A})	TBD
External (I/O) Supply Voltage (V _{DD_EXT})	–0.3 V to +4.6V
DDR2 Controller Supply Voltage (V _{DD_DDR2})	–0.5 V to +2.7V
Input Voltage	–0.5 V to +3.8V
Output Voltage Swing	–0.5 V to V _{DD_EXT} +0.5V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

TIMING SPECIFICATIONS

The ADSP-21469's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1–0 pins (see [Table 9 on Page 15](#)). To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

Figure 4 shows core to CLKIN ratios of 6:1, 16:1, and 32:1 with external oscillator or crystal. Note that more ratios are possible and can be set through software using the power management control register (PMCTL). For more information, see the *ADSP-21469 SHARC Processor Programming Reference*.

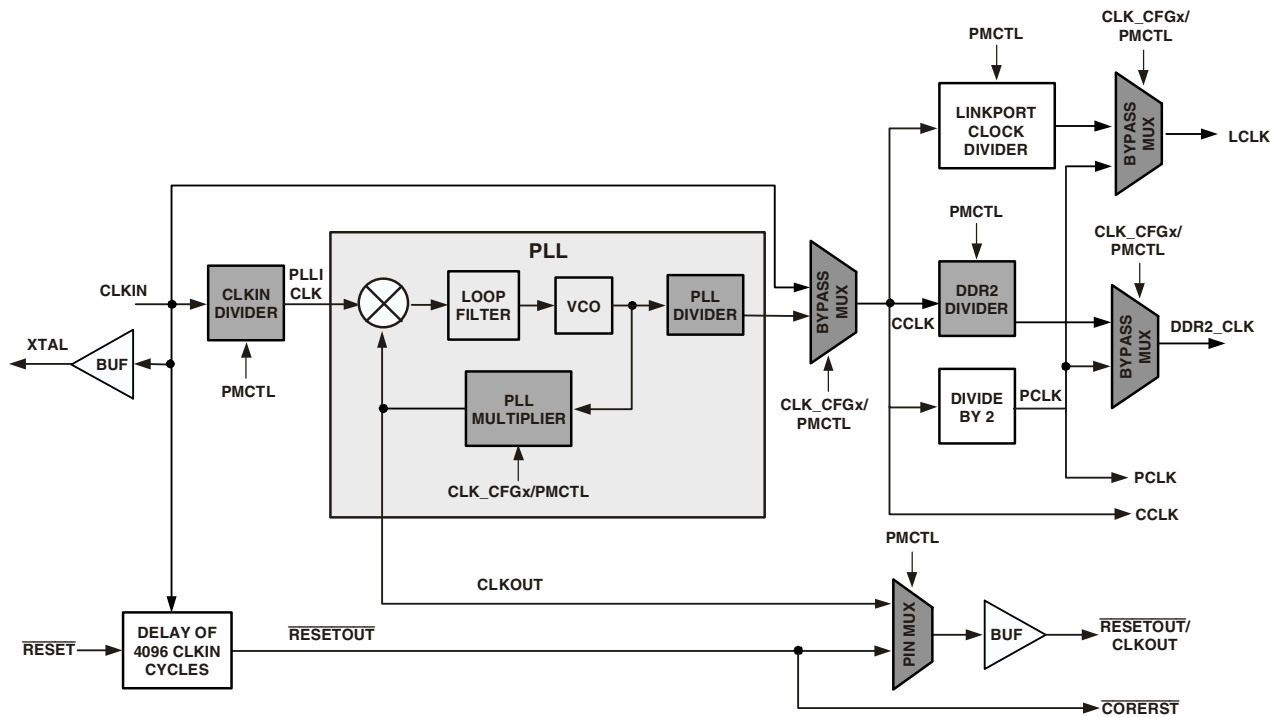


Figure 4. Core Clock and System Clock Relationship to CLKIN

The ADSP-21469's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Core clock frequency can be calculated as:

$$CCLK = (f_{INPUT} \times 2 \times PLLM) / (2 \times PLLD)$$

Note the definitions of various clock periods shown in [Table 13](#) which are a function of CLKIN and the appropriate ratio con-

Note that in the user application, the PLL multiplier value should be selected in such a way that the VCO frequency falls in between 200 MHz and 900 MHz. The VCO frequency is calculated as follows:

where:

$$f_{VCO} = f_{INPUT} \times 2 \times PLLM$$

$PLLM$ = multiplier value programmed.

$PLLD$ = divider value programmed.

f_{INPUT} = input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled.

f_{INPUT} = CLKIN/2 when the input divider is enabled.

trol shown in [Table 12](#).

Table 12. ADSP-21469 CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Table 13. Clock Periods

Timing Requirements	Description ¹
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = $2 \times t_{CCLK}$
t_{SCLK}	Serial Port Clock Period = $(t_{PCLK}) \times SR$
t_{DDR2_CLK}	DDR2 DRAM Clock Period = $(t_{CCLK}) \times SDR$
t_{SPICLK}	SPI Clock Period = $(t_{PCLK}) \times SPIR$

¹ where:

SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV bits in DIVx register)

SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPIBAUD register setting)

SDR=DDR2 DRAM-to-Core Clock Ratio (Values determined by bits 20-18 of the PMCTL register)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See [Figure 42 on Page 50](#) under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are given in [Table 14](#).

Table 14. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{RSTVDD}	\overline{RESET} Low Before V_{DD_EXT} or V_{DD_DDR2} On	0		ms
$t_{EVDD_DDR2VDD}$	V_{DD_EXT} on Before V_{DD_DDR2}	TBD		ms
$t_{DDR2VDD_IVDD}$	V_{DD_DDR2} on Before V_{DD_INT}	TBD		ms
t_{CLKVDD}^1	CLKIN Valid After V_{DD_INT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before \overline{RESET} Deasserted	10^2		ms
t_{PLLRST}	PLL Control Setup Before \overline{RESET} Deasserted	20^3		ms
<i>Switching Characteristic</i>				
$t_{CORERST}$	Core Reset Deasserted After \overline{RESET} Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}^{4,5}$		ms

¹ Valid V_{DD_INT} assumes that the supply is fully ramped to its 1 volt rail. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

² Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

³ Based on CLKIN cycles.

⁴ Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for \overline{RESET} to be held low in order to properly initialize and propagate default states at all I/O pins.

⁵ The 4096 cycle count depends on t_{SRST} specification in [Table 16](#). If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

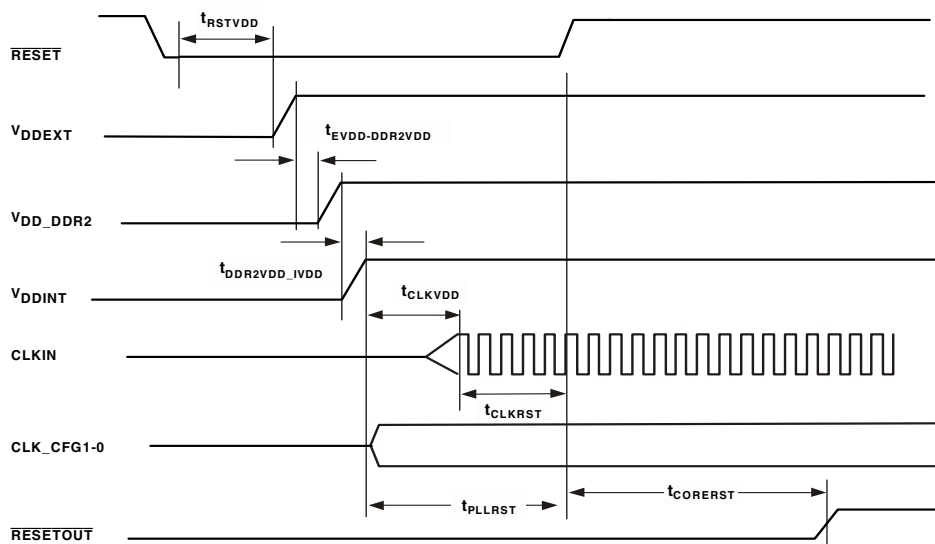


Figure 5. Power-Up Sequencing

Clock Input

Table 15. Clock Input

Parameter		450 MHz		Unit
		Min	Max	
Timing Requirements				
t _{CK}	CLKIN Period	TBD ¹	TBD ²	ns
t _{CKL}	CLKIN Width Low	TBD ¹	TBD ²	ns
t _{CKH}	CLKIN Width High	TBD ¹	TBD ²	ns
t _{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		TBD	ns
t _{CCLK} ³	CCLK Period	2.22 ¹	TBD	ns

¹ Applies only for CLKCFG1-0 = 00 and default values for PLL control bits in PMCTL.

² Applies only for CLKCFG1-0 = 01 and default values for PLL control bits in PMCTL.

³ Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK} .

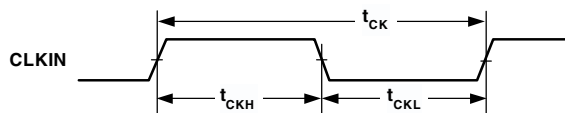


Figure 6. Clock Input

Clock Signals

The ADSP-21469 can use an external clock or a crystal. See the CLKIN pin description in Table 6. The programmer can configure the ADSP-21469 to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 28.125 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 450 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

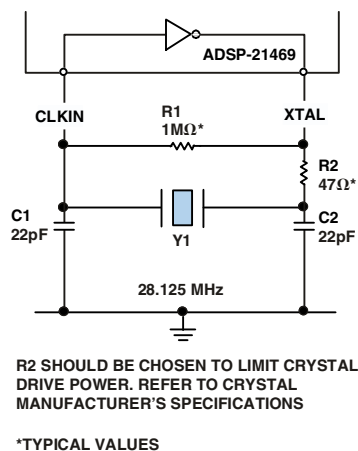
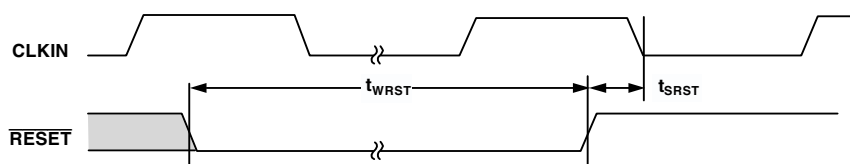


Figure 7. 450 MHz Operation (Fundamental Mode Crystal)

Reset**Table 16. Reset**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{WRST}^1	\overline{RESET} Pulse Width Low	TBD	TBD	ns
t_{SRST}	\overline{RESET} Setup Before CLKIN Low	TBD	TBD	ns

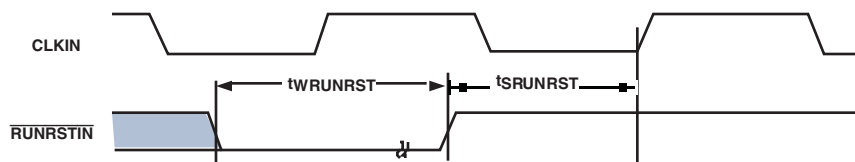
¹ Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 μ s while \overline{RESET} is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

*Figure 8. Reset***Running Reset**

The following timing specification applies to CLKOUT/ $\overline{RESETOUT}$ /RUNRSTIN pin when it is configured as RUNRSTIN.

Table 17. Running Reset

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{WRUNRST}$	Running \overline{RESET} Pulse Width Low	TBD	TBD	ns
$t_{SRUNRST}$	Running \overline{RESET} Setup Before CLKIN High	TBD	TBD	ns

*Figure 9. Running Reset*

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20-1 and DPI_P14-1 pins when they are configured as interrupts.

Table 18. Interrupts

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{IPW} $\overline{\text{IRQx}}$ Pulse Width	TBD	TBD	ns

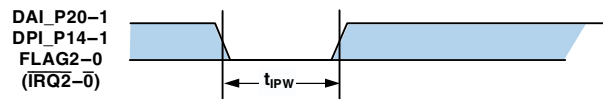


Figure 10. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 19. Core Timer

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{WCTIM} CTIMER Pulse Width	TBD	TBD	ns

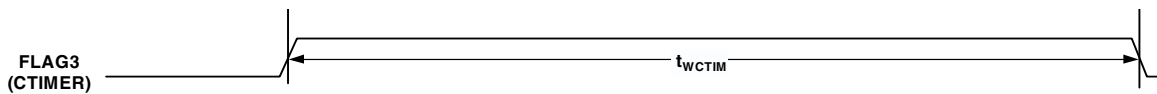


Figure 11. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14-1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14-1 pins.

Table 20. Timer PWM_OUT Timing

Parameter	Min	Max	Unit
<i>Switching Characteristic</i>			
t_{PWMO} Timer Pulse Width Output	TBD	TBD	ns

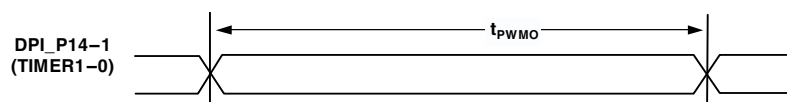


Figure 12. Timer PWM_OUT Timing

Timer WDT_H_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDT_H_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 21. Timer Width Capture Timing

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{PWI} Timer Pulse Width	TBD	TBD	ns

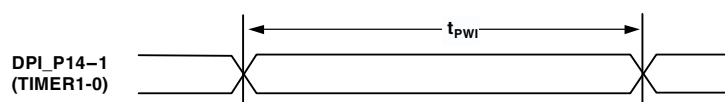


Figure 13. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 22. DAI Pin to Pin Routing

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{DPIO} Delay DAI/DPI Pin Input Valid to DAI Output Valid	TBD	TBD	ns

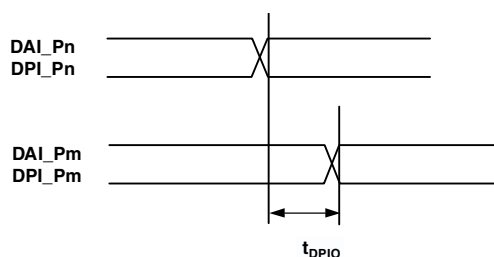


Figure 14. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's

inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 23. Precision Clock Generator (Direct Pin Routing)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{PCGIW} Input Clock Period	TBD	TBD	ns
t_{STRIG} PCG Trigger Setup Before Falling Edge of PCG Input Clock	TBD	TBD	ns
t_{HTRIG} PCG Trigger Hold After Falling Edge of PCG Input Clock	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{DPCGIO} PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	TBD	TBD	ns
$t_{DTRIGCLK}$ PCG Output Clock Delay After PCG Trigger	TBD	TBD	ns
$t_{DTRIGFS}$ PCG Frame Sync Delay After PCG Trigger	TBD	TBD	ns
t_{PCGOW}^1 Output Clock Period	TBD	TBD	ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-21469 SHARC Processor Hardware Reference for the ADSP-21469 Processor, "Precision Clock Generators" chapter.

¹Normal mode of operation.

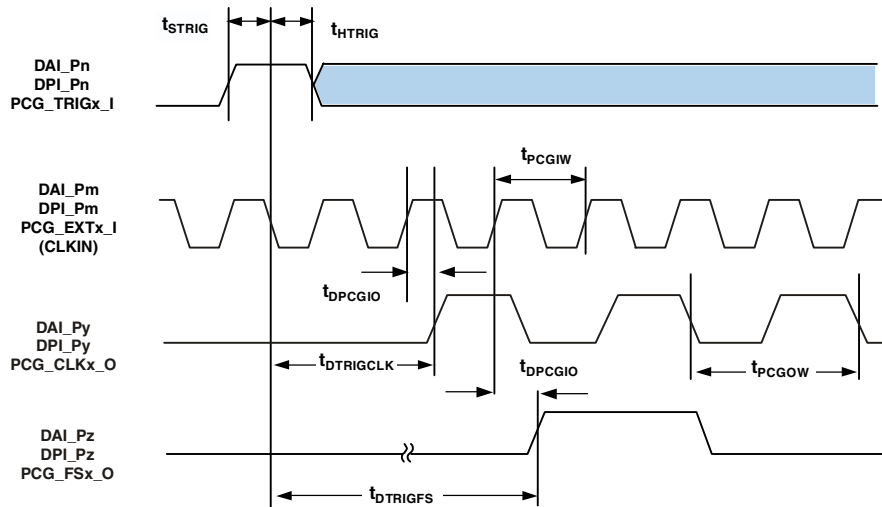


Figure 15. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to AMI_ADDR23-0 and AMI_DATA7-0 when configured as FLAGS. See [Table 6 on page 12](#) for more information on flag use.

Table 24. Flags

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{FIPW} DPI_P14-1, AMI_ADDR23-0, AMI_DATA7-0, FLAG3-0 IN Pulse Width	TBD	TBD	ns
<i>Switching Characteristic</i>			
t_{FOPW} DPI_P14-1, AMI_ADDR23-0, AMI_DATA7-0, FLAG3-0 OUT Pulse Width	TBD	TBD	ns

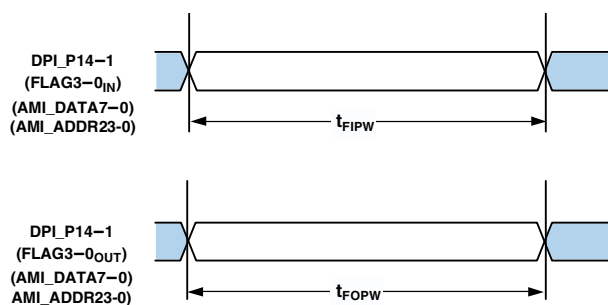


Figure 16. Flags

DDR2 SDRAM Read Cycle Timing

Table 25. DDR2 SDRAM Read Cycle Timing, V_{DD-DDR2} nominal 1.8V

Parameter	Symbol	Minimum	Maximum	Unit
Timing Requirements				
TBD	TBD	TBD	TBD	TBD

TBD

Figure 17. DDR2 SDRAM Controller Input AC Timing

DDR2 SDRAM Write Cycle Timing

Table 26. DDR2 SDRAM Write Cycle Timing, $V_{DD-DDR2}$ nominal 1.8V

Parameter	Symbol	Minimum	Maximum	Unit
Switching Characteristics				
TBD	TBD	TBD	TBD	TBD

TBD

Figure 18. DDR2 SDRAM Controller Output AC Timing

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for $\overline{\text{AMI_ACK}}$, $\overline{\text{AMI_DATA}}$, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 27. Memory Read—Bus Master

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{DAD} Address, Selects Delay to Data Valid ^{1,2}	TBD	TBD	ns
t_{DRLD} $\overline{\text{AMI_RD}}$ Low to Data Valid ¹	TBD	TBD	ns
t_{SDS} Data Setup to $\overline{\text{AMI_RD}}$ High	TBD	TBD	ns
t_{HDRH} Data Hold from $\overline{\text{AMI_RD}}$ High ^{3,4}	TBD	TBD	ns
t_{DAAK} $\overline{\text{AMI_ACK}}$ Delay from Address, Selects ^{2,5}	TBD	TBD	ns
t_{DSAK} $\overline{\text{AMI_ACK}}$ Delay from $\overline{\text{AMI_RD}}$ Low ⁴	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{DRHA} Address Selects Hold After $\overline{\text{AMI_RD}}$ High	TBD	TBD	ns
t_{DARL} Address Selects to $\overline{\text{AMI_RD}}$ Low ²	TBD	TBD	ns
t_{RW} $\overline{\text{AMI_RD}}$ Pulse Width	TBD	TBD	ns
t_{RWR} $\overline{\text{AMI_RD}}$ High to $\overline{\text{AMI_WR}}$, $\overline{\text{AMI_RD}}$, Low	TBD	TBD	ns

$W = (\text{number of wait states specified in AMICTLx register}) \times t_{\text{DDR2_CLK}}$.

$HI = RHC + IC$ ($RHC = (\text{number of Read Hold Cycles specified in AMICTLx register}) \times t_{\text{DDR2_CLK}}$).

$IC = (\text{number of idle cycles specified in AMICTLx register}) \times t_{\text{DDR2_CLK}}$.

$H = (\text{number of hold cycles specified in AMICTLx register}) \times t_{\text{DDR2_CLK}}$.

¹Data delay/setup: System must meet t_{DAD} , t_{DRLD} , or t_{SDS} .

²The falling edge of $\overline{\text{MSx}}$, is referenced.

³Note that timing for $\overline{\text{AMI_ACK}}$, $\overline{\text{AMI_DATA}}$, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

⁴Data hold: User must meet t_{HDRH} in asynchronous access mode. See [Test Conditions on Page 50](#) for the calculation of hold times given capacitive and dc loads.

⁵ $\overline{\text{AMI_ACK}}$ delay/setup: User must meet t_{DAAK} or t_{DSAK} for deassertion of $\overline{\text{AMI_ACK}}$ (low). For asynchronous assertion of $\overline{\text{AMI_ACK}}$ (high) user must meet t_{DAAK} or t_{DSAK} .

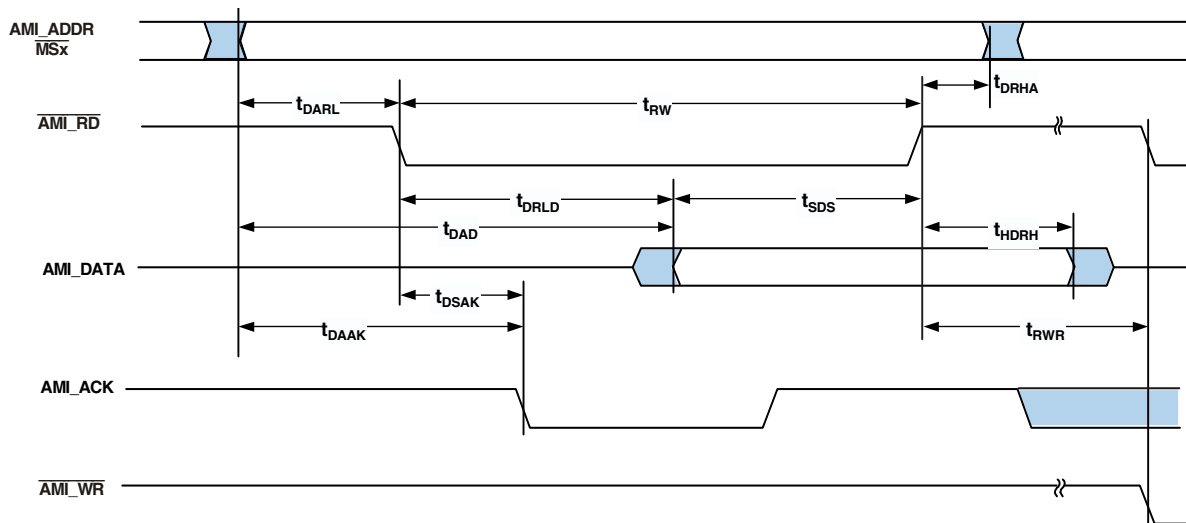


Figure 19. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for $\overline{\text{AMI_ACK}}$, $\overline{\text{AMI_DATA}}$, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 28. Memory Write—Bus Master

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{DAAK}	$\overline{\text{AMI_ACK}}$ Delay from Address, Selects ^{1,2}	TBD	TBD	ns
t_{DSAK}	$\overline{\text{AMI_ACK}}$ Delay from $\overline{\text{AMI_WR}}$ Low ^{1,3}	TBD	TBD	ns
<i>Switching Characteristics</i>				
t_{DAWH}	Address, Selects to $\overline{\text{AMI_WR}}$ Deasserted ²	TBD	TBD	ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI_WR}}$ Low ²	TBD	TBD	ns
t_{WW}	$\overline{\text{AMI_WR}}$ Pulse Width	TBD	TBD	ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI_WR}}$ High	TBD	TBD	ns
t_{DWHA}	Address Hold After $\overline{\text{AMI_WR}}$ Deasserted	TBD	TBD	ns
t_{DWHd}	Data Hold After $\overline{\text{AMI_WR}}$ Deasserted	TBD	TBD	ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI_WR}}$ Deasserted ⁴	TBD	TBD	ns
t_{WWR}	$\overline{\text{AMI_WR}}$ High to $\overline{\text{AMI_WR}}$, $\overline{\text{AMI_RD}}$ Low	TBD	TBD	ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI_RD}}$ Low	TBD	TBD	ns
t_{WDE}	$\overline{\text{AMI_WR}}$ Low to Data Enabled	TBD	TBD	ns

$W = (\text{number of wait states specified in AMICTLx register}) \times t_{\text{sDDR2_CLKH}} = (\text{number of hold cycles specified in AMICTLx register}) \times t_{\text{DDR2_CLK}}$

¹ $\overline{\text{AMI_ACK}}$ delay/setup: System must meet t_{DAAK} , or t_{DSAK} , for deassertion of $\overline{\text{AMI_ACK}}$ (low). For asynchronous assertion of $\overline{\text{AMI_ACK}}$ (high) user must meet t_{DAAK} or t_{DSAK} .

² The falling edge of $\overline{\text{MSx}}$ is referenced.

³ Note that timing for $\overline{\text{AMI_ACK}}$, $\overline{\text{AMI_DATA}}$, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only applies to asynchronous access mode.

⁴ See [Test Conditions on Page 50](#) for calculation of hold times given capacitive and dc loads.

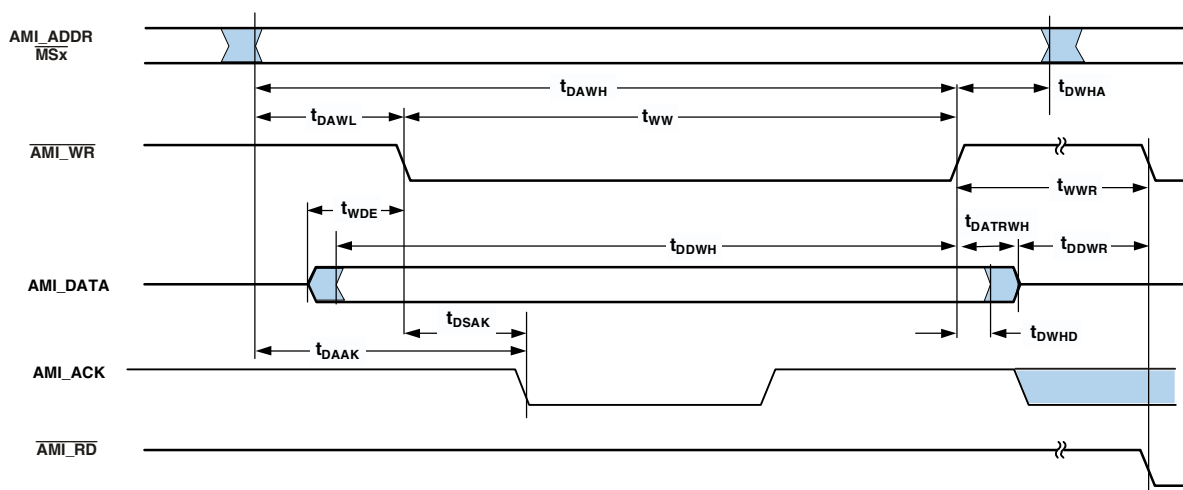


Figure 20. Memory Write—Bus Master

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = $t_{LCLK-TWH \min} - t_{DLDCH} - t_{SLDCL}$). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLK-TWL \min} - t_{HLDCH} - t_{HLDCL}$). Calculations made directly

from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

ADSP-21469 Setup Skew = TBD ns max

ADSP-21469 Hold Skew = TBD ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 29. Link Ports – Receive

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SLDCL} Data Setup Before LCLK Low	TBD	TBD	ns
t_{HLDCL} Data Hold After LCLK Low	TBD	TBD	ns
t_{LCLKIW} LCLK Period	TBD	TBD	ns
$t_{LCLKRWL}$ LCLK Width Low	TBD	TBD	ns
$t_{LCLKRWH}$ LCLK Width High	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{DLALC} LACK Low Delay After LCLK High ¹	TBD	TBD	ns

¹ LACK goes low with t_{DLALC} relative to rise of LCLK after first byte, but does not go low if the receiver's link buffer is not about to fill.

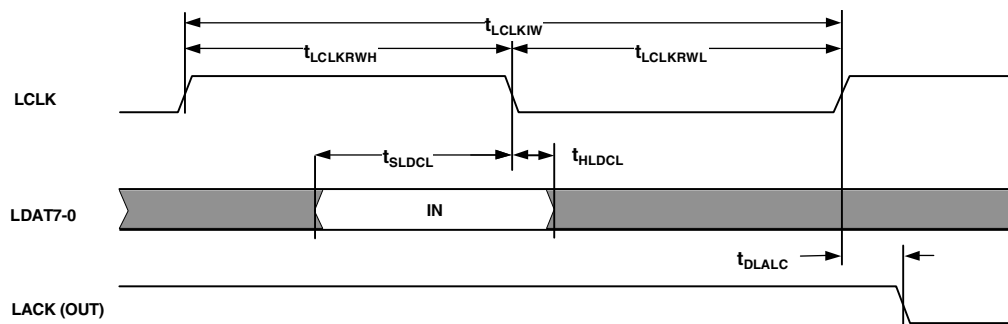


Figure 21. Link Ports—Receive

Table 30. Link Ports – Transmit

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SLACH}	LACK Setup Before LCLK High	TBD	TBD	ns
t_{HLACH}	LACK Hold After LCLK High	TBD	TBD	ns
<i>Switching Characteristics</i>				
t_{DLCH}	Data Delay After LCLK High	TBD	TBD	ns
t_{HLDCH}	Data Hold After LCLK High	TBD	TBD	ns
$t_{LCLKTWL}$	LCLK Width Low	TBD	TBD	ns
$t_{LCLKTWH}$	LCLK Width High	TBD	TBD	ns
t_{DLACK}	LCLK Low Delay After LACK High	TBD	TBD	ns

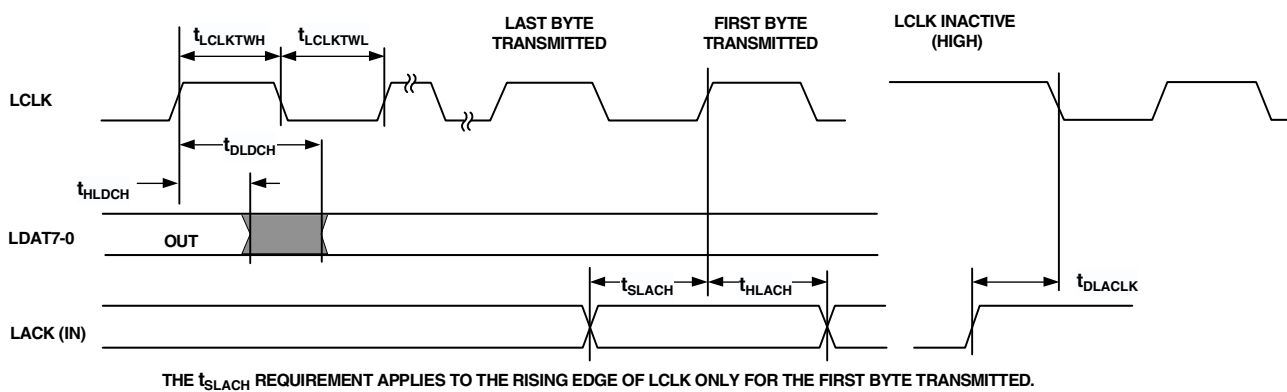


Figure 22. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n , the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 31. Serial Ports—External Clock

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SFSE}^1 FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HFSE}^1 FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{SDRE}^1 Receive Data Setup Before Receive SCLK	TBD	TBD	ns
t_{HDRE}^1 Receive Data Hold After SCLK	TBD	TBD	ns
t_{SCLKW} SCLK Width	TBD	TBD	ns
t_{SCLK} SCLK Period	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{DFSE}^2 FS Delay After SCLK (Internally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HOFSE}^2 FS Hold After SCLK (Internally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{DDTE}^2 Transmit Data Delay After Transmit SCLK	TBD	TBD	ns
t_{HDT}^2 Transmit Data Hold After Transmit SCLK	TBD	TBD	ns

¹Referenced to sample edge.

²Referenced to drive edge.

Table 32. Serial Ports—Internal Clock

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SFSI}^1 FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HFSI}^1 FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{SDRI}^1 Receive Data Setup Before SCLK	TBD	TBD	ns
t_{HDRI}^1 Receive Data Hold After SCLK	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{DFSIR}^2 FS Delay After SCLK (Internally Generated FS in Transmit Mode)	TBD	TBD	ns
t_{HOFSI}^2 FS Hold After SCLK (Internally Generated FS in Transmit Mode)	TBD	TBD	ns
t_{DFSIR}^2 FS Delay After SCLK (Internally Generated FS in Receive Mode)	TBD	TBD	ns
t_{HOFSI}^2 FS Hold After SCLK (Internally Generated FS in Receive Mode)	TBD	TBD	ns
t_{DDTI}^2 Transmit Data Delay After SCLK	TBD	TBD	ns
t_{HDTI}^2 Transmit Data Hold After SCLK	TBD	TBD	ns
t_{SCKLIW} Transmit or Receive SCLK Width	TBD	TBD	ns

¹Referenced to the sample edge.

²Referenced to drive edge.

Table 33. Serial Ports—Enable and Three-State

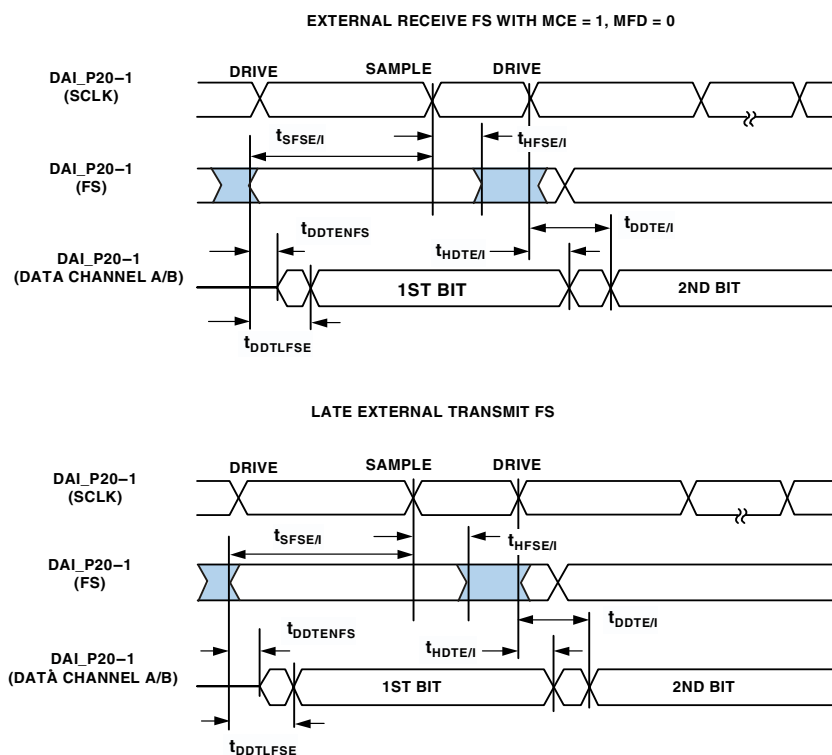
Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
t_{DDTEN}^1 Data Enable from External Transmit SCLK	TBD	TBD	ns
t_{DDTTE}^1 Data Disable from External Transmit SCLK	TBD	TBD	ns
t_{DDTIN}^1 Data Enable from Internal Transmit SCLK	TBD	TBD	ns

¹ Referenced to drive edge.

Table 34. Serial Ports—External Late Frame Sync

Parameter	Min	Max	Unit
<i>Switching Characteristics</i>			
$t_{DDTLFSE}^1$ Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0	TBD	TBD	ns
$t_{DDTENFS}^1$ Data Enable for MCE = 1, MFD = 0	TBD	TBD	ns

¹ The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.



NOTE: SERIAL PORT SIGNALS (SCLK, FS, DATA CHANNEL A/B) ARE ROUTED TO THE DAI_P20-1 PINS USING THE SRU. THE TIMING SPECIFICATIONS PROVIDED HERE ARE VALID AT THE DAI_P20-1 PINS. THE CHARACTERIZED AC SPORT TIMINGS ARE APPLICABLE WHEN INTERNAL CLOCKS AND FRAMES ARE LOOPED BACK FROM THE PIN, NOT ROUTED DIRECTLY THROUGH SAU.

Figure 23. External Late Frame Sync¹

¹ This figure reflects changes made to support left-justified sample pair mode.

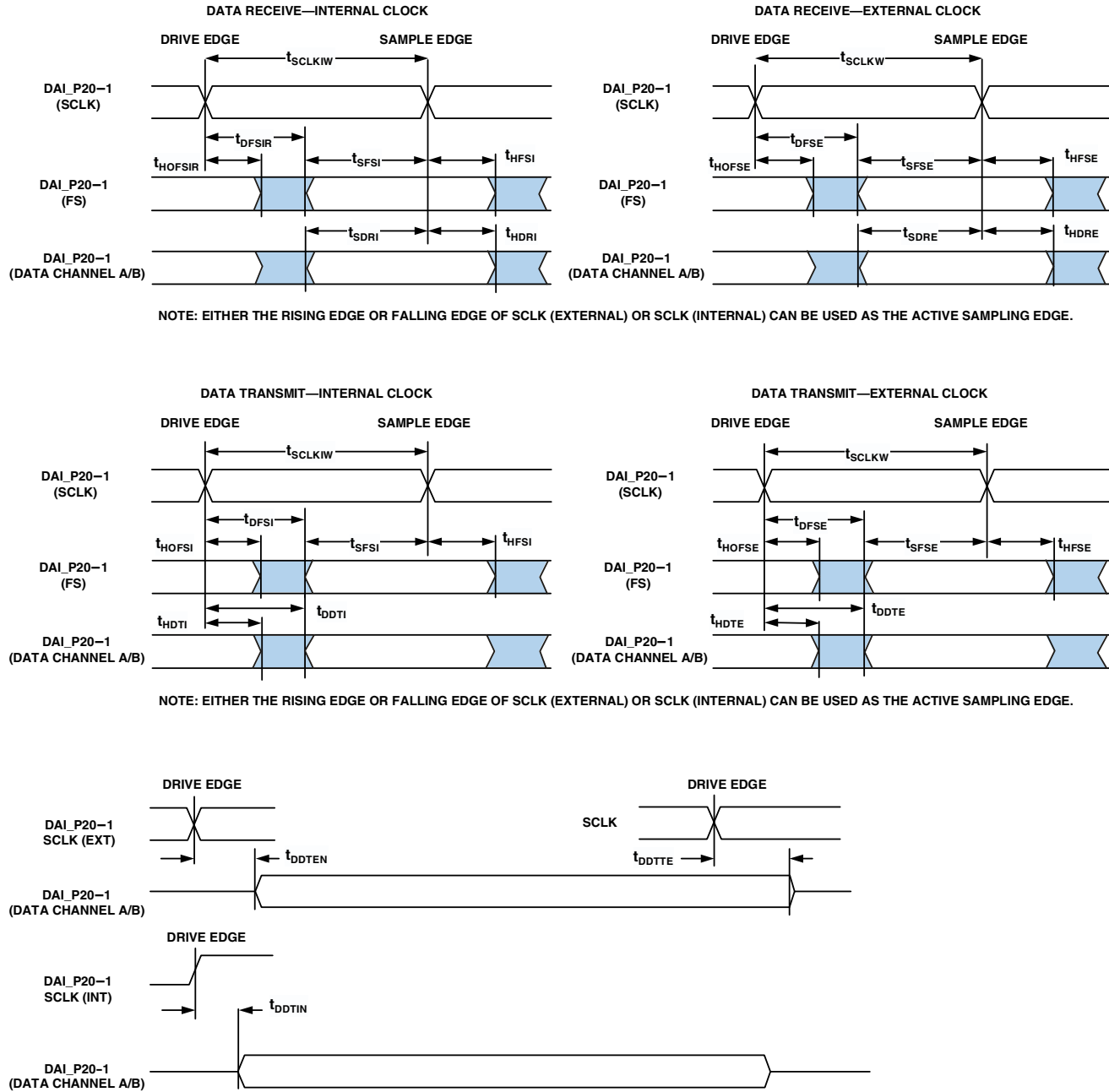


Figure 24. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 35. IDP signals (SCLK, FS, and SDATA) are routed to the DAI_P20-1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20-1 pins.

Table 35. Input Data Port (IDP)

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SISFS}^1	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHFS}^1	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SISD}^1	SDATA Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHD}^1	SDATA Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{IDPCLKW}$	Clock Width	TBD	TBD	ns
t_{IDPCLK}	Clock Period	TBD	TBD	ns

¹ AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

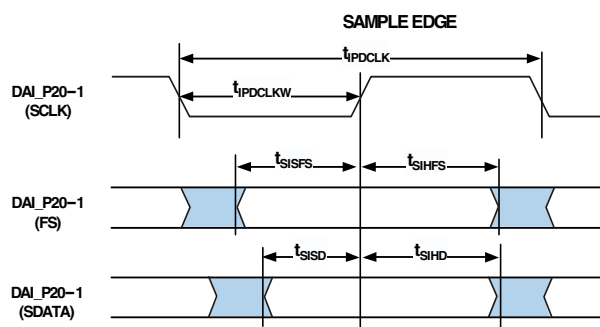


Figure 25. IDP Master Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals (SCLK, FS, and SDATA) are routed from the DAI_P20-1 pins using the SRU. Therefore, the timing specifications provided in Table 36 are valid at the DAI_P20-1 pins.

Table 36. ASRC, Serial Input Port

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SRCFS}^1	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHFS}^1	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SRCSD}^1	SDATA Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHD}^1	SDATA Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SRCCLKW}$	Clock Width	TBD	TBD	ns
t_{SRCCLK}	Clock Period	TBD	TBD	ns

¹ AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

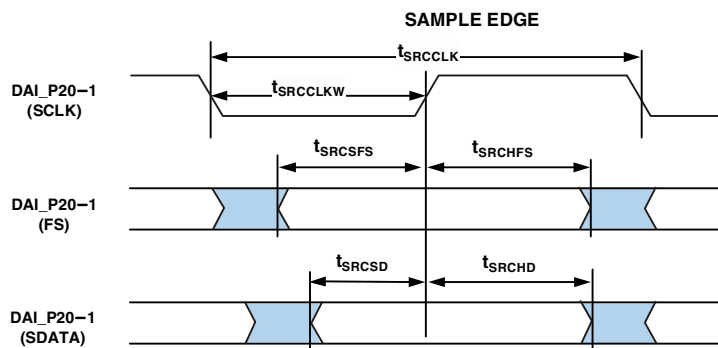


Figure 26. ASRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time

and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 37. ASRC, Serial Output Port

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
t_{SRCSFS}^1 FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHFS}^1 FS Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SRCCLKW}$ Clock Width	TBD	TBD	ns
t_{SRCCLK} Clock Period	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{SRCTDD}^1 Transmit Data Delay After SCLK Falling Edge	TBD	TBD	ns
t_{SRCTDH}^1 Transmit Data Hold After SCLK Falling Edge	TBD	TBD	ns

¹ AMI_DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

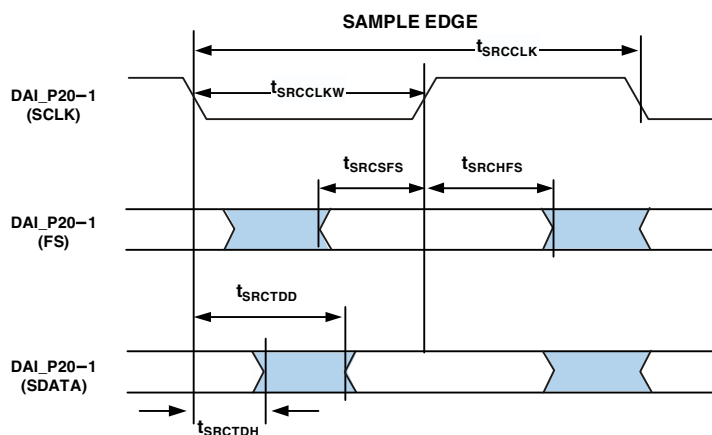


Figure 27. ASRC Serial Output Port Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in [Table 38](#). PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-21469 SHARC Processor Hardware*

Reference. Note that the most significant 16 bits of external PDAP data can be provided through the DATA7-0 pins. The remaining four bits can only be sourced through DAI_P4-1. The timing below is valid at the DATA7-0 pins.

Table 38. Parallel Data Acquisition Port (PDAP)

Parameter	Min	Max	Unit
<i>Timing Requirements</i>			
$t_{SPCLKEN}^1$ PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	TBD	TBD	ns
$t_{HPCLKEN}^1$ PDAP_CLKEN Hold After PDAP_CLK Sample Edge	TBD	TBD	ns
$t_{PDS D}^1$ PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	TBD	TBD	ns
t_{PDHD}^1 PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	TBD	TBD	ns
t_{PDCLKW} Clock Width	TBD	TBD	ns
t_{PDCLK} Clock Period	TBD	TBD	ns
<i>Switching Characteristics</i>			
t_{PDHLDD} Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	TBD	TBD	ns
t_{PDSTRB} PDAP Strobe Pulse Width	TBD	TBD	ns

¹ Source pins of AMI_DATA are DATA7-0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

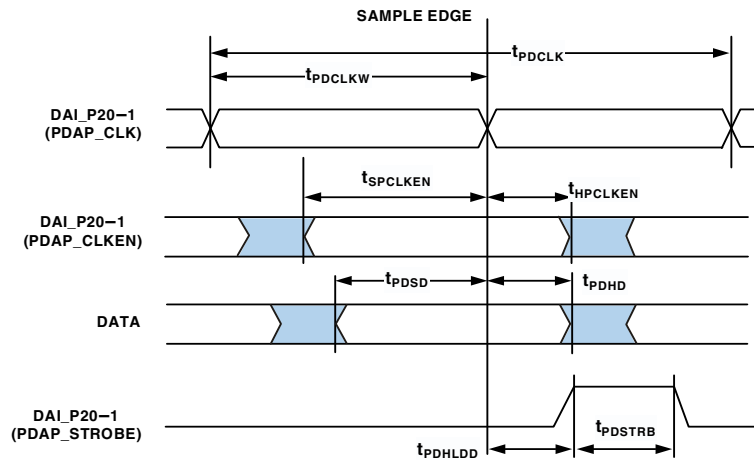


Figure 28. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the AML_ADDR23-8 pins are configured as PWM.

Table 39. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
<i>Switching Characteristics</i>				
t_{PWMW}	PWM Output Pulse Width	TBD	TBD	ns
t_{PWMP}	PWM Output Period	TBD	TBD	ns

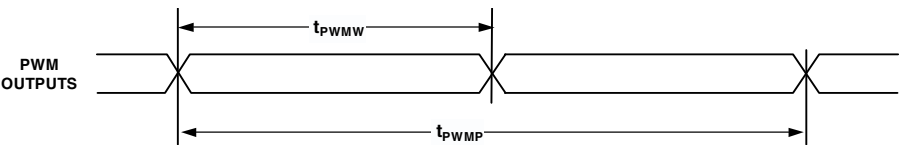


Figure 29. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output

mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

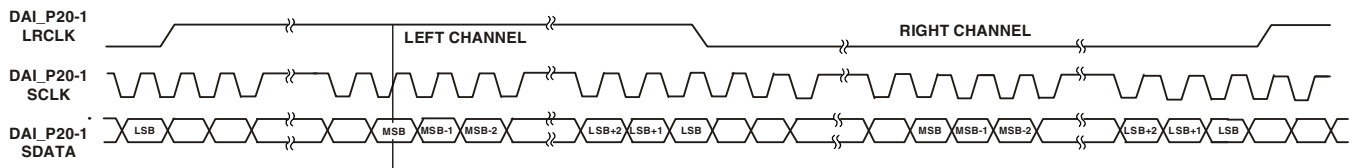


Figure 30. Right-Justified Mode

Figure 31 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

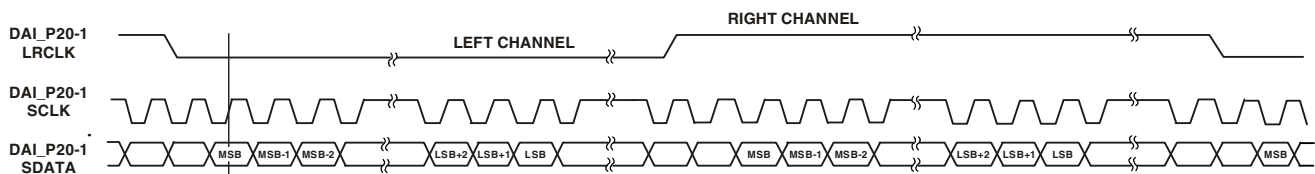


Figure 31. I²S-Justified Mode

Figure 32 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

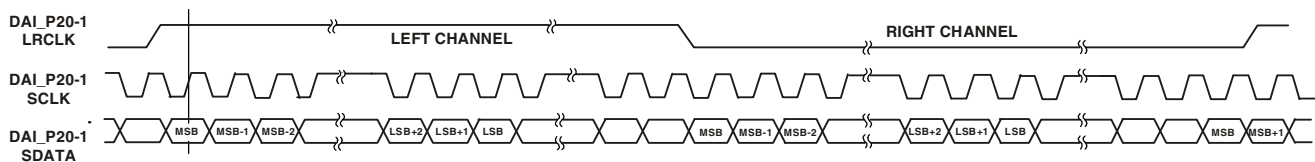


Figure 32. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 40. Input signals (SCLK, FS, SDATA) are routed to the DAI_P20-1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20-1 pins.

Table 40. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SISFS}^1	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHFS}^1	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SISD}^1	SData Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHD}^1	SData Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SITXCLKW}$	Transmit Clock Width	TBD	TBD	ns
$t_{SITXCLK}$	Transmit Clock Period	TBD	TBD	ns
$t_{SISCLKW}$	Clock Width	TBD	TBD	ns
t_{SISCLK}	Clock Period	TBD	TBD	ns

¹ AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

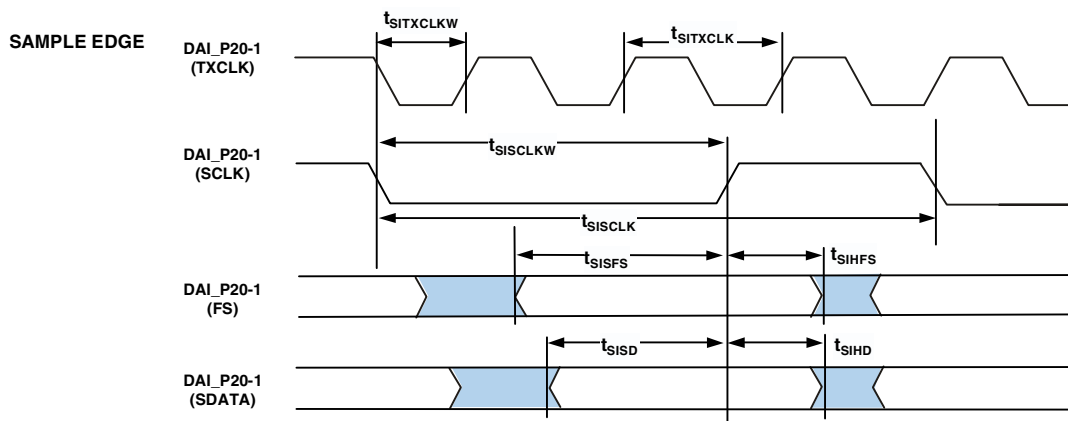


Figure 33. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphas clock.

Table 41. Over Sampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = $384 \times FS$	TBD	TBD	MHz
TxCLK Frequency for TxCLK = $256 \times FS$	TBD	TBD	MHz
Frame Rate	TBD	TBD	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the $TBD \times FS$ clock.

Table 42. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
<i>Switching Characteristics</i>				
t_{DFSI}	LRCLK Delay After SCLK	TBD	TBD	ns
t_{HOFSI}	LRCLK Hold After SCLK	TBD	TBD	ns
t_{DDTI}	Transmit Data Delay After SCLK	TBD	TBD	ns
t_{HDTI}	Transmit Data Hold After SCLK	TBD	TBD	ns
t_{SCLKIW}^1	Transmit SCLK Width	TBD	TBD	ns

¹ SCLK frequency is $TBD \times FS$ where FS = the frequency of LRCLK.

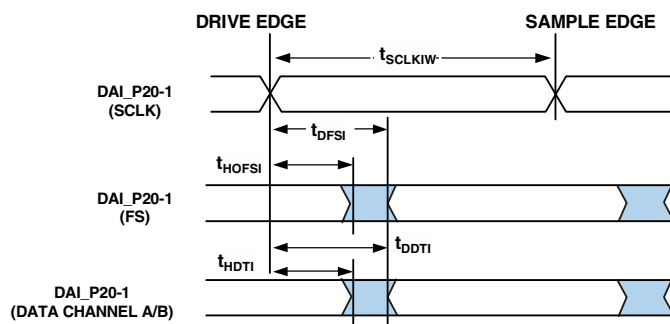


Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-21469 contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in [Table 43](#) and [Table 44](#) applies to both.

Table 43. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	TBD	TBD	ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	TBD	TBD	ns
<i>Switching Characteristics</i>				
$t_{SPICLKM}$	Serial Clock Cycle	TBD	TBD	ns
t_{SPICHM}	Serial Clock High Period	TBD	TBD	ns
t_{SPICLM}	Serial Clock Low Period	TBD	TBD	ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)	TBD	TBD	ns
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	TBD	TBD	ns
t_{SDSCIM}	FLAG3–0IN (SPI device select) Low to First SPICLK Edge	TBD	TBD	ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	TBD	TBD	ns
t_{SPITDM}	Sequential Transfer Delay	TBD	TBD	ns

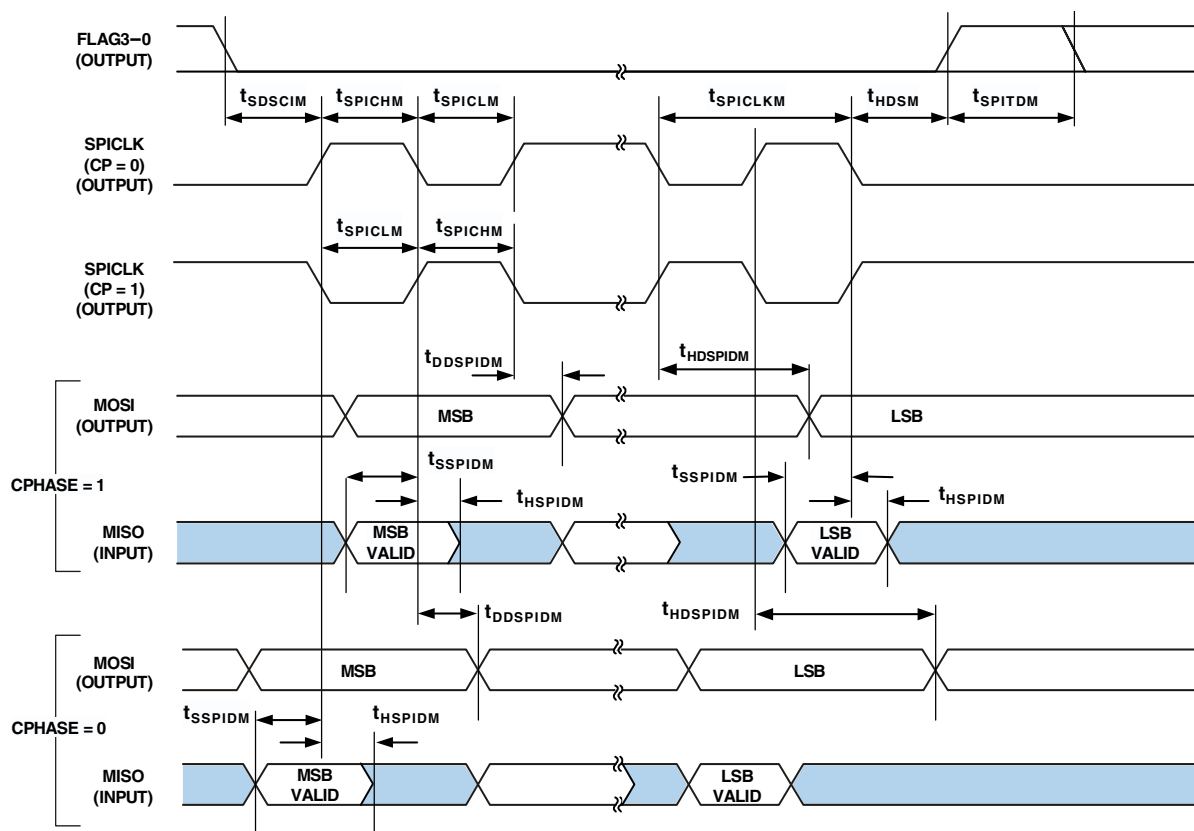


Figure 35. SPI Master Timing

SPI Interface—Slave**Table 44. SPI Interface Protocol—Slave Switching and Timing Specifications**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
$t_{SPICLKS}$	Serial Clock Cycle	TBD	TBD	ns
t_{SPICHs}	Serial Clock High Period	TBD	TBD	ns
t_{SPICLS}	Serial Clock Low Period	TBD	TBD	ns
t_{SDSCO}	\overline{SPIDS} Assertion to First SPICLK Edge			
	CPHASE = 0	TBD	TBD	ns
	CPHASE = 1	TBD	TBD	ns
t_{HDS}	Last SPICLK Edge to \overline{SPIDS} Not Asserted, CPHASE = 0	TBD	TBD	ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	TBD	TBD	ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	TBD	TBD	ns
t_{SDPPW}	\overline{SPIDS} Deassertion Pulse Width (CPHASE=0)	TBD	TBD	ns
<i>Switching Characteristics</i>				
t_{DSOE}	\overline{SPIDS} Assertion to Data Out Active	TBD	TBD	ns
t_{DSDHI}	\overline{SPIDS} Deassertion to Data High Impedance	TBD	TBD	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)	TBD	TBD	ns
$t_{HDSPIIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	TBD	TBD	ns
t_{DSOV}	\overline{SPIDS} Assertion to Data Out Valid (CPHASE = 0)	TBD	TBD	ns

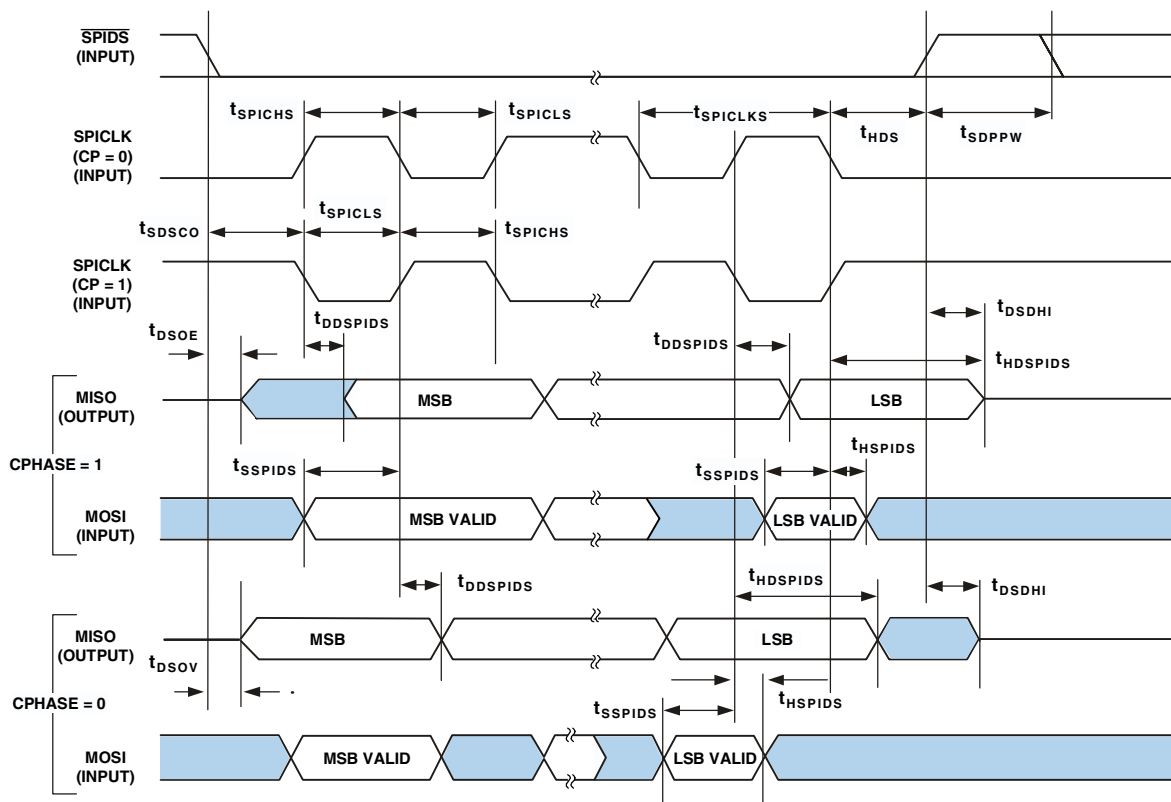


Figure 36. SPI Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 37 describes UART port receive and transmit operations. The maximum baud rate is $PCLK/16$ where $PCLK = 1/tPCLK$. As shown in Figure 37 there is some latency between the gener-

ation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 45. UART Port

Parameter	Min	Max	Unit
<i>Timing Requirement</i>			
t_{RXD}^1 Incoming Data Pulse Width	TBD	TBD	ns
Switching Characteristic	TBD	TBD	
t_{TXD}^1 Outgoing Data Pulse Width	TBD	TBD	ns

¹UART signals RXD and TXD are routed through DPI P14-1 pins using the SRU.

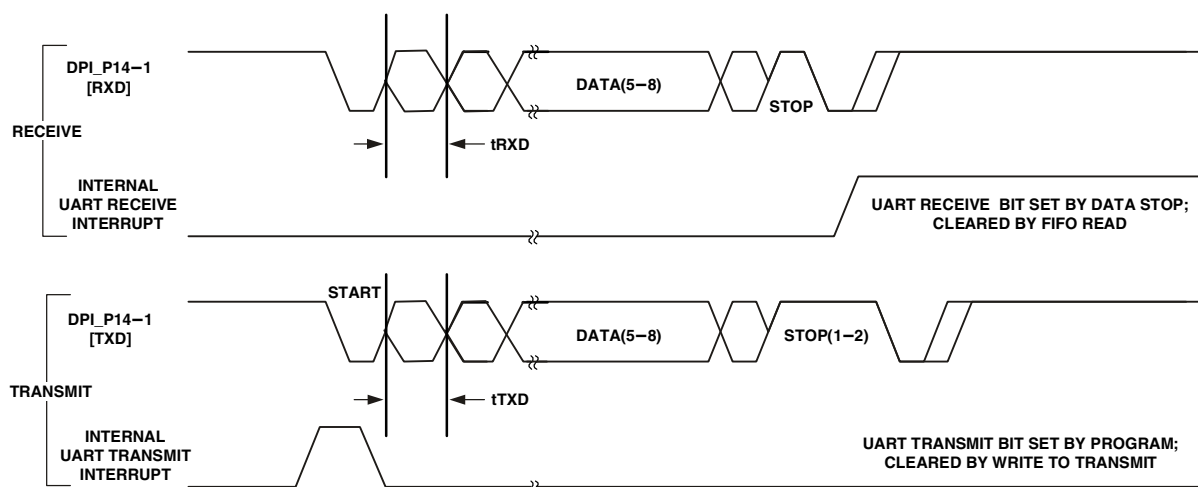


Figure 37. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 46 and Figure 38 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14-1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14-1 pins.

Table 46. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices¹

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	TBD	TBD	TBD	TBD	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	TBD		TBD		μ s
t_{LOW}	Low Period of the SCL Clock	TBD				μ s
t_{HIGH}	High Period of the SCL Clock	TBD				μ s
t_{SUSTA}	Setup Time for a Repeated Start Condition	TBD		TBD		μ s
t_{HDDAT}	Data Hold Time for TWI-bus Devices	TBD		TBD		μ s
t_{SUDAT}	Data Setup Time	TBD		TBD		ns
t_{SUSTO}	Setup Time for Stop Condition	TBD		TBD		μ s
t_{BUF}	Bus Free Time Between a Stop and Start Condition	TBD		TBD		μ s
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	TBD	TBD	ns

¹ All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 17.

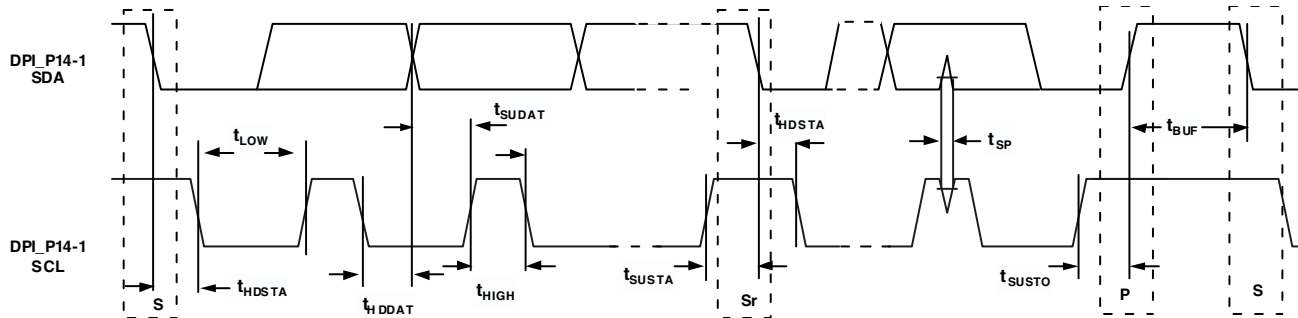


Figure 38. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation**Table 47. JTAG Test Access Port and Emulation**

Parameter		Min	Max	Unit
<i>Timing Requirements</i>				
t_{TCK}	TCK Period	TBD	TBD	ns
t_{STAP}	TDI, TMS Setup Before TCK High	TBD	TBD	ns
t_{HTAP}	TDI, TMS Hold After TCK High	TBD	TBD	ns
t_{SSYS}^1	System Inputs Setup Before TCK High	TBD	TBD	ns
t_{HSYS}^1	System Inputs Hold After TCK High	TBD	TBD	ns
t_{TRSTW}	\overline{TRST} Pulse Width	TBD	TBD	ns
<i>Switching Characteristics</i>				
t_{DTDO}	TDO Delay from TCK Low	TBD	TBD	ns
t_{DSYS}^2	System Outputs Delay After TCK Low	TBD	TBD	ns

¹System Inputs = AD15–0, CLKCFG1–0, \overline{RESET} , BOOTCFG1–0, DAI_Px, and FLAG3–0.

²System Outputs = DAI_Px, AD15–0, $\overline{AMI_RD}$, $\overline{AMI_WR}$, FLAG3–0, CLKOUT, \overline{EMU} , and ALE.

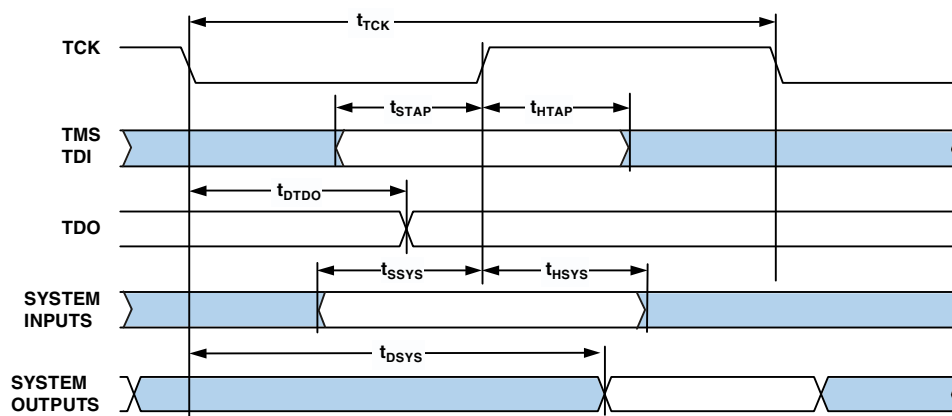


Figure 39. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 40 shows typical I-V characteristics for the output drivers of the ADSP-21469. The curves represent the current drive capability of the output drivers as a function of output voltage.

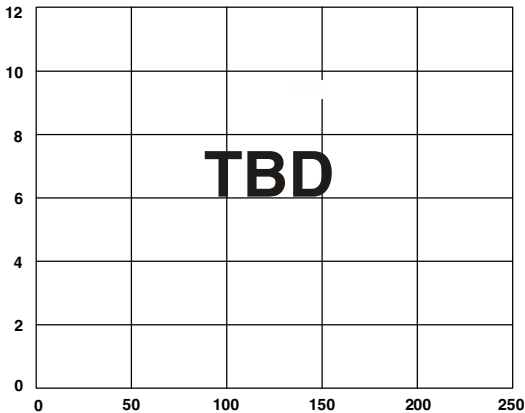


Figure 40. ADSP-21469 Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 16 on Page 23 through Table 47 on Page 49. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 42.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 42. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.



Figure 42. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 41). Figure 45 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 43, Figure 44, and Figure 45 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

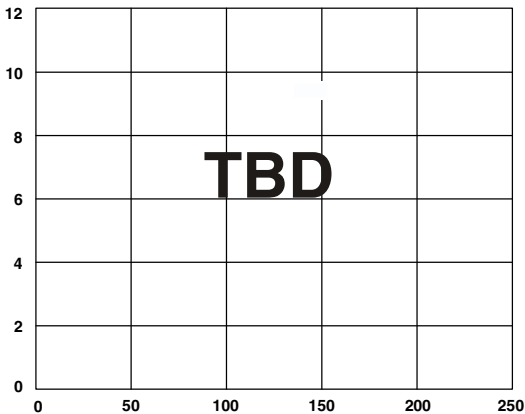
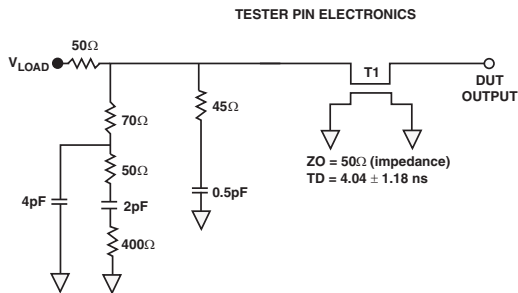


Figure 43. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.
ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 41. Equivalent Device Loading for AC Measurements
(Includes All Fixtures)

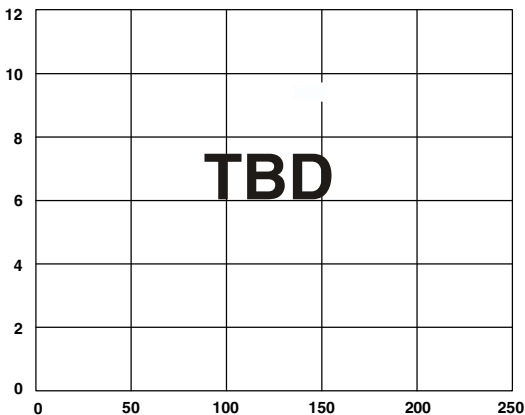


Figure 44. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

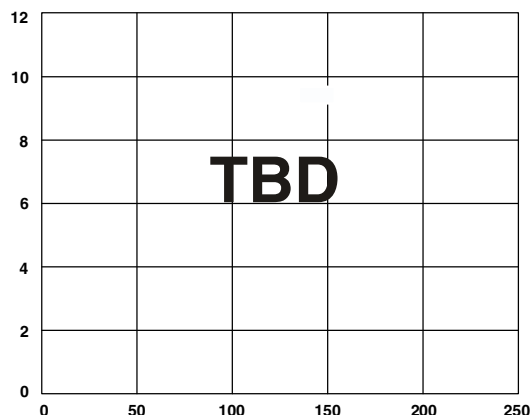


Figure 45. Typical Output Delay or Hold vs. Load Capacitance
(at Ambient Temperature)

THERMAL CHARACTERISTICS

The ADSP-21469 processor is rated for performance over the temperature range specified in [Operating Conditions on Page 16](#).

[Table 48](#) airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL-STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from [Table 48](#).

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in [Table 48](#) are modeled values.

Table 48. Thermal Characteristics for 324-Lead PBGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

BALL CONFIGURATION - ADSP-21469

Figure 46 shows the ball configuration for the ASDP-21469.

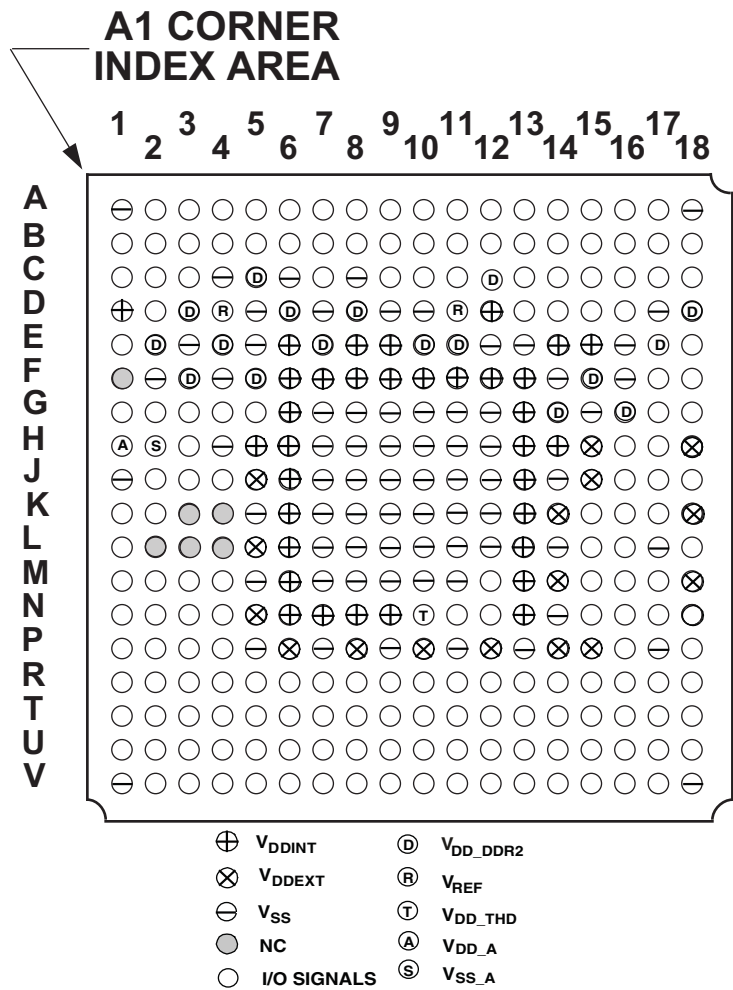


Figure 46. ADSP-21469 Ball Configuration - Pin Out

PBGA PINOUT

Table 49 lists the pin assignments of the ADSP-21469 SHARC processor.

Table 49. 19 mm by 19 mm PBGA Pin Assignment (Alphabetically by Signal)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
AMI_ACK	R10	$\overline{\text{BR3}}$	T8	DDR2_ADDR14	B17	DPI_P3	T1
AMI_ADDR0	V16	$\overline{\text{BR4}}$	V9	DDR2_ADDR15	A17	DPI_P4	R1
AMI_ADDR1	U16	$\overline{\text{BR5}}$	U9	DDR2_BA0	C18	DPI_P5	P1
AMI_ADDR2	T16	$\overline{\text{BR6}}$	T9	DDR2_BA1	C17	DPI_P6	P2
AMI_ADDR3	R16	CLK_CFG0	G1	DDR2_BA2	B18	DPI_P7	P3
AMI_ADDR4	V15	CLK_CFG1	G2	$\overline{\text{DDR2_CAS}}$	C7	DPI_P8	P4
AMI_ADDR5	U15	CLKIN	L1	DDR2_CKE	E1	DPI_P9	N1
AMI_ADDR6	T15	CLKOUT	M2	DDR2_CLK0	B7	DPI_P10	N2
AMI_ADDR7	R15	DAI_P1	R7	$\overline{\text{DDR2_CLK0}}$	A7	DPI_P11	N3
AMI_ADDR8	V14	DAI_P2	V6	DDR2_CLK1	B13	DPI_P12	N4
AMI_ADDR9	U14	DAI_P3	U6	$\overline{\text{DDR2_CLK1}}$	A13	DPI_P13	M3
AMI_ADDR10	T14	DAI_P4	T6	$\overline{\text{DDR2_CS0}}$	C1	DPI_P14	M4
AMI_ADDR11	R14	DAI_P5	R6	$\overline{\text{DDR2_CS1}}$	D1	EMU	K2
AMI_ADDR12	V13	DAI_P6	V5	$\overline{\text{DDR2_CS2}}$	C2	FLAG0	R8
AMI_ADDR13	U13	DAI_P7	U5	$\overline{\text{DDR2_CS3}}$	D2	FLAG1	V7
AMI_ADDR14	T13	DAI_P8	T5	DDR2_DATA0	B2	FLAG2	U7
AMI_ADDR15	R13	DAI_P9	R5	DDR2_DATA1	A2	FLAG3	T7
AMI_ADDR16	V12	DAI_P10	V4	DDR2_DATA2	B3	ID_0	G3
AMI_ADDR17	U12	DAI_P11	U4	DDR2_DATA3	A3	ID_1	G4
AMI_ADDR18	T12	DAI_P12	T4	DDR2_DATA4	B5	ID_2	G5
AMI_ADDR19	R12	DAI_P13	R4	DDR2_DATA5	A5	LACK_0	K17
AMI_ADDR20	V11	DAI_P14	V3	DDR2_DATA6	B6	LACK_1	P17
AMI_ADDR21	U11	DAI_P15	U3	DDR2_DATA7	A6	LCLK_0	J18
AMI_ADDR22	T11	DAI_P16	T3	DDR2_DATA8	B8	LCLK_1	N18
AMI_ADDR23	R11	DAI_P17	R3	DDR2_DATA9	A8	LDAT0_0	E18
AMI_DATA0	U18	DAI_P18	V2	DDR2_DATA10	B9	LDAT0_1	F17
AMI_DATA1	T18	DAI_P19	U2	DDR2_DATA11	A9	LDAT0_2	F18
AMI_DATA2	R18	DAI_P20	T2	DDR2_DATA12	A11	LDAT0_3	G17
AMI_DATA3	P18	DDR2_ADDR0	D13	DDR2_DATA13	B11	LDAT0_4	G18
AMI_DATA4	V17	DDR2_ADDR1	C13	DDR2_DATA14	A12	LDAT0_5	H16
AMI_DATA5	U17	DDR2_ADDR2	D14	DDR2_DATA15	B12	LDAT0_6	H17
AMI_DATA6	T17	DDR2_ADDR3	C14	DDR2_DM0	C3	LDAT0_7	J16
AMI_DATA7	R17	DDR2_ADDR4	B14	DDR2_DM1	C11	LDAT1_0	K18
$\overline{\text{AMI_MS0}}$	T10	DDR2_ADDR5	A14	DDR2_DQS0	A4	LDAT1_1	L16
$\overline{\text{AMI_MS1}}$	U10	DDR2_ADDR6	D15	$\overline{\text{DDR2_DQS0}}$	B4	LDAT1_2	L17
$\overline{\text{AMI_RD}}$	J4	DDR2_ADDR7	C15	DDR2_DQS1	A10	LDAT1_3	L18
$\overline{\text{AMI_WR}}$	V10	DDR2_ADDR8	B15	$\overline{\text{DDR2_DQS1}}$	B10	LDAT1_4	M16
BOOT_CFG0	J2	DDR2_ADDR9	A15	DDR2_ODT	B1	LDAT1_5	M17
BOOT_CFG1	J3	DDR2_ADDR10	D16	$\overline{\text{DDR2_RAS}}$	C9	LDAT1_6	N16
BOOT_CFG2	H3	DDR2_ADDR11	C16	$\overline{\text{DDR2_WE}}$	C10	LDAT1_7	P16
$\overline{\text{BR1}}$	V8	DDR2_ADDR12	B16	DPI_P1	R2	NC	F1
$\overline{\text{BR2}}$	U8	DDR2_ADDR13	A16	DPI_P2	U1	NC	K3

Table 49. 19 mm by 19 mm PBGA Pin Assignment (Alphabetically by Signal)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
NC	K4	VDD_EXT	P14	VSS	D9	VSS	L9
NC	L2	VDD_EXT	P15	VSS	D10	VSS	L10
NC	L3	VDD_INT	D12	VSS	D17	VSS	L11
NC	L4	VDD_INT	E6	VSS	E3	VSS	L12
$\overline{\text{RESET}}$	M1	VDD_INT	E8	VSS	E5	VSS	L14
RPBA	R9	VDD_INT	E9	VSS	E12	VSS	M5
TCK	K15	VDD_INT	E14	VSS	E13	VSS	M7
TDI	L15	VDD_INT	E15	VSS	E16	VSS	M8
TDO	M15	VDD_INT	F6	VSS	F2	VSS	M9
THD_M	N12	VDD_INT	F7	VSS	F4	VSS	M10
THD_P	N11	VDD_INT	F8	VSS	F14	VSS	M11
TMS	K16	VDD_INT	F9	VSS	F16	VSS	M12
$\overline{\text{TRST}}$	N15	VDD_INT	F10	VSS	G7	VSS	N14
VDD_A	H1	VDD_INT	F11	VSS	G8	VSS	N17
VDD_DDR2	C5	VDD_INT	F12	VSS	G9	VSS	P5
VDD_DDR2	C12	VDD_INT	F13	VSS	G10	VSS	P7
VDD_DDR2	D3	VDD_INT	G6	VSS	G11	VSS	P9
VDD_DDR2	D6	VDD_INT	G13	VSS	G12	VSS	P11
VDD_DDR2	D8	VDD_INT	H5	VSS	G15	VSS	P13
VDD_DDR2	D18	VDD_INT	H6	VSS	H4	VSS	V1
VDD_DDR2	E2	VDD_INT	H13	VSS	H7	VSS	V18
VDD_DDR2	E4	VDD_INT	H14	VSS	H8	VREF	D4
VDD_DDR2	E7	VDD_INT	J6	VSS	H9	VREF	D11
VDD_DDR2	E10	VDD_INT	J13	VSS	H10	XTAL	K1
VDD_DDR2	E11	VDD_INT	K6	VSS	H11		
VDD_DDR2	E17	VDD_INT	K13	VSS	H12		
VDD_DDR2	F3	VDD_INT	L6	VSS	J1		
VDD_DDR2	F5	VDD_INT	L13	VSS	J7		
VDD_DDR2	F15	VDD_INT	M6	VSS	J8		
VDD_DDR2	G14	VDD_INT	M13	VSS	J9		
VDD_DDR2	G16	VDD_INT	N6	VSS	J10		
VDD_EXT	H15	VDD_INT	N7	VSS	J11		
VDD_EXT	H18	VDD_INT	N8	VSS	J12		
VDD_EXT	J5	VDD_INT	N9	VSS	J14		
VDD_EXT	J15	VDD_INT	N13	VSS	J17		
VDD_EXT	K14	VDD_THD	N10	VSS	K5		
VDD_EXT	L5	VSS_A	H2	VSS	K7		
VDD_EXT	M14	VSS	A1	VSS	K8		
VDD_EXT	M18	VSS	A18	VSS	K9		
VDD_EXT	N5	VSS	C4	VSS	K10		
VDD_EXT	P6	VSS	C6	VSS	K11		
VDD_EXT	P8	VSS	C8	VSS	K12		
VDD_EXT	P10	VSS	D5	VSS	L7		
VDD_EXT	P12	VSS	D7	VSS	L8		

OUTLINE DIMENSIONS

The ADSP-21469 is available in a 19 mm by 19 mm PBGA lead-free package.

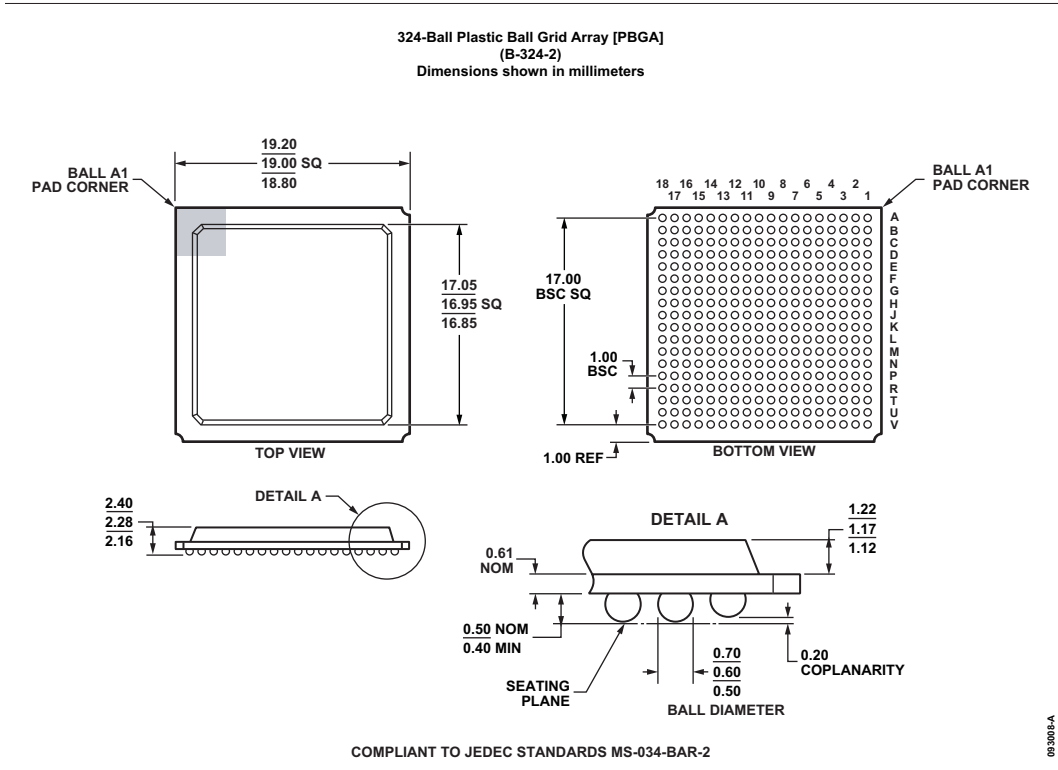


Figure 47. 19 mm by 19 mm 324-Ball PBGA

ORDERING GUIDE

Model	Temperature Range ¹	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ADSP-21469KBZ-ENG ^{2,3,4}	0°C to +70°C	5 Mbit	TBD	324-Ball Plastic Ball Grid Array (PBGA)	B-324-2

¹ Referenced temperature is ambient temperature.

² Z =Part number subject to change.

³ Z =RoHS Compliant Part

⁴ Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC

