

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification.

<http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/MAT02

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
MAT02-903H	Low-noise, matched dual monolithic transistor
MAT02-913H	Radiation Tested, Low-noise, matched dual monolithic transistor

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
H	MACY1-X6	6-Lead can package (TO)

Figure 1 - Terminal connections.

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Collector to base voltage (BV_{CBO})	40V
Collector to emitter voltage (BV_{CEO})	40V
Collector to collector voltage (BV_{CC})	40V
Emitter to emitter voltage (BV_{EE})	40V
Collector current (I_C)	20mA
Emitter current (I_E)	20mA
Total power dissipation ^{1/}	500mW
Operating ambient temperature range	-55 to +125°C
Operating junction temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60 sec)	+300°C
Dice junction temperature range	-65°C to +150°C

^{1/} Rating applies to applications not using heat sinking, device is free air only.

3.1 Thermal Characteristics:

Thermal Resistance, TO-78 (H) Package

Junction-to-Case (Θ_{JC}) = 45°C/W Max

Junction-to-Ambient (Θ_{JA}) = 150°C/W Max

Derate linearly at 6.67 mW/°C for ambient temperatures above 70°C.

Terminal Connections <u>1/</u>	
Terminal	6 lead TO
1	C1
2	B1
3	E1
4	E2
5	B2
6	C2
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	

1/ Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

4.0 Electrical Table:

Table I						
Parameter See notes at end of table	Symbol	Conditions <u>1/</u>	Sub-group	Limit Min	Limit Max	Units
Current Gain	h_{FE}	$I_C = 1\text{mA}; V_{CB} = 0\text{V}, 40\text{V}$	1	500		
			2, 3	275		
		$I_C = 100\mu\text{A}; V_{CB} = 0\text{V}, 40\text{V}$	1	500		
		$I_C = 100\mu\text{A}; V_{CB} = 15\text{V}$	2, 3	225		
		$I_C = 10\mu\text{A}; V_{CB} = 0\text{V}, 40\text{V}$	1	400		
		$I_C = 10\mu\text{A}; V_{CB} = 15\text{V}$	2, 3	175		
		$I_C = 1\mu\text{A}; V_{CB} = 0\text{V}, 40\text{V}$	1	300		
		$I_C = 1\mu\text{A}; V_{CB} = 15\text{V}$	2, 3	150		
Current Gain Match <u>2/</u>	Δh_{FE}	$I_C=10\mu\text{A}, 100\mu\text{A}, 1\text{mA}; V_{CB}=0\text{V}$	1		2	%
Offset Voltage	V_{OS}	$V_{CB} = 0\text{V}$	1		50	μV
			2, 3		80	
Offset Voltage vs. Temperature <u>5/</u>	TCV_{OS}	$V_{CB} = 0\text{V}$			0.3	$\mu\text{V}/^\circ\text{C}$
Offset Voltage vs. V_{CB} <u>3/</u>	$\Delta V_{OS} / \Delta V_{CB}$	$V_{CB} = 0\text{V}, 40\text{V}$	1		25	μV
Offset Voltage vs. Collector Current	$\Delta V_{OS} / \Delta I_C$	$V_{CB} = 0\text{V}; I_C = 10\mu\text{A}, 1\text{mA}$	1		25	
Input Offset Current	I_{OS}	$V_{CB} = 0\text{V}, 40\text{V}$	1		0.6	nA
			2, 3		9.0	
Offset Current vs. V_{CB}	$\Delta I_{OS} / \Delta V_{CB}$	$V_{CB} = 0\text{V}, 40\text{V}$	1		70	pA/V
Bulk Emitter Resistance	r_{BE}		1		0.5	Ω
Collector Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	1		200	pA
Collector Emitter Leakage Current <u>4/</u>	I_{CES}	$V_{CE} = 40\text{V}, V_{BE} = 0\text{V}$	1		200	
Collector-Collector Leakage Current <u>4/</u>	I_{CC}	$V_{CC} = 40\text{V}$	1		200	
Bias Current	I_B	$V_{CB} = 0\text{V}, 40\text{V}$	1		25	nA
			2, 3		60	
Collector Saturation Voltage	V_{CESAT}	$I_C = 1\text{mA}, I_B = 100\mu\text{A}$	1		0.1	V
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu\text{A}$	1	40		
Noise voltage density	e_n	$I_C=1\text{mA},$ $V_{CB}=0\text{V}$	$f_O = 10\text{Hz}$	7	2	$\text{nV}/\sqrt{\text{Hz}}$
			$f_O = 100\text{Hz}$		1	
			$f_O = 1000\text{Hz}$		1	
			$f_O = 10\text{KHz}$		1	

TABLE I NOTES:

- 1/ $V_{CB} = 15V$; $I_C = 10\mu A$, unless otherwise specified.
- 2/ Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)h_{FE} \text{ min}}{I_C}$
- 3/ Measured at $I_C = 10\mu A$ and guaranteed by design over $1\mu A \leq I_C \leq 1mA$.
- 4/ I_{CC} and I_{CES} are verified by measurement of I_{CBO} .
- 5/ Guaranteed by V_{OS} test $\left(TCV_{OS} \cong \frac{V_{OS}}{T} \text{ for } V_{OS} \ll V_{BE} \right)$ $T = 298^\circ K$ for $T_A = +25^\circ C$.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 7
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.

2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFE TEST ENDPOINT	DELTA LIMIT	UNITS
$h_{FE} @ 1mA$	500	420	± 80	nA
$h_{FE} @ 100\mu A$	500	410	± 90	
$h_{FE} @ 10\mu A$	400	300	± 100	
$h_{FE} @ 1\mu A$	300	180	± 120	
IOS	0.6	1.1	± 0.5	

5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Aug. 29, 2000
B	Correct typo at Dice temperature range, change RC package Θ_{JC} from 18 to 35°C/W, correct typo's on table I (subscript), make correction to Table I note 3 (change from "Measured at $I_C = 10\text{mA}$ and guaranteed by design over $10\text{mA} \leq I_C \leq 1\text{mA}$ " to "Measured at $I_C = 10\mu\text{A}$ and guaranteed by design over $1\mu\text{A} \leq I_C \leq 1\text{mA}$ "), add subgroup 7 for e_n , add subgroup 7 to table II, delete subgroups 4, 5, 6 from table II.	Jan. 7, 2002
C	Update web address. Delete burn-in and rad circuits	June 20, 2003
D	Update package offering	Oct. 10, 2007