Low noise, matched, dual PNP transistor

MAT03

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification.
<http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/MAT03

2.0 Part Number.

The complete part number(s) of this specification follow:

Part Number	Description
MAT03-903H	Low noise, matched, dual PNP transistor
MAT03-903L	Low noise, matched, dual PNP transistor
MAT03-913H	Radiation Tested, Low noise, matched, dual PNP transistor
MAT03-913L	Radiation Tested, Low noise, matched, dual PNP transistor

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
H	MACY1-X6	6-Lead can package (TO)
L	GDFP1-F10	10-Lead ceramic flatpack (cerpak)

Figure 1 - Terminal connections.

3.0 Absolute Maximum Ratings.

(T_A = 25°C, unless otherwise noted)

Collector to base voltage (BV_{CBO})....36V
Collector to emitter voltage (BV_{CEO})....36V
Collector to collector voltage (BV_{CC})....36V
Emitter to emitter voltage (BV_{EE})....36V
Collector current (I_C)....20mA
Emitter current (I_E)....20mA
Total power dissipation 1/....500mW
Operating ambient temperature range....-55 to +125°C
Operating junction temperature range....-55°C to +125°C
Storage temperature range....-65°C to +150°C
Lead temperature (soldering, 60 sec)....+300°C
Dice junction temperature range....-65°C to +150°C

1/ Rating applies to applications not using heat sinking, device is free air only.

3.1 **Thermal Characteristics**:

Thermal Resistance, TO-78 (H) Package
Junction-to-Case (Θ_{JC}) = 45°C/W Max
Junction-to-Ambient (Θ_{JA}) = 150°C/W Max
Derate linearly at 6.67 mW/°C for ambient temperatures above 70°C.

Thermal Resistance, cerpac (L) Package
Junction-to-Case (Θ_{JC}) = 80°C/W Max
Junction-to-Ambient (Θ_{JA}) = 180°C/W Max
Derate linearly at 5.56 mW/°C for ambient temperatures above 70°C.

Terminal Connections 1/		
Terminal	6 lead TO	10 lead flatpack
1	C1	C1
2	B1	nc
3	E1	B1
4	E2	nc
5	B2	E1
6	C2	E2
7		nc
8		B2
9		nc
10		C2
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		

1/ Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

4.0 **Electrical Table**:

Table I

Parameter See notes at end of table	Symbol	Conditions 1/		Sub-group	Limit Min	Limit Max	Units
Current gain	h_{FE}	I_C = 1mA, V_{CB} = 0V, -36V		1	100		
				2, 3	70		
		I_C = 100μA, V_{CB} = 0V, -36V		1	90		
		I_C = 100μA, V_{CB} =-36V		2, 3	60		
		I_C = 10μA, V_{CB} = 0V, -36V		1	80		
		I_C = 10μA, V_{CB} = -36V		2, 3	50		
Current gain match 2/	Δh_{FE}	I_C = 100μA, V_{CB} = 0V		1		3	%
Offset voltage	V_{OS}	V_{CB} = 0V		1		100	μV
				2,3		150	
Change in offset voltage vs temperature 3/	TCV_{OS}	V_{CB} = 0V				0.5	μV/°C
Offset voltage change vs V_{CB}	$\Delta V_{OS} / \Delta V_{CB}$	VCB = 0V, -36V		1		150	μV
Offset voltage change vs collector current	$\Delta V_{OS} / \Delta I_C$	I_C1 = 10μA, I_C2 = 1mA, V_{CB}=0V		1		50	
Input offset current	I_{OS}	V_{CB} = 0V, I_C = 100μA		1		35	nA
Bulk emitter resistance	r_{BE}			1		0.75	Ohm
Collector base leakage current	I_{CBO}	V_{CB} = -36V		1		200	pA
Collector saturation voltage	$V_{CE}SAT$	I_C = 1mA, I_B = 100μA		1		0.1	V
Breakdown voltage	BV_{CEO}			1	36		V
Noise voltage density	e_N	IC = 1mA	f_O = 10Hz	7		2	$nV/\sqrt{Hz}$
		VCB = 0V	f_O = 100Hz			1	
			f_O = 1000Hz			1	
			f_O = 10000Hz			1	

TABLE I NOTES:

1/ V_{CB} = -15V, I_C = 10μA, unless otherwise specified.

2/ Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B) h_{FE} \min}{I_C}$.

3/ Guaranteed by VOS test ($TC_{VOS} = V_{OS}/T$ for $V_{OS} << V_{BE}$) (T = 298°K for T_A = +25°C).

4.1 **Electrical Test Requirements**:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 1/ 2/
Group A Test Requirements	1, 2, 3, 7
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for delta parameters. See table I for conditions.

4.2 **Table III. Burn-in test delta limits**.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
h_{FE} @ 1mA	100 min	60 min	±40	
h_{FE} @ 100µA	90 min	54 min	±36	
h_{FE} @ 10µA	80 min	48 min	±32	
IOS	35	55	±20	nA

5.0 **Life Test/Burn-In Circuit:**
5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	July 24, 2000
B	Page 1: Update web address; correct typo for dice junction temperature. Page 2: change RC package theta JC from 18 to 35 °C Page 3: delete text “note 1” under table I conditions; change delta hFE condition from mA to µA; delete subgroups for TCVOS; format note numbers for table I; change note 3 from ” This is the maximum change in VOS measured at IC = 10mA with VCB = 0V” TO “Guaranteed by VOS test (TC_{VOS} = V_{OS}/T for V_{OS} << V_{BE}) (T = 298°K for T_A = +25°C)” Page 4, Table II: delete subgroup 7 from final electricals Page 5: add resistor values to burn-in figure.	Jan. 22, 2002
C	Change R3 of BI circuit from 2.5K to 10K ohm.	Apr. 17, 2002
D	Update web address. Delete burn-in circuit.	June 20, 2003
E	Update package offering	Oct. 10, 2007