8-Channel JFET Analog Multiplexer

MUX08

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/MUX08

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
MUX08-903Q	8-channel JFET analog multiplexer
MUX08-903RC	8-channel JFET analog multiplexer
MUX08-913Q	Radiation Tested, 8-channel JFET analog multiplexer
MUX08-913RC	Radiation Tested, 8-channel JFET analog multiplexer

2.1 Package Description: (see figure 1 for terminal connections)

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Q	GDIP1-T16	16-Lead ceramic dual-in-line package (CERDIP)
RC	CQCC1-N20	20 terminal leadless chip carrier (LCC)

3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

Positive supply voltage ..... +18V
Negative supply voltage ..... -18V
Logic input voltage ..... (-4V or V_{EE}) to V_{CC}
Analog input voltage ..... V_{EE} - 20V to V_{CC} + 20V
Maximum current through any pin 25mA
Storage temperature range ..... -65°C to +150°C
Power dissipation (P_D) 500mW
Lead temperature (soldering, 60 seconds) ..... +300°C
Junction temperature (T_J) ..... +150°C
Thermal resistance, junction to case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, Junction to ambient (θ_{JA})
- Case Q ..... 91°C/W
- Case RC ..... 110°C/W

		Package	
		Q	RC
Terminal Number	1	A_O	n.c.
	2	ENABLE	A_O
	3	V_{EE}	ENABLE
	4	S1	V_{EE}
	5	S2	S1
	6	S3	n.c.
	7	S4	S2
	8	DRAIN	S3
	9	S8	S4
	10	S7	DRAIN
	11	S6	n.c.
	12	S5	S8
	13	V_{CC}	S7
	14	GND	S6
	15	A_2	S5
	16	A_1	n.c.
	17		V_{CC}
	18		GND
	19		A_2
	20		A_1

Figure 1 - Terminal connections.

A2	A1	A0	ENABLE	"0n" Channel
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Figure 2 - Truth Table

4.0 **Electrical Table**:

Parameter See notes at end of table	Symbol	Conditions V_S = ±15V unless otherwise specified		Sub-group	Limit Min	Limit Max	Units
Positive supply current	I_{CC}			1		12	mA
				2, 3		15	
Negative supply current	I_{EE}			1	-3.8		
				2, 3	-5		
Digital input current	I_{IN}	V_{IN} = 0.4V to 15V		1		±10	µA
				2, 3		±20	
Digital "0" enable current	$I_{IN(EN)}$	$V_{IN(EN)}$ = 0.4V		1		±10	
				2, 3		±20	
"ON" resistance	R_{ON}	-10V < V_S < +10V, I_S = 200 µA		1		300	Ω
				2, 3		400	
"ON" resistance change with change in source voltage 1/	$\Delta R_{ON}/\Delta V_S$	-10V < V_S < +10V, I_S = 200 µA		1		5	%
				2		7	
				3		6	
RON match between switches 4/	R_{ON} MATCH	V_S = 0V, I_S = 200 µA		1		15	
				2		20	
				3		18	
Analog voltage range 1/	V_A			1, 2, 3	±10		V
Source current (OFF)	$I_{S(OFF)}$	V_S = +10V, V_D = -10V 3/	V_{IL} = 0.8V	1, 3		±1	nA
			V_{IL} = 0.7V	2		±25	
Drain current (OFF)	$I_{D(OFF)}$		V_{IL} = 0.8V	1, 3		±1	
			V_{IL} = 0.7V	2		±100	
Leakage current, switch (ON)	$I_{S(ON)}$ + $I_{D(ON)}$	V_S = V_D = +10V, V_{IH} = 2V 3/		1, 3		±1	
				2		±100	
Digitial "0" input voltage 1/	V_{IL}			1, 3		0.8	V
				2		0.7	
Digital "1" input voltage 1/	V_{IH}			1, 2, 3	2.0		
Functional testes 2/				1, 2, 3	--	--	
Switching time	t_{PHL}	V_{S1} = +10V, V_{S8} = -10V, R_L =		9		2.1	µS
	t_{PLH}	10MΩ, C_L = 10pF, see fig. 4 & 5		10, 11		3.5	
Enable delay "ON"	$t_{ON(EN)}$	V_{S1} = -10V, C_L = 10pF,		9		2.0	
		R_L = 1KΩ, see fig. 5 & 6		10, 11		3.0	
Enable delay "OFF"	$t_{OFF(EN)}$			9		0.4	
				10, 11		1.0	
Break-before-make delay	t_{OPEN}	V_S1 = V_S8 = -1V, see fig. 5 & 7		9	0.1		

TABLE I NOTES:

1/ Guaranteed, if not tested, to the specified limits
2/ Verified by leakage tests
3/ Conditions applied to leakage tests insure worst case leakages.
4/ $R_{ON\ MATCH}$ specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{1}{N}\frac{N}{\sum_{i=1} Ri}$$ with N = number of channels, Ri = each channel's "ON" resistance.

4.1 **Electrical Test Requirements**:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 9 1/ 2/
Group A Test Requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. Delta limits are excluded from PDA
2/ See table III for delta limits.

4.2 **Table III. Burn-in test delta limits**.

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
R_{ON}	300	50	Ohm

5.0 **Life Test/Burn-In Circuit:**

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

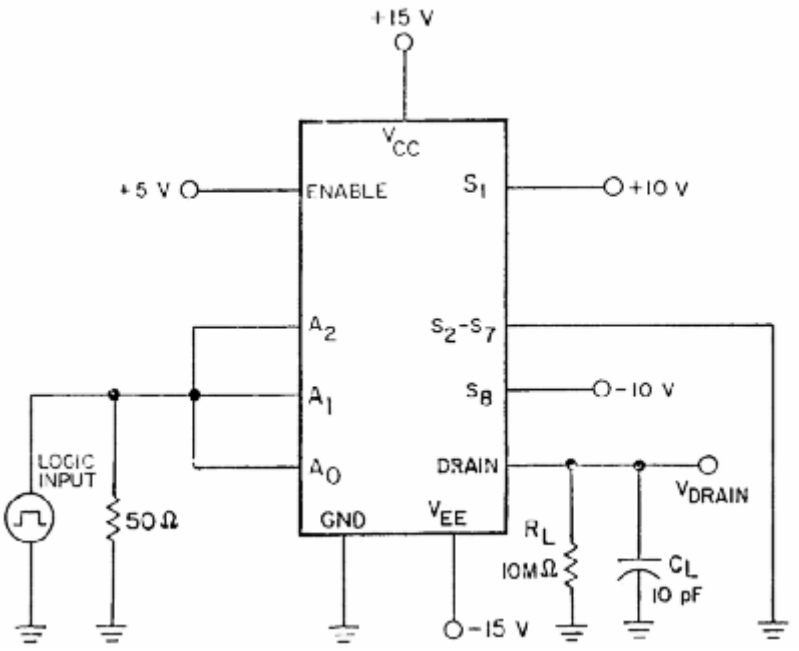

Figure 4 - Transition time test circuit

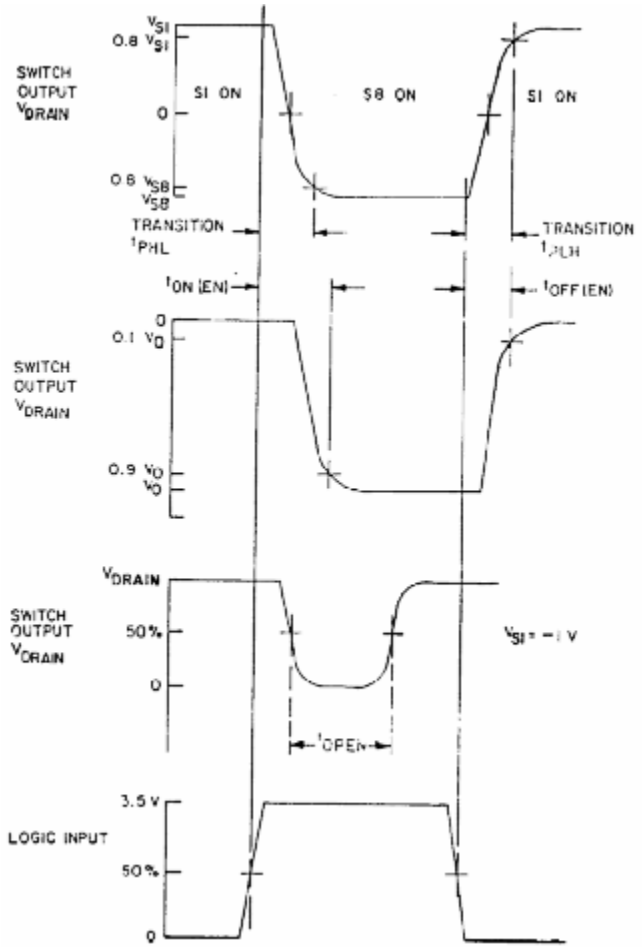

Figure 5 - Switching time waveforms

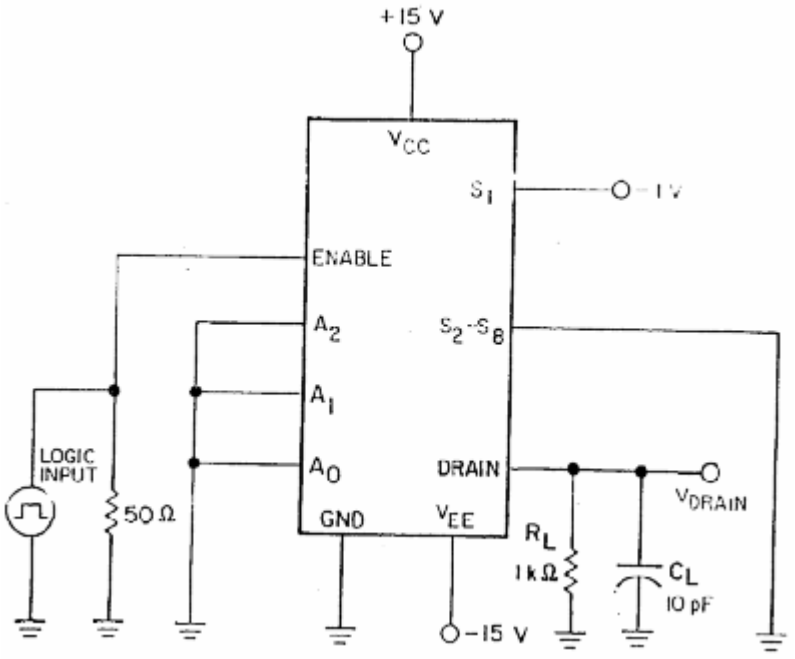

Figure 6 - Enable delay time test circuit

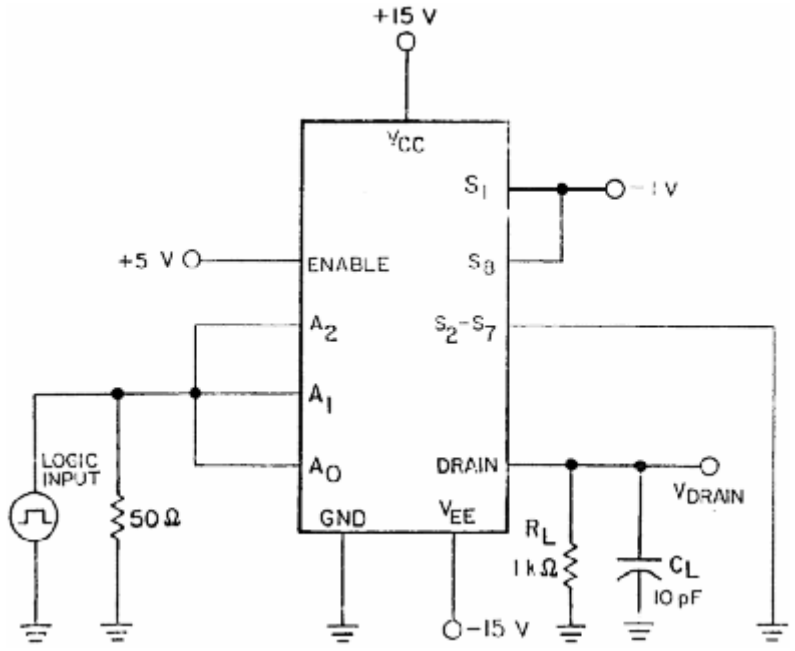

Figure 7 - Break-before-make test circuit

Rev	Description of Change	Date
A	Initiate	June 30, 2000
B	Update web address	Feb. 18, 2002
C	Update web address. Remove Burn-In and rad bias circuits.	15-May-03