

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification.

<http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/MUX16

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
MUX16-903T	16-channel JFET analog multiplexer
MUX16-903TC	16-channel JFET analog multiplexer
MUX16-913T	Radiation Tested, 16-channel JFET analog multiplexer
MUX16-913TC	Radiation Tested, 16-channel JFET analog multiplexer

2.1 Package Description: (see figure 1 for terminal connections)

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
T	GDIP1-T28	28-Lead ceramic dual-in-line package (CERDIP)
TC	CQCC1-N28	28 terminal leadless chip carrier (LCC)

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Positive supply voltage	+18V
Negative supply voltage.....	-18V
Logic input voltage	(-4V or V_{EE}) to V_{CC}
Analog input voltage	$V_{EE} - 20\text{V}$ to $V_{CC} + 20\text{V}$
Maximum current through any pin	25mA
Storage temperature range	-65°C to $+150^\circ\text{C}$
Power dissipation (P_D)	1200mW
Lead temperature (soldering, 60 seconds)	$+300^\circ\text{C}$
Junction temperature (T_J).....	$+150^\circ\text{C}$
Thermal resistance, junction to case (θ_{JC}).....	See MIL-STD-1835
Thermal resistance, Junction to ambient (θ_{JA})	
Case T	55°C/W
Case TC.....	108°C/W

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Terminal Number	Function	
	1	V _{CC}
	2	n.c.
	3	n.c.
	4	S16
	5	S15
	6	S14
	7	S13
	8	S12
	9	S11
	10	S10
	11	S9
	12	GND
	13	n.c.
	14	A3
	15	A2
	16	A1
	17	A0
	18	Enable
	19	S1
	20	S2
	21	S3
	22	S4
	23	S5
	24	S6
	25	S7
	26	S8
	27	V _{EE}
	28	Drain

Figure 1 - Terminal connections.

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A3	A2	A1	A0	ENABLE	"ON" Channel
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

Figure 2 - Truth Table

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4.0 Electrical Table:

Parameter See notes at end of table	Symbol	Conditions V _S = ±15V unless otherwise specified		Sub- group	Limit Min	Limit Max	Units	
Positive supply current	I _{CC}			1		19	mA	
				2, 3		24		
Negative supply current	I _{EE}			1	-7.0			
				2, 3	-8.2			
Digital input current	I _{IN}	V _{IN} = 0.4V to 15V		1		±10	µA	
				2, 3		±20		
Digital "0" enable current	I _{IN(EN)}	V _{IN(EN)} = 0.4V		1		±10		
				2, 3		±20		
"ON" resistance	R _{ON}	-10V < V _S < +10V, I _S = 200 µA		1		380	Ω	
				2, 3		500		
"ON" resistance change with change in source voltage <u>1/</u>	ΔR _{ON} / ΔV _{SOURCE}	-10V < V _S < +10V, I _S = 200 µA		1, 2		5.0	%	
				3		7.0		
R _{ON} match between switches <u>4/</u>	R _{ON} MATCH	V _S = 0V, I _S = 200 µA		1, 2		15		
				3		18		
Analog voltage range <u>1/</u>	V _A			1, 2, 3	±10		V	
Source current (OFF)	I _{S(OFF)}	VS = +10V, VD = -10V <u>3/</u>	VIL = 0.8V	1, 3		±1	nA	
Drain current (OFF)	I _{D(OFF)}		VIL = 0.7v	2		±25		
			VIL = 0.8V	1, 3		±1		
			VIL = 0.7v	2		±75		
Leakage current, switch (ON)	I _{S(ON)} + I _{D(ON)}	VS = VD = +10V, VIH = 2V <u>3/</u>		1, 3		±1		
				2		±75		
Digital "0" input voltage <u>1/</u>	VIL			1, 3		0.8	V	
				2		0.7		
Digital "1" input voltage <u>1/</u>	VIH			1, 2, 3	2.0			
Functional testes <u>2/</u>				1, 2, 3				
Switching time	t _{PHL}	V _{S1} = +10V, V _{S16} = -10V, R _L = 10MΩ, C _L = 10pF, see fig. 5 & 6		9		2.0	µS	
	t _{PLH}			10, 11		3.5		
Enable delay "ON"	t _{ON(EN)}	V _{S1} = -10V, C _L = 10pF, R _L = 1KΩ, see fig. 6 & 7		9		2.0		
				10, 11		3.0		
Enable delay "OFF"	t _{OFF(EN)}			9		0.5		
				10, 11		1.0		
Break-before-make delay	t _{OPEN}	VS1 = VS8 = -1V, see fig. 6 & 8		9	0.2			

TABLE I NOTES:

- 1/ Guaranteed, if not tested, to the specified limits
- 2/ Verified by leakage tests
- 3/ Conditions applied to leakage tests insure worst case leakages.
- 4/ $R_{ON\ MATCH}$ specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{1}{N} \frac{N}{\sum_{i=1} R_i} \text{ with } N = \text{number of channels, } R_i = \text{each channel's "ON" resistance.}$$

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 9 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

- 1/ PDA applies to Subgroup 1 only. Delta limits are excluded from PDA
- 2/ See table III for delta limits.

4.2 Table III. Burn-in test delta limits.

Table III			
TEST TITLE	ENDPOINT LIMIT	DELTA LIMIT	UNITS
R_{ON}	380	50	Ohm

5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

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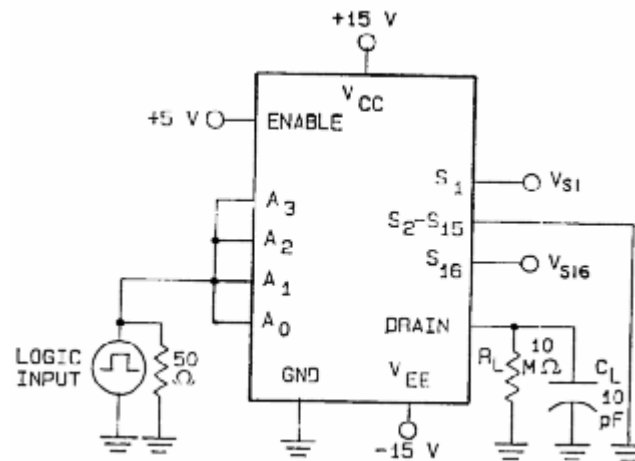


Figure 5 - Switching time test circuit

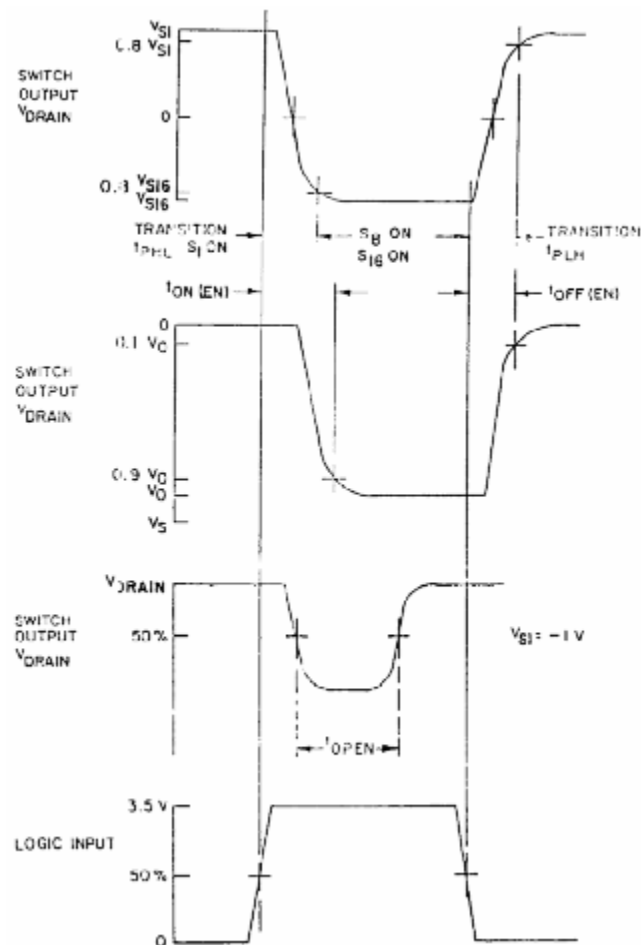


Figure 6 - Switching time waveforms

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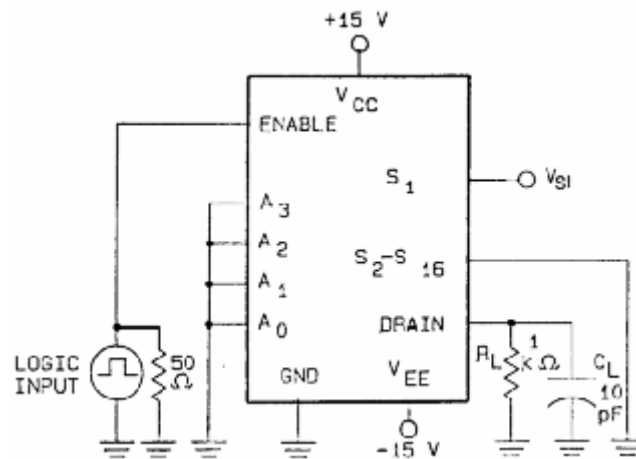


Figure 7 - Enable delay time test circuit

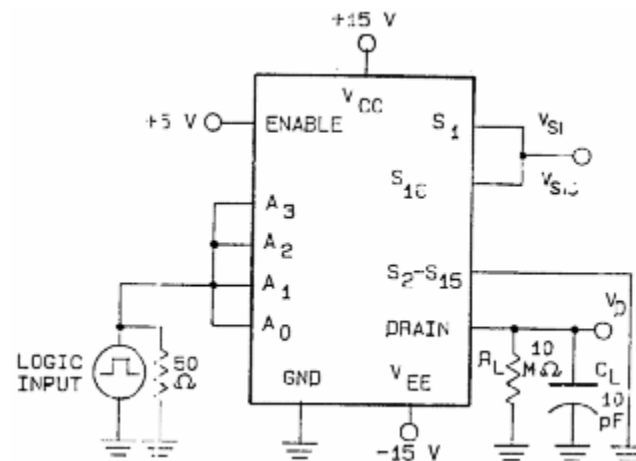


Figure 8 - Break-before-make test circuit

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Rev	Description of Change	Date
A	Initiate	June 30, 2000
B	Change t_{OPEN} from 2.0 μ S min to 0.2 μ S min (typo)	March 21, 2001
C	Update web address. Renumber Figures into sequential order.	Feb. 18, 2002
D	Update web address. Delete burn-in and rad circuits	June 20, 2003