

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification.

<http://www.analog.com/aerospace>

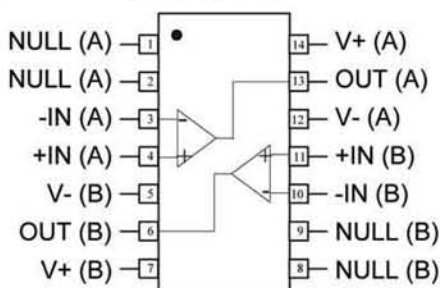
This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete datasheet for commercial product grades can be found at www.analog.com/OP227

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
OP227-903Y	Dual, low-offset, low noise operational amplifier
OP227R903Y	Radiation Tested, Dual, low-offset, low noise operational amplifier
OP227-903M	Dual, low-offset, low noise operational amplifier
OP227R903M	Radiation Tested, Dual, low-offset, low noise operational amplifier

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
Y	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)
M	GDFP1-F14	14-Lead ceramic flat pack (CERPAK)



NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B
2. V-(A) and V-(B) are internally connected via substrate resistance.

Figure 1 - Terminal connections.

3.0 Absolute Maximum Ratings. 1/

Supply voltage (V)	±22 V dc CC
Input voltage range (V)	±22 V dc IN
Output short circuit duration	Indefinite
Differential input current <u>2/</u>	±25 mA
Differential input voltage range	±0.7 V dc
Lead temperature (soldering, 60 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) <u>3/</u>	500 mW

NOTES:

- 1/ Unless otherwise specified, all voltages are referenced to ground.

- 2/ The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ± 0.7 V, the input current should be limited to 25 mA.
- 3/ For T greater than 106°C, derate linearly at 11.3 mW/°C.

3.1 Thermal Characteristics:

Thermal Resistance, Y (cerdip) Package

Junction-to-Case (Θ_{JC}) = 29°C/W Max

Junction-to-Ambient (Θ_{JA}) = 91°C/W Max

Thermal Resistance, M (cerpak) Package

Junction-to-Case (Θ_{JC}) = 90°C/W Max

Junction-to-Ambient (Θ_{JA}) = 150°C/W Max

4.0 Electrical Table:

Table I

Parameter See notes at end of table	Symbol	Conditions Note 1	Sub-group	Limit Min	Limit Max	Units
Input offset voltage	V_{IO}	M, D, L, R	1		80	μ V
			2, 3		180	
			1		160	
Average input offset drift <u>2/</u> <u>4/</u>	TCV_{IO}		1, 2, 3		1.0	μ V/°C
Input offset current	I_{IO}	M, D, L, R	1		± 35	nA
			2, 3		± 50	
			1		± 120	
Input bias current	I_{IB}	M, D, L, R	1		± 40	
			2, 3		± 60	
			1		± 1200	
Power supply rejection ratio <u>4/</u>	PSRR	$V_S = \pm 4V$ to $\pm 18V$	1		10	μ V/V
		$V_S = \pm 4.5V$ to $\pm 18V$	2, 3		16	
Common mode rejection ratio <u>4/</u>	CMRR	$V_{CM} = \pm 11V$	1	114		dB
		$V_{CM} = \pm 10V$	2, 3	108		
Large signal voltage gain	A_{VOL}	$V_O = \pm 10V$, $R_L = 2K\Omega$	4	1000		V/mV
			5, 6	600		
		M, D, L, R	4	500		
			4	800		
Input voltage range <u>4/</u>	IVR		1	± 11		V
			2, 3	± 10		
Output voltage swing <u>4/</u>	V_O	$RL = 2K\Omega$	4	± 12		
		$RL = 600\Omega$	5, 6	± 11.5		
			4	± 10		
Slew rate <u>2/</u> <u>4/</u>	SR	$RL = 2K\Omega$	7	1.7		V/ μ S
Input noise voltage <u>4/</u>	e_N	$f_O = 1$ to 100Hz	7		50	nV _{RMS}
Gain bandwidth product <u>2/</u> <u>4/</u>	GBW	$f = 100kHz$	7	5.0		MHz
Input offset voltage match <u>4/</u>	V_{OS}		1		80	μ V
			2, 3		180	
Average non-inverting bias current <u>4/</u>	I_{B+}	<u>3/</u>	1		± 40	nA
			2, 3		± 60	
Non-inverting offset current <u>4/</u>	I_{OS+}	$I_{OS+} = I_{B+A} - I_{B+B}$	1		± 60	
			2, 3		± 90	
Inverting offset current <u>4/</u>	I_{OS-}	$I_{OS-} = I_{B-A} - I_{B-B}$	1		± 60	
			2, 3		± 90	

TABLE I NOTES:

1/ $V_S = \pm 15V$, unless otherwise specified

2/ Guaranteed but not tested.

3/ $I_{B+} = \frac{(I_{B+} + A) + (I_{B+} + B)}{2}$

4/ Not tested post irradiation.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.

2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Burn-in/Life Test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	GROUP C ENDPOINT	DELTA LIMIT	UNITS
VOS	±80	±180	±100	μV
±IB	±40	±50	±10	nA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	July 18, 2000
B	Update web address	Feb. 18, 2002
C	Add note 2 to TCVIO, Guaranteed if not tested, ref SMD 86887	Nov. 22, 2002
D	Update web address. Add note 4 to indicate parameters not test post irradiation	May 13, 2003
E	Delete burn-in and radiation bias circuits	Aug. 5, 2003
F	Add OP227-903M & OP227R903M versions	Jul. 29, 2004