

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/SMP11

2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
SMP11-803Y	Low Droop Rate/Accurate Sample and Hold
SMP11-813Y	Radiation Tested, Low Droop Rate/Accurate Sample and Hold

2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designer</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
Y	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)

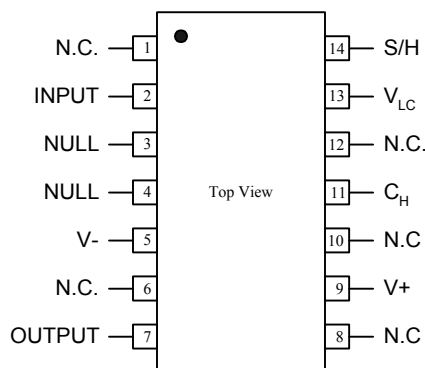


Figure 1 - Terminal connections.

3.0 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Supply Voltage.....	$\pm 36\text{V}$
Power Dissipation.....	500mW
Input Voltage	Supply Voltage
Logic and Logic Reference Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Hold Capacitor Short-Circuit Duration.....	60 sec.
Operating Temperature Range.....	-55°C to $+125^\circ\text{C}$
Storage Temperature Range.....	-65°C to $+150^\circ\text{C}$
DICE Junction Temperature Range (T_J).....	$+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec.).....	$+300^\circ\text{C}$

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Rev. F

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3.1 Thermal Characteristics:

Thermal Resistance, CERDIP (Y) Package

Junction-to-Case (Θ_{JC}) = 29°C/W Max

Junction-to-Ambient (Θ_{JA}) = 100 °C/W Max

4.0 Electrical Table:

Table I						
Parameter See notes at end of table	Symbol	Conditions (Note 1)	Sub-group	Limit Min	Limit Max	Units
Zero Scale Error (Hold mode)	V_{ZS}	$V_{S/H} = 3.5V$ (500 μ S after hold) $V_{IN} = 0V$	1		± 3.0	mV
			2, 3		± 5.5	
Input Bias Current	I_B	$V_{IN} = 0V$	1		± 120	nA
			2, 3		± 280	
Input voltage range or Output Voltage swing	V_{SW}	$R_L = 2.5K\Omega$	1, 2, 3	± 10.5		V
Power Supply Rejection Ratio	PSRR	$V_+ = \pm 9V$ to $\pm 18V$ Sample mode	1	77		dB
			2, 3	72		
Differential logic threshold	V_{TH}		1	0.8	2.0	V
			2, 3	0.6	2.0	
Logic control input current	I_{LC}	$V_{LC} = 0V$	1		-3	μ A
			2, 3		-5	
Supply Current	I_{SY}		1	2	7.0	mA
			2, 3	2	8.4	
Logic input current	$I_{S/H}$	$V_{S/H} = 0.6V$ (Sample mode)	1, 2, 3		-15	μ A
		$V_{S/H} = 5V$ (Hold mode)	1, 2, 3	-1	1	
Droop Rate	$\Delta V_{CH}/\Delta t$		4		500	μ V/mS
			5		5000	
			6		2000	
Leakage (Droop) Current	I_{DR}		4		2.5	nA
			5		25	
			6		10	
Voltage Gain (sample mode)	A_V	$V_{IN} = \pm 10V$, $R_L = 5K\Omega$ or	4	0.99953		V/V
		$V_{IN} = \pm 5V$, $R_L = 2.5K\Omega$	5, 6	0.99940		
Hold Capacitor Charging Current	ICH+	$V_{IN} - V_{OUT} \geq +3V$	4, 5, 6	15		mA
	ICH-	$V_{IN} - V_{OUT} \leq -3V$	4, 5, 6	-15		
Sample/Hold current ratio	I_{CH}/I_{DR}		1, 2, 3	2×10^6		mA/mA
Slew Rate Aperture Time	SR	$V_{IN} = \pm 10V$, $R_L = 2.5K\Omega$	9	2.5		V/ μ S
	Tap		9 2/		100	nS
Acquisition Time	Taq1	10V step to 0.1%	9		7	μ S
	Taq2	10V step to 0.01%	9		10	
Hold mode settling time	T_{HM}	Settling to 1mV of final value	9		4.5	

TABLE I NOTES:

- $V_S = \pm 15V$, $C_H = 5000pF$, V_{LC} connected to ground, unless otherwise specified.
- Subgroup 9 is sample tested.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6 <u>1/</u> <u>2/</u>
Group A Test Requirements	1, 2, 3, 4, 5, 6, 9
Group C end-point electrical parameters	1 <u>2/</u>
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

2/ See table III for delta parameters. Exclude Delta's from PDA.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
V _{ZS}	±3	±5	±2	mV
I _B	120	132	±12	nA
I _{SY}	7	7.7	±0.7	mA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.

5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.

5.3 Steady state life test is per MIL-STD-883 Method 1005.

6.0 Radiation Test: Per 883 Methods 1019/5004. No Lot Jeopardy

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Rev	Description of Change	Date
A	Initiate	Apr. 4, 08
B	Table III IB from 90nA to 120 nA. Delta IB from 6.5 to 12 nA. Add Delta ISY. Change subgroup 11 to 9. Delete Figs. 2 & 3. Update Table III.	Aug. 1, 2001
C	Update web address. Correct typo on Table I, V_{TH} min at temp is 0.6, not .06. Table II, add “exclude delta’s from PDA” to note 2.	Mar. 6, 2002
D	Update web address.	June 20, 2003
E	Update header/footer and add to 1.0 Scope description	Feb. 15, 2008
F	Remove range from DICE Junction Temperature (T_J)	April 4, 2008