Low Power Audio Codec

# SSM2603

## FEATURES

**Stereo, 24-bit analog-to-digital and digital-to-analog converters**
**DAC SNR: 100 dB (A-weighted), THD: −80 dB at 48 kHz, 3.3 V**
**ADC SNR: 90 dB (A-weighted), THD: −80 dB at 48 kHz, 3.3 V**
**Highly efficient headphone amplifier**
**Stereo line input and monaural microphone input**
**Low power**
- **7 mW stereo playback (1.8 V/1.5 V supplies)**
- **14 mW record and playback (1.8 V/1.5 V supplies)**

**Low supply voltages**
- **Analog: 1.8 V to 3.6 V**
- **Digital core: 1.5 V to 3.6 V**
- **Digital I/O: 1.8 V to 3.6 V**

**256/384 oversampling rate in normal mode; 250/272 oversampling rate in USB mode**
**Audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz**
**28-lead, 5 mm × 5 mm LFCSP (QFN) package**

## APPLICATIONS

**Mobile phones**
**MP3 players**
**Portable gaming**
**Portable electronics**
**Educational toys**

## GENERAL DESCRIPTION

The SSM2603 is a low power, high quality stereo audio codec for portable digital audio applications with one set of stereo programmable gain amplifier (PGA) line inputs and one monaural microphone input. It features two 24-bit analog-to-digital converter (ADC) channels and two 24-bit digital-to-analog (DAC) converter channels.

The SSM2603 can operate as a master or a slave. It supports various master clock frequencies, including 12 MHz or 24 MHz for USB devices; standard 256 $f_S$ or 384 $f_S$ based rates, such as 12.288 MHz and 24.576 MHz; and many common audio sampling rates, such as 96 kHz, 88.2 kHz, 48 kHz, 44.1 kHz, 32 kHz, 24 kHz, 22.05 kHz, 16 kHz, 12 kHz, 11.025 kHz, and 8 kHz.

The SSM2603 can operate at power supplies as low as 1.8 V for the analog circuitry and as low as 1.5 V for the digital circuitry. The maximum voltage supply is 3.6 V for all supplies.

The SSM2603 software-programmable stereo output options provide the user with many application possibilities because the device can be used as a headphone driver or as a speaker driver. Its volume control functions provide a large range of gain control of the audio signal.

The SSM2603 is specified over the industrial temperature range of −40°C to +85°C. It is available in a 28-lead, 5 mm × 5 mm lead frame chip scale package (LFCSP).

## FUNCTIONAL BLOCK DIAGRAM

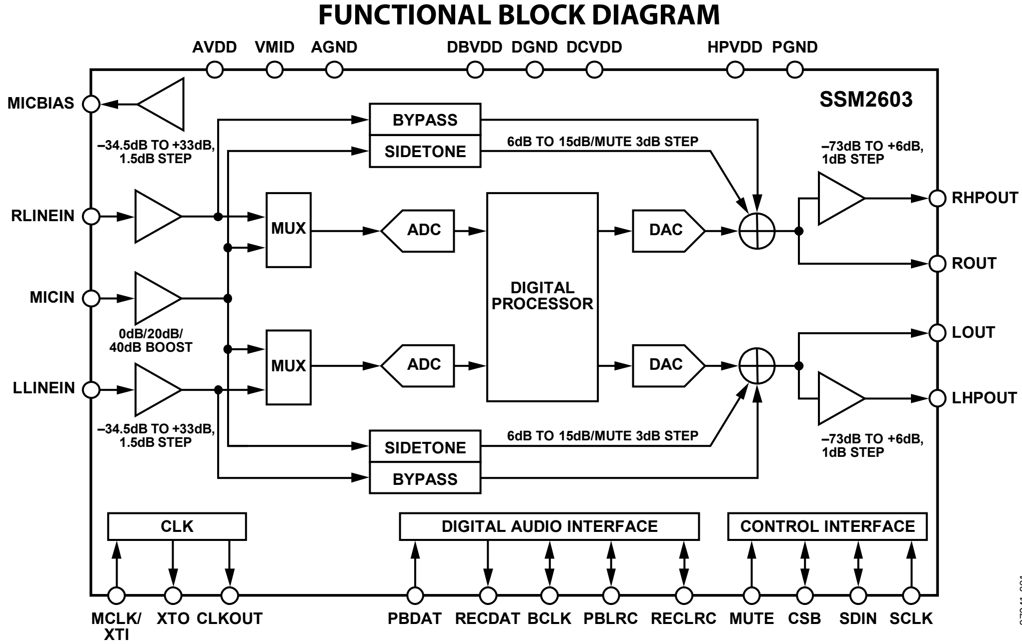


*Figure 1.*



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# TABLE OF CONTENTS



## REVISION HISTORY

**2/08—Revision 0: Initial Version**

# SPECIFICATIONS

$T_A$ = 25°C, AVDD = DVDD = 3.3 V, PVDD = 3.3 V, 1 kHz signal, $f_S$ = 48 kHz, PGA gain = 0 dB, 24-bit audio data, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Analog Voltage Supply (AVDD) | 1.8 | 3.3 | 3.6 | V | |
| Digital Power Supply | 1.5 | 3.3 | 3.6 | V | |
| Ground (AGND, PGND, DGND) | | 0 | | V | |
| POWER CONSUMPTION | | | | | |
| Power-Up | | | | | |
| Stereo Record (1.5 V and 1.8 V) | | 7 | | mW | |
| Stereo Record (3.3 V) | | 22 | | mW | |
| Stereo Playback (1.5 V and 1.8 V) | | 7 | | mW | |
| Stereo Playback (3.3 V) | | 22 | | mW | |
| Power-Down | | | 40 | μW | |
| LINE INPUT | | | | | |
| Input Signal Level (0 dB) | | 1 × AVDD/3.3 | | V rms | |
| Input Impedance | | 200 | | kΩ | PGA gain = 0 dB |
| | | 10 | | kΩ | PGA gain = +33 dB |
| | | 480 | | kΩ | PGA gain = −34.5 dB |
| Input Capacitance | | 10 | | pF | |
| Signal-to-Noise Ratio (A-Weighted) | 70 | 90 | | dB | PGA gain = 0 dB, AVDD = 3.3 V |
| | | 84 | | dB | PGA gain = 0 dB, AVDD = 1.8 V |
| Total Harmonic Distortion (THD) | | −80 | | dB | −1 dBFS input, AVDD = 3.3 V |
| | | −75 | | dB | −1 dBFS input, AVDD = 1.8 V |
| Channel Separation | | 80 | | dB | |
| Programmable Gain | −34.5 | 0 | +33.5 | dB | |
| Gain Step | | 1.5 | | dB | |
| Mute Attenuation | | −80 | | dB | |
| MICROPHONE INPUT | | | | | |
| Input Signal Level | | 1 | | V rms | |
| Signal-to-Noise Ratio (A-Weighted) | | 85 | | dB | Microphone gain = 0 dB ($R_{SOURCE}$ = 40 kΩ) |
| Total Harmonic Distortion | | −70 | | dB | 0 dBFS input, 0 dB gain |
| Power Supply Rejection Ratio | | 50 | | dB | |
| Mute Attenuation | | 80 | | dB | |
| Input Resistance | | 10 | | kΩ | |
| Input Capacitance | | 10 | | pF | |
| MICROPHONE BIAS | | | | | |
| Bias Voltage | | 0.75 × AVDD | | V | |
| Bias Current Source | | | 3 | mA | |
| Noise in the Signal Bandwidth | | 40 | | nV/√Hz | 20 Hz to 20 kHz |
| LINE OUTPUT[1] | | | | | |
| Full-Scale Output | | 1 × AVDD/3.3 | | V rms | |
| Signal-to-Noise Ratio (A-Weighted) | 85 | 100 | | dB | AVDD = 3.3 V |
| | | 94 | | | AVDD = 1.8 V |
| THD + N | | −80 | −70 | dB | AVDD = 3.3 V |
| | | −75 | | | AVDD = 1.8 V |
| Power Supply Rejection Ratio | | 50 | | dB | |
| Channel Separation | | 80 | | dB | |

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| HEADPHONE OUTPUT | | | | | |
| Full-Scale Output Voltage | | 1 × AVDD/3.3 | | V rms | |
| Maximum Output Power | | 30 | | mW | $R_L = 32\ \Omega$ |
| | | 60 | | mW | $R_L = 16\ \Omega$ |
| Signal-to-Noise Ratio (A-Weighted) | 85 | 96 | | dB | AVDD = 3.3 V |
| | | 90 | | dB | AVDD = 1.8 V |
| THD + N | | −65 | | dB | $P_{OUT}$ = 10 mW |
| | | −60 | | dB | $P_{OUT}$ = 20 mW |
| Power Supply Rejection Ratio | | 50 | | dB | |
| Mute Attenuation | | 80 | | dB | |
| LINE INPUT TO LINE OUTPUT | | | | | |
| Full-Scale Output Voltage | | 1 × AVDD/3.3 | | V rms | |
| Signal-to-Noise Ratio (A-Weighted) | | 92 | | dB | AVDD = 3.3 V |
| | | 86 | | dB | AVDD = 1.8 V |
| Total Harmonic Distortion | | −80 | | dB | AVDD = 3.3 V |
| | | −80 | | dB | AVDD = 1.8 V |
| Power Supply Rejection | | 50 | | dB | |
| MICROPHONE INPUT TO HEADPHONE OUTPUT | | | | | |
| Full-Scale Output Voltage | | 1 × AVDD/3.3 | | V rms | |
| Signal-to-Noise Ratio (A-Weighted) | | 94 | | dB | AVDD = 3.3 V |
| | | 88 | | dB | AVDD = 1.8 V |
| Power Supply Rejection Ratio | | 50 | | dB | |
| Programmable Attenuation | 6 | | 15 | dB | |
| Gain Step | | 3 | | dB | |
| Mute Attenuation | | 80 | | dB | |

[1] The line output is tested by sending a −1 dBFS input from the DAC to the line output.

## DIGITAL FILTER CHARACTERISTICS

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| ADC FILTER | | | | | |
| Pass Band | 0 | | 0.445 $f_S$ | Hz | ±0.04 dB |
| | | 0.5 $f_S$ | | Hz | −6 dB |
| Pass-Band Ripple | | | ±0.04 | dB | |
| Stop Band | 0.555 $f_S$ | | | Hz | |
| Stop-Band Attenuation | −61 | | | dB | f > 0.567 $f_S$ |
| High-Pass Filter Corner Frequency | | 3.7 | | Hz | −3 dB |
| | | 10.4 | | Hz | −0.5 dB |
| | | 21.6 | | Hz | −0.1 dB |
| DAC FILTER | | | | | |
| Pass Band | 0 | | 0.445 $f_S$ | Hz | ±0.04 dB |
| | | 0.5 $f_S$ | | Hz | −6 dB |
| Pass-Band Ripple | | | ±0.04 | dB | |
| Stop Band | 0.555 $f_S$ | | | Hz | |
| Stop-Band Attenuation | −61 | | | dB | f > 0.565 $f_S$ |
| CORE CLOCK TOLERANCE | | | | | |
| Frequency Range | 8.0 | | 13.8 | MHz | |
| Jitter Tolerance | | 50 | | ps | |

## TIMING CHARACTERISTICS

**Table 3. I[2]C® Timing**

| Parameter | Limit $t_{MIN}$ | Limit $t_{MAX}$ | Unit | Description |
|---|---|---|---|---|
| $t_{SCS}$ | 600 | | ns | Start condition setup time |
| $t_{SCH}$ | 600 | | ns | Start condition hold time |
| $t_{PH}$ | 600 | | ns | SCLK pulse width high |
| $t_{PL}$ | 1.3 | | μs | SCLK pulse width low |
| $f_{SCLK}$ | 0 | 526 | kHz | SCLK frequency |
| $t_{DS}$ | 100 | | ns | Data setup time |
| $t_{DH}$ | | 900 | ns | Data hold time |
| $t_{RT}$ | | 300 | ns | SDIN and SCLK rise time |
| $t_{FT}$ | | 300 | ns | SDIN and SCLK fall time |
| $t_{HCS}$ | 600 | | ns | Stop condition setup time |

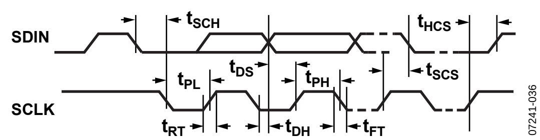



*Figure 2. I[2]C Timing*

**Table 4. Digital Audio Interface Slave Mode Timing**

| Parameter | Limit $t_{MIN}$ | Limit $t_{MAX}$ | Unit | Description |
|---|---|---|---|---|
| $t_{DS}$ | 10 | | ns | PBDAT setup time from BCLK rising edge |
| $t_{DH}$ | 10 | | ns | PBDAT hold time from BCLK rising edge |
| $t_{LRSU}$ | 10 | | ns | RECLRC/PBLRC setup time to BCLK rising edge |
| $t_{LRH}$ | 10 | | ns | RECLRC/PBLRC hold time to BCLK rising edge |
| $t_{DD}$ | | 30 | ns | RECDAT propagation delay from BCLK falling edge (external load of 70 pF) |
| $t_{BCH}$ | 25 | | ns | BCLK pulse width high |
| $t_{BCL}$ | 25 | | ns | BCLK pulse width low |
| $t_{BCY}$ | 50 | | ns | BCLK cycle time |

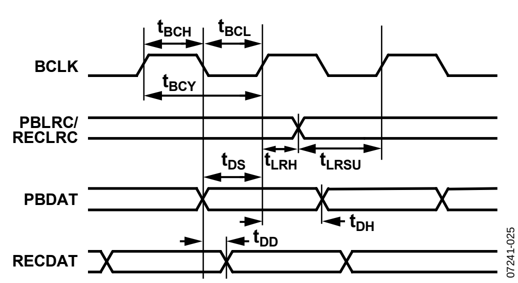



*Figure 3. Digital Audio Interface Slave Mode Timing*

**Table 5. Digital Audio Interface Master Mode Timing**

| Parameter | Limit | | Unit | Description |
|---|---|---|---|---|
| | $t_{MIN}$ | $t_{MAX}$ | | |
| $t_{DST}$ | 30 | | ns | PBDAT setup time to BCLK rising edge |
| $t_{DHT}$ | 10 | | ns | PBDAT hold time to BCLK rising edge |
| $t_{DL}$ | | 10 | ns | RECLRC/PBLRC propagation delay from BCLK falling edge |
| $t_{DDA}$ | | 10 | ns | RECDAT propagation delay from BCLK falling edge |
| $t_{BCLKR}$ | 10 | | ns | BCLK rising time (10 pF load) |
| $t_{BCLKF}$ | 10 | | ns | BCLK falling time (10 pF load) |
| $t_{BCLKDS}$ | 45:55:00 | 55:45:00 | | BCLK duty cycle (normal and USB mode) |

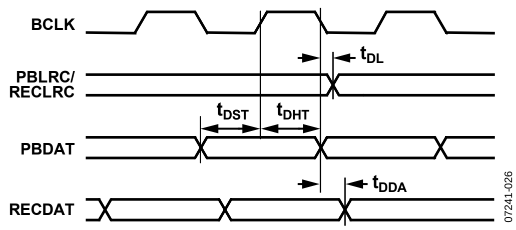



*Figure 4. Digital Audio Interface Master Mode Timing*

**Table 6. System Clock Timing**

| Parameter | Limit | | Unit | Description |
|---|---|---|---|---|
| | $t_{MIN}$ | $t_{MAX}$ | | |
| $t_{XTIY}$ | 72 | | ns | MCLK/XTI system clock cycle time |
| $t_{MCLKDS}$ | 40:60 | 60:40:00 | | MCLK/XTI duty cycle |
| $t_{XTIH}$ | 32 | | ns | MCLK/XTI system clock pulse width high |
| $t_{XTIL}$ | 32 | | ns | MCLK/XTI system clock pulse width low |
| $t_{COP}$ | 20 | | ns | CLKOUT propagation delay from MCLK/XTI falling edge |
| $t_{COPDIV2}$ | 20 | | ns | CLKODIV2 propagation delay from MCLK/XTI falling edge |

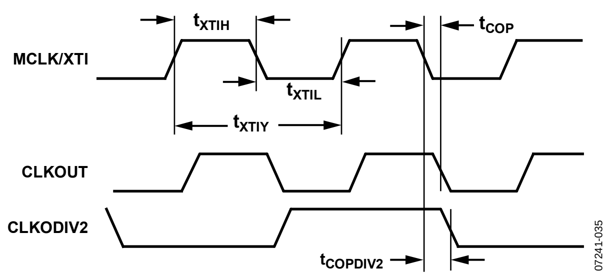



*Figure 5. System (MCLK) Clock Timing*

# ABSOLUTE MAXIMUM RATINGS

At 25°C, unless otherwise noted.

**Table 7.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 5 V |
| Input Voltage | $V_{DD}$ |
| Common-Mode Input Voltage | $V_{DD}$ |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Junction Temperature Range | −65°C to +165°C |
| Lead Temperature (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

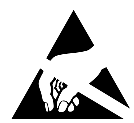
## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 8. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 28-Lead, 5 mm × 5 mm LFCSP | 28 | 32 | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

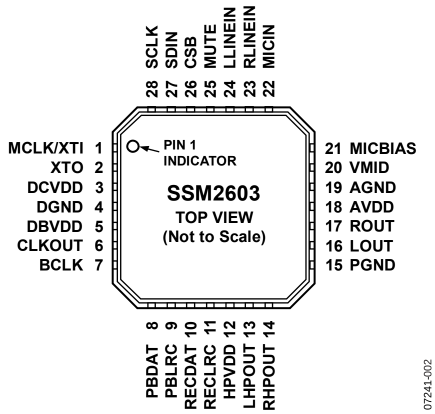



*Figure 6. Pin Configuration*

**Table 9. Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| 1 | MCLK/XTI | Digital Input | Master Clock Input/Crystal Input. |
| 2 | XTO | Digital Output | Crystal Output. |
| 3 | DCVDD | Digital Supply | Digital Core Supply. |
| 4 | DGND | Digital Ground | Digital Ground. |
| 5 | DBVDD | Digital Supply | Digital I/O Supply. |
| 6 | CLKOUT | Digital Output | Buffered Clock Output. |
| 7 | BCLK | Digital Input/Output | Digital Audio Bit Clock. |
| 8 | PBDAT | Digital Input | DAC Digital Audio Data Input, Playback Function. |
| 9 | PBLRC | Digital Input/Output | DAC Sampling Rate Clock, Playback Function (from Left and Right Channels). |
| 10 | RECDAT | Digital Output | ADC Digital Audio Data Output, Record Function. |
| 11 | RECLRC | Digital Input/Output | ADC Sampling Rate Clock, Record Function (from Left and Right Channels). |
| 12 | HPVDD | Analog Supply | Headphone Supply. |
| 13 | LHPOUT | Analog Output | Headphone Output for Left Channel. |
| 14 | RHPOUT | Analog Output | Headphone Output for Right Channel. |
| 15 | PGND | Analog Ground | Headphone Ground. |
| 16 | LOUT | Analog Output | Line Output for Left Channel. |
| 17 | ROUT | Analog Output | Line Output for Right Channel. |
| 18 | AVDD | Analog Supply | Analog Supply. |
| 19 | AGND | Analog Ground | Analog Ground. |
| 20 | VMID | Analog Output | Midrail Voltage Decoupling Input. |
| 21 | MICBIAS | Analog Output | Microphone Bias. |
| 22 | MICIN | Analog Input | Microphone Input Signal. |
| 23 | RLINEIN | Analog Input | Line Input for Right Channel. |
| 24 | LLINEIN | Analog Input | Line Input for Left Channel. |
| 25 | MUTE | Digital Input | DAC Output Mute, Active Low |
| 26 | CSB | Digital Input | 2-Wire Control Interface I²C Address Selection. |
| 27 | SDIN | Digital Input/Output | 2-Wire Control Interface Data Input/Output. |
| 28 | SCLK | Digital Input | 2-Wire Control Interface Clock Input. |
| | GND Pad | Thermal Pad | Center Thermal Pad. Connect to PCB ground layer. |

# TYPICAL PERFORMANCE CHARACTERISTICS

## CONVERTER FILTER RESPONSE

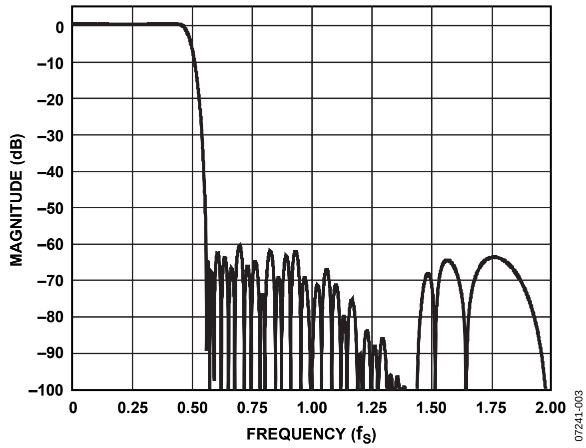



*Figure 7. ADC Digital Filter Frequency Response*

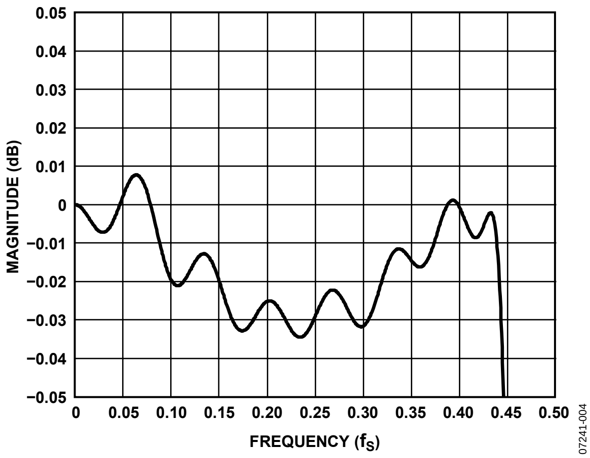



*Figure 8. ADC Digital Filter Ripple*

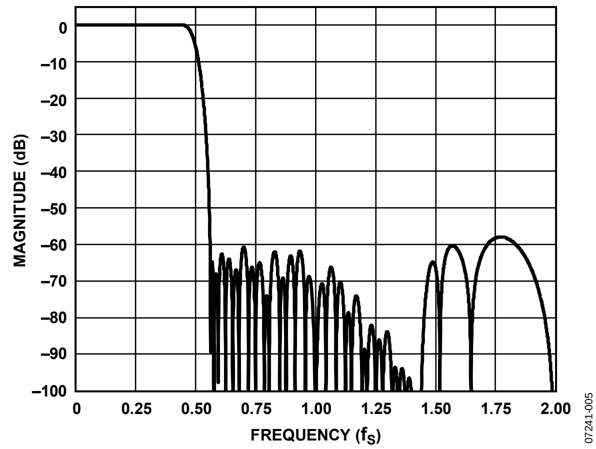



*Figure 9. DAC Digital Filter Frequency Response*

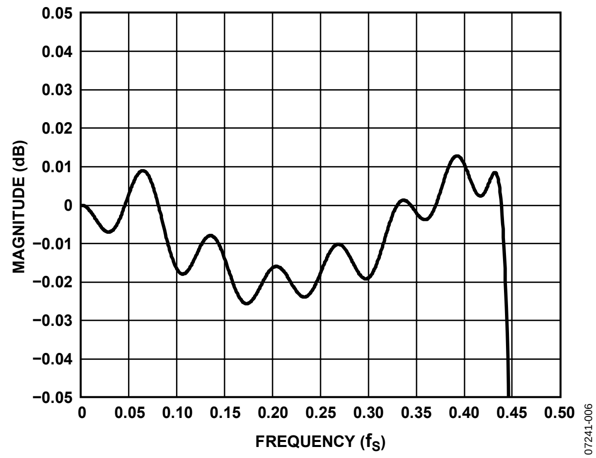



*Figure 10. DAC Digital Filter Ripple*

## DIGITAL DE-EMPHASIS

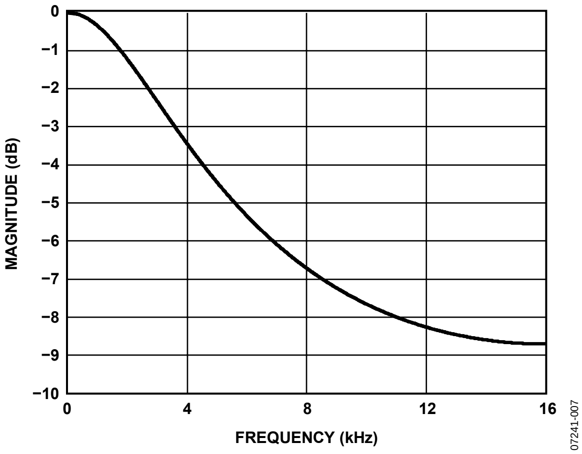



*Figure 11. De-Emphasis Frequency Response, Audio Sampling Rate = 32 kHz*

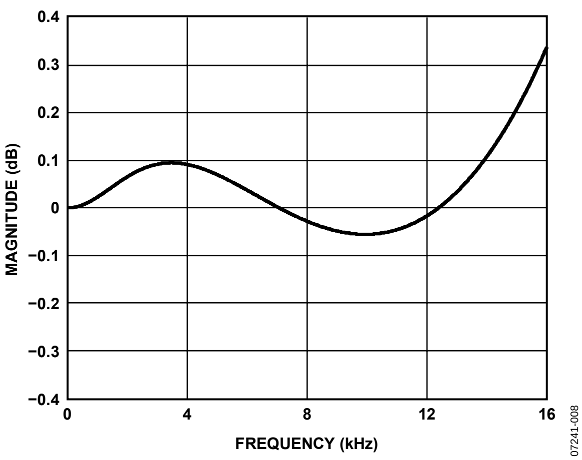



*Figure 12. De-Emphasis Error, Audio Sampling Rate = 32 kHz*

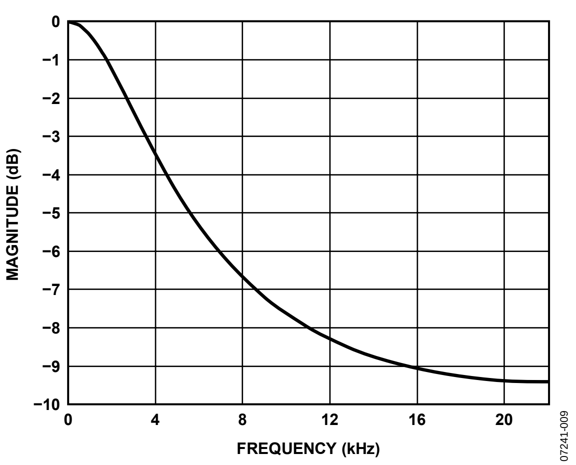



*Figure 13. De-Emphasis Frequency Response, Audio Sampling Rate = 44.1 kHz*

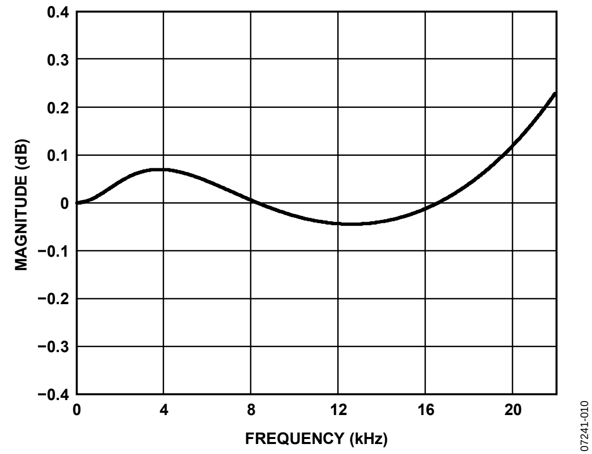



*Figure 14. De-Emphasis Error, Audio Sampling Rate = 44.1 kHz*

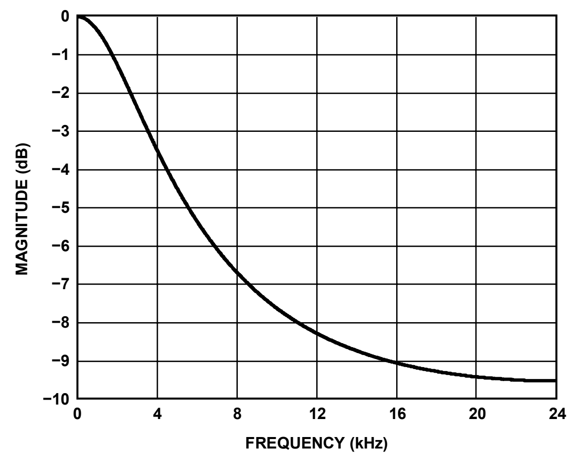



*Figure 15. De-Emphasis Frequency Response, Audio Sampling Rate = 48 kHz*

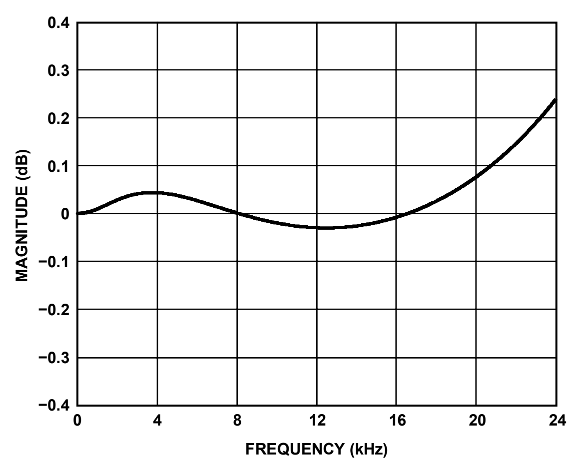



*Figure 16. De-Emphasis Error, Audio Sampling Rate = 48 kHz*

# THEORY OF OPERATION

## DIGITAL CORE

Inside the SSM2603 digital core is one central clock source, called the master clock (MCLK), that produces a reference clock for all internal audio data processing and synchronization. When using an external clock source to drive the MCLK pin, great care should be taken to select a clock source with less than 50 ps of jitter. Without careful generation of the MCLK signal, the digital audio quality will most likely suffer.

To enable the SSM2603 to generate the central reference clock in a system, connect a crystal oscillator between the MCLK/XTI input pin and the XTO output pin.

To allow an external device to generate the central reference clock, apply the external clock signal directly through the MCLK/XTI input pin. In this configuration, the oscillator circuit of the SSM2603 can be powered down by using the OSC bit (Register R6, Bit D5) to reduce power consumption.

To accommodate applications with very high frequency master clocks, the internal core reference clock of the SSM2603 can be set to either MCLK or MCLK divided by 2. This is enabled by adjusting the setting of the CLKDIV2 bit (Register R8, Bit D6). Complementary to this feature, the CLKOUT pin can also drive external clock sources with either the core clock signal or core clock divided by 2 by enabling the CLKODIV2 bit (Register R8, Bit D7).

## ADC AND DAC

The SSM2603 contains a pair of oversampling Σ-Δ ADCs. The maximum ADC full-scale input level is 1.0 V rms when AVDD = 3.3 V. If the input signal to the ADC exceeds this level, data overloading occurs and causes audible distortion.

The ADC can accept analog audio input from either the stereo line inputs or the monaural microphone input. Note that the ADC can only accept input from a single source, so the user must choose either the line inputs or the microphone input as the source using the INSEL bit (Register R4, Bit D2). The digital data from the ADC output, once converted, is processed using the ADC filters.

Complementary to the ADC channels, the SSM2603 contains a pair of oversampling Σ-Δ DACs that convert the digital audio data from the internal DAC filters into an analog audio signal. The DAC output can also be muted by setting the DACMU bit (Register R5, Bit D3) in the control register.

## ADC HIGH-PASS AND DAC DE-EMPHASIS FILTERS

The ADC and DAC employ separate digital filters that perform 24-bit signal processing. The digital filters are used for both record and playback modes and are optimized for each individual sampling rate used.

For recording mode operations, the unprocessed data from the ADC enters the ADC filters and is converted to the appropriate sampling frequency, and then is output to the digital audio interface.

For playback mode operations, the DAC filters convert the digital audio interface data to oversampled data, using a sampling rate selected by the user. The oversampled data is processed by the DAC and then is sent to the analog output mixer by enabling the DACSEL (Register R4, Bit D4).

Users have the option of setting up the device so that any dc offset in the input source signal is automatically detected and removed. To accomplish this, enable the digital high-pass filter (see Table 2 for characteristics) contained in the ADC digital filters by using the ADCHPF bit (Register R5, Bit D0).

In addition, users can implement digital de-emphasis by using the DEEMPH bits (Register R5, Bit D1 and Bit D2).

## HARDWARE MUTE PIN

The MUTE pin is a hardware mute pin that puts the DAC output of the SSM2603 codec into a silent state. When MUTE is activated and the codec enters a mute state, the playback output voltage settles to VMID. The enabling of MUTE is shown in Figure 17.

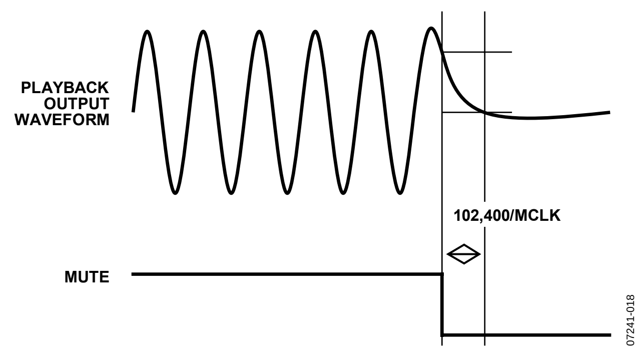



*Figure 17. Enabling of MUTE*

## AUTOMATIC LEVEL CONTROL (ALC)

The SSM2603 codec has an automatic level control (ALC) that can be activated to suppress clipping and improve dynamic range even if a sudden, loud input signal is introduced. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant.

### *Decay (Gain Ramp-Up) Time*

Decay time is the time taken for the PGA gain to ramp up to 90% of its range. The time for the recording level to return to its target value, therefore, depends on both the decay time and the gain adjustment required. If the gain adjustment is small, the time to return to the target value will be less than the decay time.

### *Attack (Gain Ramp-Down) Time*

Attack time is the time taken for the PGA gain to ramp down through 90% of its range. The time for the recording level to return to its target value, therefore, depends on both the attack time and the gain adjustment required. If the gain adjustment is small, the time to return to the target value will be less than the attack time.

### *Noise Gate*

When the ALC function is enabled but the input signal is silent for long periods, an audible hissing sound may be introduced by a phenomenon called noise pumping. To prevent this occurrence, the SSM2603 employs a noise gate function. A user-selected threshold can be set by using the NGTH bits (Register R18, Bit D3 to Bit D7). When the noise gate is enabled, the ADC output is either muted or held at a constant gain to prevent the noise-pumping phenomenon. For more information about the noise gate settings, see Table 41.

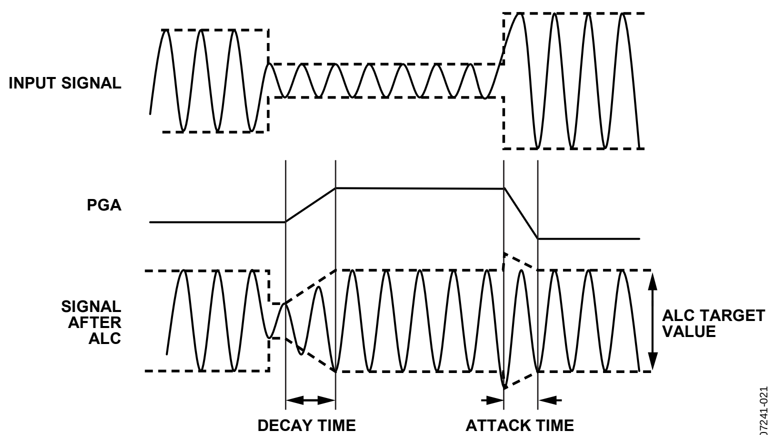



*Figure 18. PGA and ALC Decay Time and Attack Time Definitions*

## ANALOG INTERFACE

### Signal Chain

The SSM2603 includes stereo single-ended line and monaural microphone inputs to the on-board ADC. Either the line inputs or the microphone input, but not both simultaneously, can be connected to the ADC by setting the INSEL bit (Register R4, Bit D2). In addition, the line or microphone inputs can be routed and mixed directly to the output terminals via the SIDETONE_EN (Register R4, Bit D5) and BYPASS (Register R4, Bit D3) bits. The SSM2603 also includes line and headphone outputs from the on-board DAC.

### Stereo Line and Monaural Microphone Inputs

The SSM2603 contains a set of single-ended stereo line inputs (RLINEIN and LLINEIN) that are internally biased to VMID by a voltage divider placed between AVDD and AGND. The line input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the bypass path by using the BYPASS bit (Register R4, Bit D3).

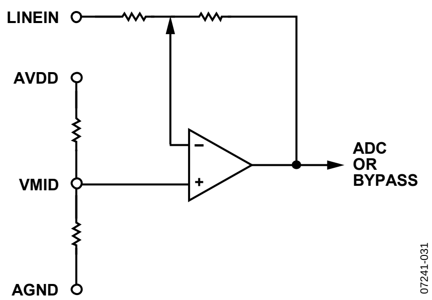



Figure 19. Line Input to ADC

The line input volume can be adjusted from −34.5 dB to +33 dB in steps of +1.5 dB by setting the LINVOL (Register R0, Bit D0 to Bit D5) and RINVOL (Register R1, Bit D0 to Bit D5) bits. Volume control, by default, is independently adjustable on both right and left line inputs. However, the LRINBOTH or RLINBOTH bit, if selected, simultaneously loads both sets of volume control with the same value. The user can also set the LINMUTE (Register R0, Bit D7) and RINMUTE (Register R1, Bit D7) bits to mute the line input signal to the ADC.

The high impedance, low capacitance monaural microphone input pin (MICIN) has two gain stages and a microphone bias level (MICBIAS) that is internally biased to the VMID voltage level by a voltage divider placed between AVDD and AGND. The microphone input signal can be connected to the internal ADC and, if desired, routed directly to the outputs via the sidetone path by using the SIDETONE_EN bit (Register R4, Bit D5).

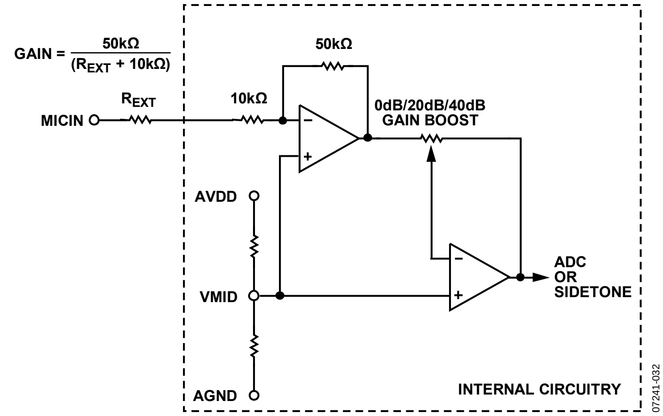



Figure 20. Microphone Input to ADC

The first gain stage is composed of a low noise operational amplifier set to an inverting configuration with integrated 50 kΩ feedback and 10 kΩ input resistors. The default microphone input signal gain is 14 dB. An external resistor ($R_{EXT}$) can be connected in series with the MICIN pin to reduce the first-stage gain of the microphone input signal to as low as 0 dB by using the following equation:

$$\textit{Microphone Input Gain} = 50\ \text{k}\Omega/(10\ \text{k}\Omega + R_{EXT})$$

The second-stage gain of the microphone signal path is derived from the internal microphone boost circuitry. The available settings are 0 dB, 20 dB, and 40 dB and are controlled by the MICBOOST (Register R4, Bit D0) and MICBOOST2 (Register R4, Bit D8) bits. To achieve 20 dB of secondary gain boost, the user can select either MICBOOST or MICBOOST2. To achieve 40 dB of secondary microphone signal gain, the user must select both MICBOOST and MICBOOST2.

In similar functionality to the line inputs, the MUTEMIC bit (Register R4, Bit D1) can be set to mute the microphone input signal to the ADC.

Note that when sourcing audio data from both line and microphone inputs, the maximum full-scale input of the ADC is 1.0 V rms when AVDD = 3.3 V. Do not source any input voltage larger than full scale to avoid overloading the ADC, which causes distortion of sound and deterioration of audio quality. For best sound quality in both microphone and line inputs, gain should be carefully configured so that the ADC receives a signal equal to its full scale. This maximizes the signal-to-noise ratio for best total audio quality.

### Bypass and Sidetone Paths to Output

The line and microphone inputs can be routed and mixed directly to the output terminals via the SIDETONE_EN (Register R4, Bit D5) and BYPASS (Register R4, Bit D3) software control register selections. In both of these modes, the analog input signal is routed directly to the output terminals and is not digitally converted. The bypass signal at the output mixer is the same level as the output of the PGA associated with each line input.

The sidetone signal at the output mixer must be attenuated by a range of −6 dB to −15 dB in steps of −3 dB by configuring the SIDETONE_ATT (Register R4, Bit D6 and Bit D7) control register bits. The selected level of attenuation occurs after the initial microphone signal amplification from the microphone first- and second-stage gains.

### Line and Headphone Outputs

The DAC outputs, the microphone (the sidetone path), and the line inputs (the bypass path) are summed at an output mixer. This output signal can be present at both the stereo line outputs and stereo headphone outputs.

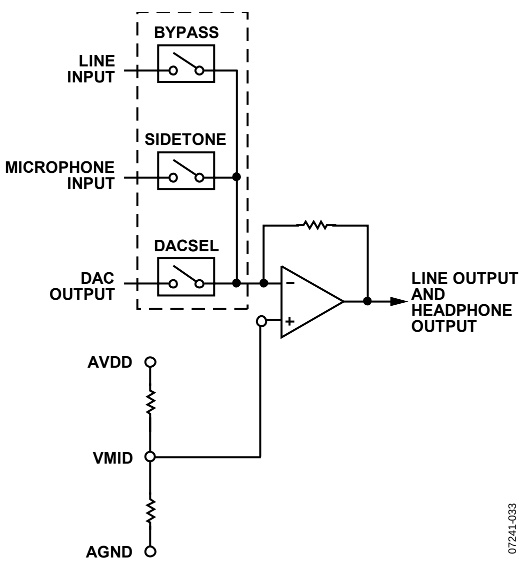



*Figure 21. Output Signal Chain*

The SSM2603 has a set of efficient headphone amplifier outputs, LHPOUT and RHPOUT, that are able to drive 16 Ω or 32 Ω headphone speakers.

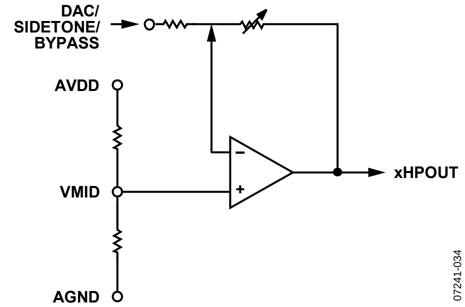



*Figure 22. Headphone Output*

In similar functionality to the line inputs, the LHPOUT and RHPOUT volumes, by default, are independently adjusted by setting the LHPVOL (Register R2, Bit D0 to Bit D6) and RHPVOL (Register R3, Bit D0 to Bit D6) bits of the headphone output control registers. The headphone outputs can be muted by writing codes less than 0110000 to the LHPVOL and RHPVOL bits. The user is also able to simultaneously load the volume control of both channels by writing to the LRHPBOTH (Register R2, Bit D8) and RLHPBOTH (Register R3, Bit D8) bits of the left- and right-channel DAC volume registers.

The maximum output level of the headphone outputs is 1.0 V rms when AVDD and HPVDD = 3.3 V. To suppress audible pops and clicks, the headphone and line outputs are held at the VMID dc voltage level when the device is set to standby mode or in the event that the headphone outputs are muted.

The stereo line outputs of the SSM2603, the LOUT and ROUT pins, are able to drive a load impedance of 10 kΩ and 50 pF. The line output signal levels are not adjustable at the output mixer, having a fixed gain of 0 dB. The maximum output level of the line outputs is 1.0 V rms when AVDD = 3.3 V.

## DIGITAL AUDIO INTERFACE

The digital audio input can support the following four digital audio communication protocols: right-justified mode, left-justified mode, I²S mode, and digital signal processor (DSP) mode.

The mode selection is performed by writing to the FORMAT bits of the digital audio interface register (Register R7, Bit D1 and Bit D0). All modes are MSB first and operate with data of 16 to 32 bits.

### *Recording Mode*

On the RECDAT output pin, the digital audio interface can send digital audio data for recording mode operation. The digital audio interface outputs the processed internal ADC digital filter data onto the RECDAT output. The digital audio data stream on RECDAT comprises left- and right-channel audio data that is time domain multiplexed.

The RECLRC is the digital audio frame clock signal that separates left- and right-channel data on the RECDAT lines.

The BCLK signal acts as the digital audio clock. Depending on if the SSM2603 is in master or slave mode, the BCLK signal is either an input or an output signal. During a recording operation, RECDAT and RECLRC must be synchronous to the BCLK signal to avoid data corruption.

### *Playback Mode*

On the PBDAT input pin, the digital audio interface can receive digital audio data for playback mode operation. The digital audio data stream on PBDAT comprises left- and right-channel audio data that is time domain multiplexed. The PBLRC is the digital audio frame clock signal that separates left- and right-channel data on the PBDAT lines.

The BCLK signal acts as the digital audio clock. Depending on whether the SSM2603 is in master or slave mode, the BCLK signal is either an input or an output signal. During a playback operation, PBDAT and PBLRC must be synchronous to the BCLK signal to avoid data corruption.

### *Digital Audio Data Sampling Rate*

To accommodate a wide variety of commonly used DAC and ADC sampling rates, the SSM2603 allows for two modes of operation, normal and USB, selected by the USB bit (Register R8, Bit D0).

In normal mode, the SSM2603 supports digital audio sampling rates from 8 kHz to 96 kHz. Normal mode supports 256 $f_S$ and 384 $f_S$ based clocks. To select the desired sampling rate, the user must set the appropriate sampling rate register in the SR control bits (Register R8, Bit D2 to Bit D5) and match this selection to the core clock frequency that is pulsed on the MCLK pin. See Table 29 and Table 30 for guidelines.

In USB mode, the SSM2603 supports digital audio sampling rates from 8 kHz to 96 kHz. USB mode is enabled on the SSM2603 to support the common universal serial bus (USB) clock rate of 12 MHz, or to support 24 MHz if the CLKDIV2 control register bit is activated. The user must set the appropriate sampling rate in the SR control bits (Register R8, Bit D2 to Bit D5). See Table 29 and Table 30 for guidelines.

Note that the sampling rate is generated as a fixed divider from the MCLK signal. Because all audio processing references the core MCLK signal, corruption of this signal, in turn, corrupts the outgoing audio quality of the SSM2603. The BCLK/RECLRC/RECDAT or BCLK/PBLRC/PBDAT signals must be synchronized with MCLK in the digital audio interface circuit. MCLK must be faster or equal to the BCLK frequency to guarantee that no data is lost during data synchronization.

The BCLK frequency should be greater than

$$\textit{Sampling Rate} \times \textit{Word Length} \times 2$$

Ensuring that the BCLK frequency is greater than this value guarantees that all valid data bits are captured by the digital audio interface circuitry. For example, if a 32 kHz digital audio sampling rate with a 32-bit word length is desired, BCLK ≥ 2.048 MHz.

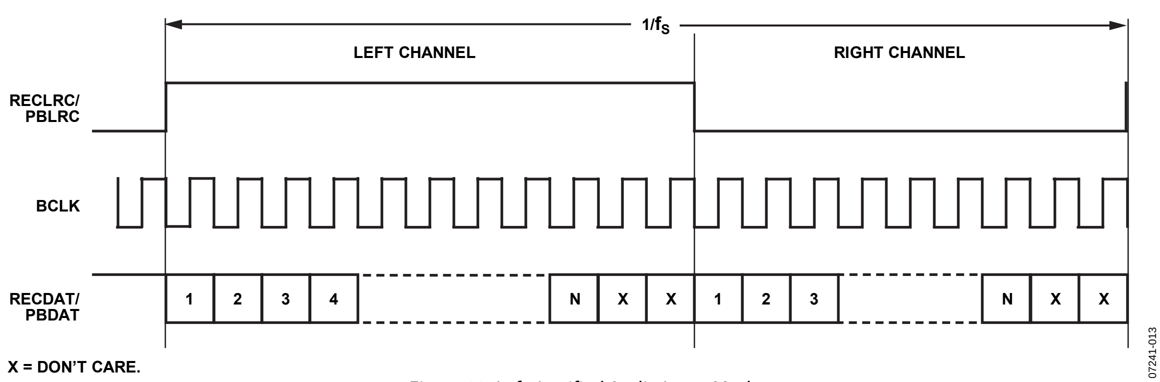



*Figure 23. Left-Justified Audio Input Mode*

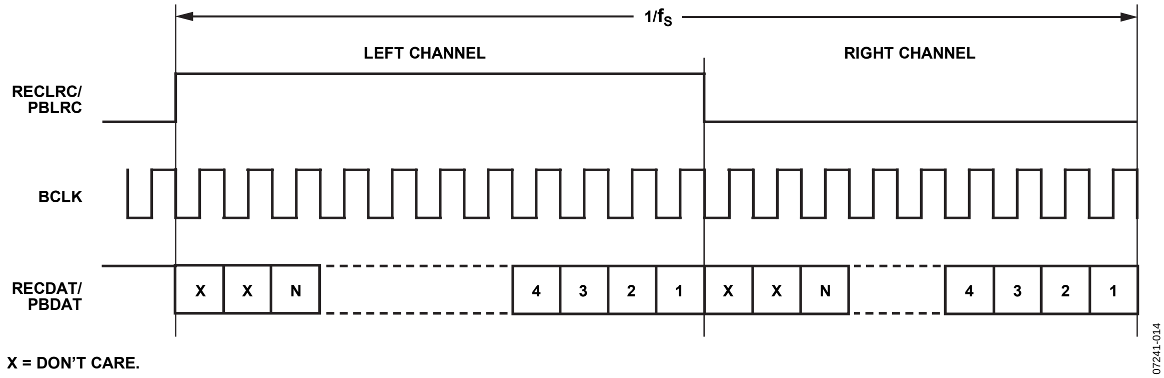



*Figure 24. Right-Justified Audio Input Mode*

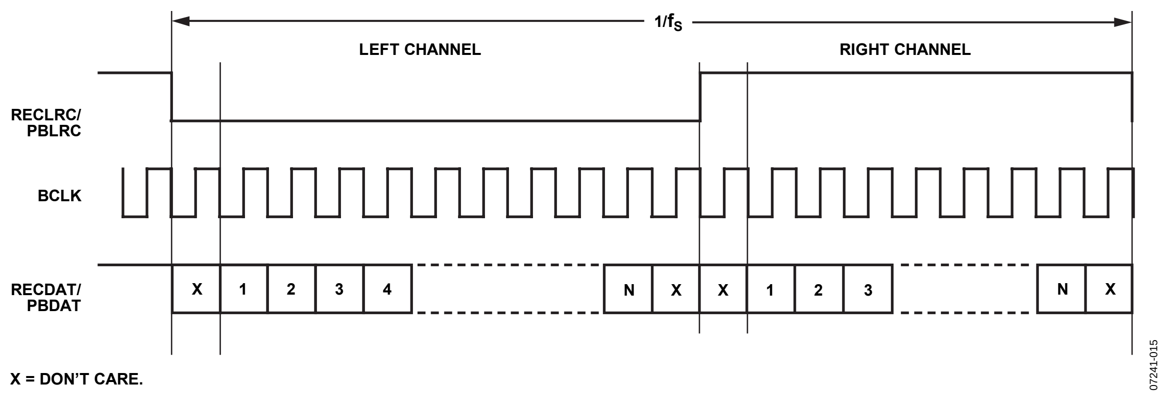



*Figure 25. I²S Audio Input Mode*

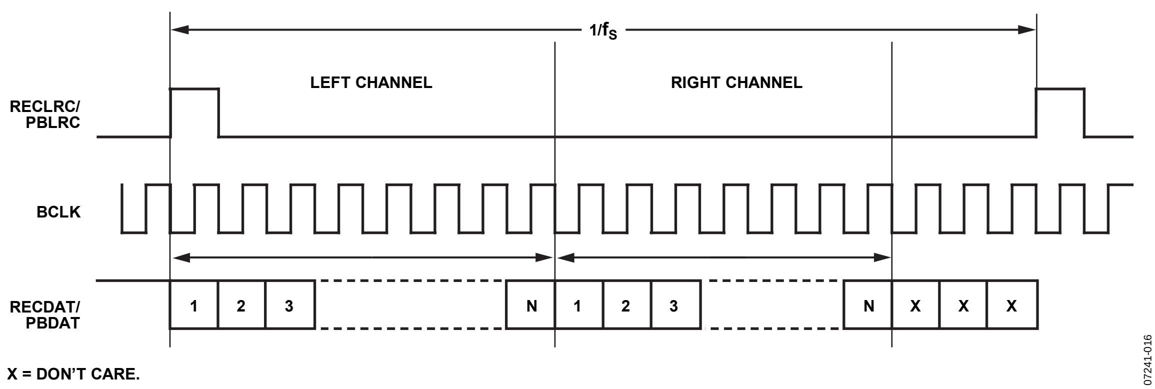



*Figure 26. DSP/Pulse Code Modulation (PCM) Mode Audio Input Submode 1 (SM1) [Bit LRP = 0]*

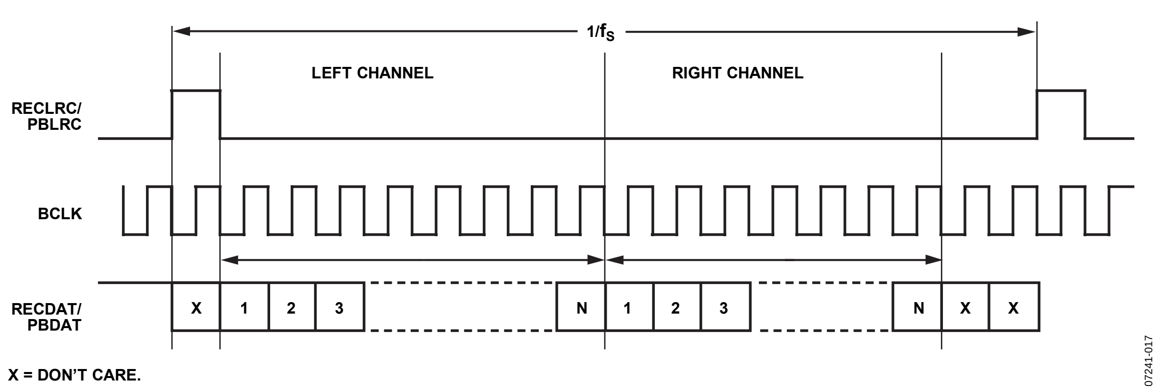



*Figure 27. DSP/PCM Mode Audio Input Submode 2 (SM2) [Bit LRP = 1]*

## SOFTWARE CONTROL INTERFACE

The software control interface provides access to the user-selectable control registers and can operate with a 2-wire ($I^2C$) interface.

Within each control register is a control data-word consisting of 16 bits, MSB first. Bit B15 to Bit B9 are the register map address, and Bit B8 to Bit B0 are register data for the associated register map.

SDIN generates the serial control data-word, SCLK clocks the serial data, and CSB determines the $I^2C$ device address. If the CSB pin is set to 0, the address selected is 0011010; if 1, the address is 0011011.

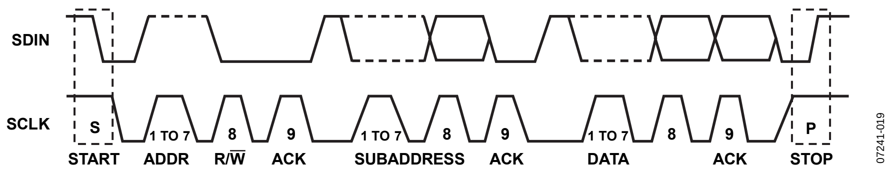



*Figure 28. 2-Wire $I^2C$ Generalized Clocking Diagram*

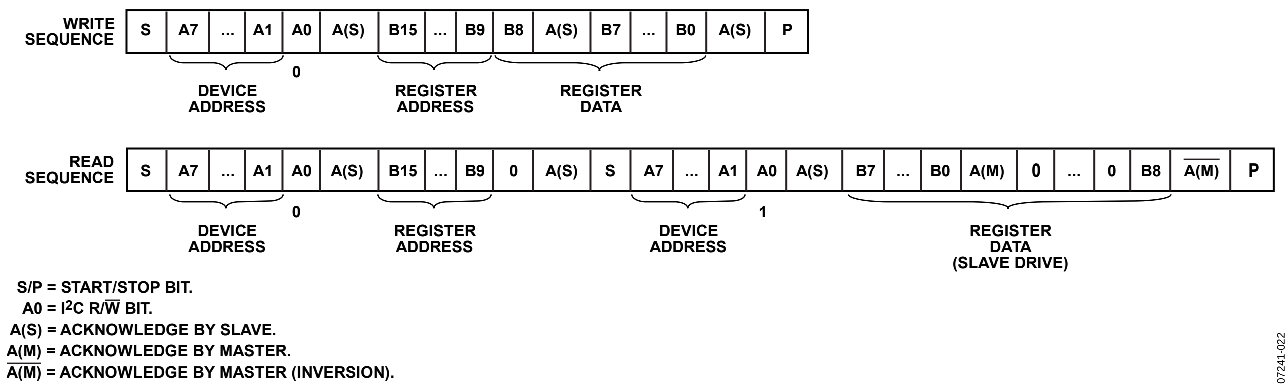



*Figure 29. $I^2C$ Write and Read Sequences*

# TYPICAL APPLICATION CIRCUITS

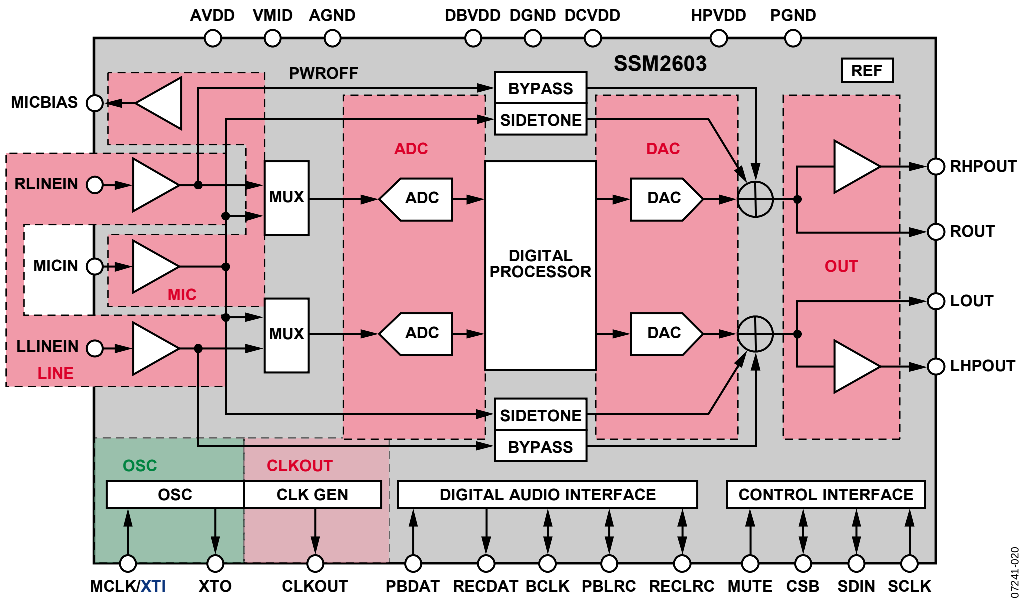



*Figure 30. Power Management Functional Location Diagram (Control Register R6, Bit D0 to Bit D7)*

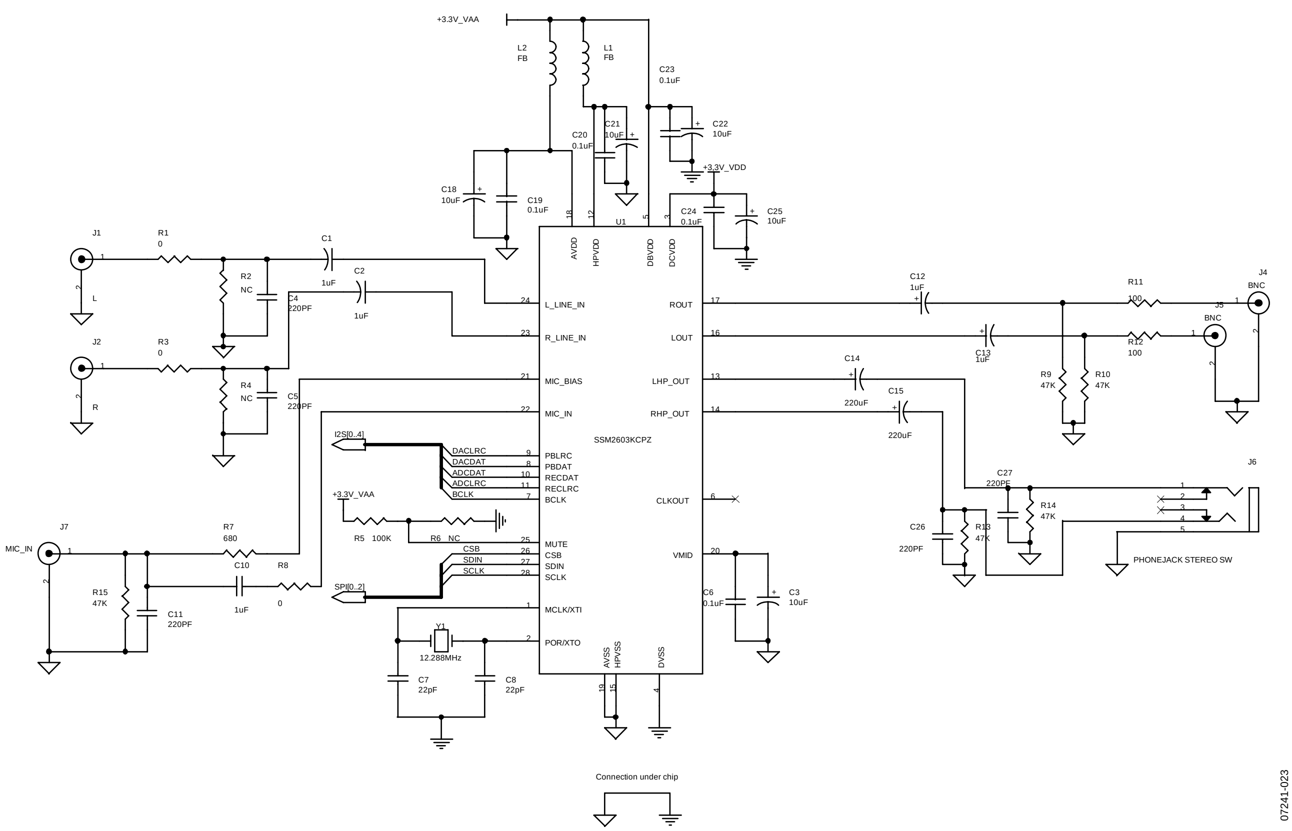



*Figure 31. Typical Application Circuit*

# REGISTER MAP

**Table 10. Register Map**

| Reg. | Address | Name | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R0 | 0x00 | Left-Channel ADC Input Volume | LRINBOTH | LINMUTE | 0 | LINVOL [5:0] | | | | | | 010010111 |
| R1 | 0x01 | Right-Channel ADC Input Volume | RLINBOTH | RINMUTE | 0 | RINVOL [5:0] | | | | | | 010010111 |
| R2 | 0x02 | Left-Channel DAC Volume | LRHPBOTH | LZCEN | LHPVOL [6:0] | | | | | | | 001111001 |
| R3 | 0x03 | Right-Channel DAC Volume | RLHPBOTH | RZCEN | RHPVOL [6:0] | | | | | | | 001111001 |
| R4 | 0x04 | Analog Audio Path | MICBOOST2 | SIDETONE_ATT [1:0] | | SIDETONE_EN | DACSEL | BYPASS | INSEL | MUTEMIC | MICBOOST | 000001010 |
| R5 | 0x05 | Digital Audio Path | 0 | 0 | 0 | 0 | HPOR | DACMU | DEEMPH [1:0] | | ADCHPF | 000001000 |
| R6 | 0x06 | Power Management | 0 | PWROFF | CLKOUT | OSC | OUT | DAC | ADC | MIC | LINEIN | 010011111 |
| R7 | 0x07 | Digital Audio I/F | 0 | BCLKINV | MS | LRSWAP | LRP | WL [1:0] | | FORMAT [1:0] | | 000001010 |
| R8 | 0x08 | Sampling Rate | 0 | CLKODIV2 | CLKDIV2 | SR [3:0] | | | | BOSR | USB | 000000000 |
| R9 | 0x09 | Active | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ACTIVE | 000000000 |
| R15 | 0x0F | Software Reset | RESET [8:0] | | | | | | | | | 000000000 |
| R16 | 0x10 | ALC Control 1 | ALCSEL [1:0] | | MAXGAIN [2:0] | | | ALCL [3:0] | | | | 001111011 |
| R17 | 0x11 | ALC Control 2 | 0 | DCY [3:0] | | | | ATK [3:0] | | | | 000110010 |
| R18 | 0x12 | Noise Gate | 0 | NGTH [4:0] | | | | | NGG [1:0] | | NGAT | 000000000 |

# REGISTER MAP DETAILS

## LEFT-CHANNEL ADC INPUT VOLUME, ADDRESS 0x00

Table 11. Left-Channel ADC Input Volume Register Bit Map

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| LRINBOTH | LINMUTE | 0 | LINVOL [5:0] | | | | | |

Table 12. Descriptions of Left-Channel ADC Input Volume Register Bits

| Bit Name | Description | Settings |
|---|---|---|
| LRINBOTH | Left-to-right line input ADC data load control | 0 = disable simultaneous loading of left-channel ADC data to right-channel register (default)<br>1 = enable simultaneous loading of left-channel ADC data to right-channel register |
| LINMUTE | Left-channel input mute | 0 = disable mute<br>1 = enable mute on data path to ADC (default) |
| LINVOL [5:0] | Left-channel PGA volume control | 00 0000 = −34.5 dB<br>… In 1.5 dB steps<br>01 0111 = 0 dB (default)<br>… In 1.5 dB steps<br>01 1111 = 12 dB<br>10 0000 = 13.5 dB<br>10 0001 = 15 dB<br>10 0010 = 16.5 dB<br>10 0011 = 18 dB<br>10 0100 = 19.5 dB<br>10 0101 = 21 dB<br>10 0110 = 22.5 dB<br>10 0111 = 24 dB<br>10 1000 = 25.5 dB<br>10 1001 = 27 dB<br>10 1010 = 28.5 dB<br>10 1011 = 30 dB<br>10 1100 = 31.5 dB<br>10 1101 = 33 dB<br>11 1111 to 10 1101 = 33 dB |

## RIGHT-CHANNEL ADC INPUT VOLUME, ADDRESS 0x01

**Table 13. Right-Channel ADC Input Volume Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| RLINBOTH | RINMUTE | 0 | RINVOL [5:0] | | | | | |

**Table 14. Descriptions of Right-Channel ADC Input Volume Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| RLINBOTH | Right-to-left line input ADC data load control | 0 = disable simultaneous loading of right-channel ADC data to left-channel register (default)<br>1 = enable simultaneous loading of right-channel ADC data to left-channel register |
| RINMUTE | Right-channel input mute | 0 = disable mute<br>1 = enable mute on data path to ADC (default) |
| RINVOL [5:0] | Right-channel PGA volume control | 00 0000 = −34.5 dB<br>… In 1.5 dB steps<br>01 0111 = 0 dB (default)<br>… In 1.5 dB steps<br>01 1111 = 12 dB<br>10 0000 = 13.5 dB<br>10 0001 = 15 dB<br>10 0010 = 16.5 dB<br>10 0011 = 18 dB<br>10 0100 = 19.5 dB<br>10 0101 = 21 dB<br>10 0110 = 22.5 dB<br>10 0111 = 24 dB<br>10 1000 = 25.5 dB<br>10 1001 = 27 dB<br>10 1010 = 28.5 dB<br>10 1011 = 30 dB<br>10 1100 = 31.5 dB<br>10 1101 = 33 dB<br>11 1111 to 10 1101 = 33 dB |

## LEFT-CHANNEL DAC VOLUME, ADDRESS 0x02

**Table 15. Left-Channel DAC Volume Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| LRHPBOTH | LZCEN | LHPVOL [6:0] | | | | | | |

**Table 16. Descriptions of Left-Channel DAC Volume Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| LRHPBOTH | Left-to-right headphone volume load control | 0 = disable simultaneous loading of left-channel headphone volume data to right-channel register (default)<br>1 = enable simultaneous loading of left-channel headphone volume data to right-channel register |
| LZCEN | Left-channel zero cross detect enable | 0 = disable (default)<br>1 = enable |
| LHPVOL [6:0] | Left-channel headphone volume control | 000 0000 to 010 1111 = mute<br>011 0000 = −73 dB<br>… In 1 dB steps<br>111 1001 = 0 dB (default)<br>… In 1 dB steps<br>111 1111 = +6 dB |

## RIGHT-CHANNEL DAC VOLUME, ADDRESS 0x03

**Table 17. Right-Channel DAC Volume Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| RLHPBOTH | RZCEN | RHPVOL [6:0] | | | | | | |

**Table 18. Descriptions of Right-Channel DAC Volume Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| RLHPBOTH | Right-to-left headphone volume load control | 0 = disable simultaneous loading of right-channel headphone volume data to left-channel register (default)<br>1 = enable simultaneous loading of right-channel headphone volume data to left-channel register |
| RZCEN | Right-channel zero cross detect enable | 0 = disable (default)<br>1 = enable |
| RHPVOL [6:0] | Right-channel headphone volume control | 000 0000 to 010 1111 = mute<br>011 0000 = −73 dB<br>… In 1 dB steps<br>111 1001 = 0 dB (default)<br>… In 1 dB steps<br>111 1111 = +6 dB |

## ANALOG AUDIO PATH, ADDRESS 0x04

**Table 19. Analog Audio Path Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| MICBOOST2 | SIDETONE_ATT [1:0] | | SIDETONE_EN | DACSEL | BYPASS | INSEL | MUTEMIC | MICBOOST |

**Table 20. Descriptions of Analog Audio Path Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| MICBOOST2 | Additional microphone amplifier gain booster control. | 0 = 0 dB (default)<br>1 = 20 dB |
| SIDETONE_ATT [1:0] | Microphone sidetone gain control. | 00 = −6 dB (default)<br>01 = −9 dB<br>10 = −12 dB<br>11 = −15 dB |
| SIDETONE_EN | Sidetone enable. Allows attenuated microphone signal to be mixed at device output terminal. | 0 = sidetone disable (default)<br>1 = sidetone enable |
| DACSEL | DAC select. Allows DAC output to be mixed at device output terminal. | 0 = do not select DAC (default)<br>1 = select DAC |
| BYPASS | Bypass select. Allows line input signal to be mixed at device output terminal. | 0 = bypass disable<br>1 = bypass enable (default) |
| INSEL | Line input or microphone input select to ADC. | 0 = line input select to ADC (default)<br>1 = microphone input select to ADC |
| MUTEMIC | Microphone mute control to ADC. | 0 = mute on data path to ADC disable<br>1 = mute on data path to ADC enable (default) |
| MICBOOST | Primary microphone amplifier gain booster control. | 0 = 0 dB (default)<br>1 = 20 dB |

## DIGITAL AUDIO PATH, ADDRESS 0x05

**Table 21. Digital Audio Path Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HPOR | DACMU | DEEMPH [1:0] | | ADCHPF |

**Table 22. Descriptions of Digital Audio Path Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| HPOR | Stores dc offset when high-pass filter is disabled | 0 = clear offset (default)<br>1 = store offset |
| DACMU | DAC digital mute | 0 = no mute (signal active)<br>1 = mute (default) |
| DEEMPH [1:0] | De-emphasis control | 00 = no de-emphasis (default)<br>01 = 32 kHz sampling rate<br>10 = 44.1 kHz sampling rate<br>11 = 48 kHz sampling rate |
| ADCHPF | ADC high-pass filter control | 0 = ADC high-pass filter enable (default)<br>1 = ADC high-pass filter disable |

## POWER MANAGEMENT, ADDRESS 0x06

**Table 23. Power Management Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | PWROFF | CLKOUT | OSC | OUT | DAC | ADC | MIC | LINEIN |

**Table 24. Description of Power Management Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| PWROFF | Whole chip power-down control | 0 = power up<br>1 = power down (default) |
| CLKOUT | Clock output power-down control | 0 = power up (default)<br>1 = power down |
| OSC | Crystal power-down control | 0 = power up (default)<br>1 = power down |
| OUT | Output power-down control | 0 = power up<br>1 = power down (default) |
| DAC | DAC power-down control | 0 = power up<br>1 = power down (default) |
| ADC | ADC power-down control | 0 = power up<br>1 = power down (default) |
| MIC | Microphone input power-down control | 0 = power up<br>1 = power down (default) |
| LINEIN | Line input power-down control | 0 = power up<br>1 = power down (default) |

### *Power Consumption*

**Table 25.**

| Mode | PWROFF | CLKOUT | OSC | OUT | DAC | ADC | MIC | LINEIN | AVDD (3.3 V) | HPVDD (3.3 V) | DCVDD (3.3 V) | DBVDD (3.3 V) | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Record and Playback | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10.7 | 2.2 | 3.6 | 3.1 | mA |
| Playback Only | | | | | | | | | | | | | |
| Oscillator Enabled | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 5.2 | 2.2 | 1.7 | 1.8 | mA |
| External Clock | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 5.1 | 2.2 | 1.7 | 1.7 | mA |
| Record Only | | | | | | | | | | | | | |
| Line Clock | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 4.7 | N/A | 2.0 | 1.9 | mA |
| Line Oscillator | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 4.7 | N/A | 2.0 | 1.8 | mA |
| Microphone 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 4.8 | N/A | 2.0 | 1.9 | mA |
| Microphone 2 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 4.8 | N/A | 2.0 | 1.8 | mA |
| Sidetone (Microphone-to-Headphone Output) | | | | | | | | | | | | | |
| External Clock | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2.0 | 2.2 | 0.2 | 1.7 | mA |
| Internally Generated Clock | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2.0 | 2.2 | 0.2 | 1.7 | mA |
| Analog Bypass (Line Input or Line Output) | | | | | | | | | | | | | |
| External Line | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2.0 | 2.2 | 0.2 | 1.7 | mA |
| Internally Generated Line | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2.0 | 2.2 | 0.2 | 1.7 | mA |
| Power-Down | | | | | | | | | | | | | |
| External Clock | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.001 | <0.001 | 0.03 | 0.03 | mA |
| Oscillator | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0.001 | <0.001 | 0.03 | 0.03 | mA |

## DIGITAL AUDIO I/F, ADDRESS 0x07

**Table 26. Digital Audio I/F Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | BCLKINV | MS | LRSWAP | LRP | WL [1:0] | | FORMAT [1:0] | |

**Table 27. Descriptions of Digital Audio I/F Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| BCLKINV | BCLK inversion control | 0 = BCLK not inverted (default)<br>1 = BCLK inverted |
| MS | Master mode enable | 0 = enable slave mode (default)<br>1 = enable master mode |
| LRSWAP | Swap DAC data control | 0 = output left- and right-channel data as normal (default)<br>1 = swap left- and right-channel DAC data in audio interface |
| LRP | Polarity control for clocks in right-justified, left-justified, and I²S modes | 0 = normal PBLRC and RECLRC (default), or DSP Submode 1<br>1 = invert PBLRC and RECLRC polarity, or DSP Submode 2 |
| WL [1:0] | Data-word length control | 00 = 16 bits<br>01 = 20 bits<br>10 = 24 bits (default)<br>11 = 32 bits |
| FORMAT [1:0] | Digital audio input format control | 00 = right justified<br>01 = left justified<br>10 = I²S mode (default)<br>11 = DSP mode |

## SAMPLING RATE, ADDRESS 0x08

**Table 28. Sampling Rate Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | CLKODIV2 | CLKDIV2 | SR [3:0] | | | | BOSR | USB |

**Table 29. Descriptions of Sampling Rate Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| CLKODIV2 | CLKOUT divider select | 0 = CLKOUT is core clock (default)<br>1 = CLKOUT is core clock divided by 2 |
| CLKDIV2 | Core clock divide select | 0 = core clock is MCLK (default)<br>1= core clock is MCLK divided by 2 |
| SR [3:0] | Clock setting condition | See Table 30 and Table 31. |
| BOSR | Base oversampling rate | USB mode:<br>0 = support for 250 $f_S$ based clock (default)<br>1 = support for 272 $f_S$ based clock<br>Normal mode:<br>0 = support for 256 $f_S$ based clock (default)<br>1 = support for 384 $f_S$ based clock |
| USB | USB mode select | 0 = normal mode enable (default)<br>1 = USB mode enable |

**Table 30. Sampling Rate Lookup Table, USB Disabled (Normal Mode)**

| MCLK (CLKDIV2 = 0) | MCLK (CLKDIV2 = 1) | ADC Sampling Rate (RECLRC) | DAC Sampling Rate (PBLRC) | USB | SR [3:0] | BOSR | BCLK (MS = 1)[1] |
|---|---|---|---|---|---|---|---|
| 12.288 MHz | 24.576 MHz | 8 kHz (MCLK/1536) | 8 kHz (MCLK/1536) | 0 | 0011 | 0 | MCLK/4 |
| | | 8 kHz (MCLK/1536) | 48 kHz (MCLK/256) | 0 | 0010 | 0 | MCLK/4 |
| | | 12 kHz (MCLK/1024) | 12 kHz (MCLK/1024) | 0 | 0100 | 0 | MCLK/4 |
| | | 16 kHz (MCLK/768) | 16 kHz (MCLK/768) | 0 | 0101 | 0 | MCLK/4 |
| | | 24 kHz (MCLK/512) | 24 kHz (MCLK/512) | 0 | 1110 | 0 | MCLK/4 |
| | | 32 kHz (MCLK/384) | 32 kHz (MCLK/384) | 0 | 0110 | 0 | MCLK/4 |
| | | 48 kHz (MCLK/256) | 8 kHz (MCLK/1536) | 0 | 0001 | 0 | MCLK/4 |
| | | 48 kHz (MCLK/256) | 48 kHz (MCLK/256) | 0 | 0000 | 0 | MCLK/4 |
| | | 96 kHz (MCLK/128) | 96 kHz (MCLK/128) | 0 | 0111 | 0 | MCLK/2 |
| 11.2896 MHz | 22.5792 MHz | 8.0182 kHz (MCLK/1408) | 8.0182 kHz (MCLK/1408) | 0 | 1011 | 0 | MCLK/4 |
| | | 8.0182 kHz (MCLK/1408) | 44.1 kHz (MCLK/256) | 0 | 1010 | 0 | MCLK/4 |
| | | 11.025 kHz (MCLK/1024) | 11.025 kHz (MCLK/1024) | 0 | 1100 | 0 | MCLK/4 |
| | | 22.05 kHz (MCLK/512) | 22.05 kHz (MCLK/512) | 0 | 1101 | 0 | MCLK/4 |
| | | 44.1 kHz (MCLK/256) | 8.0182 kHz (MCLK/1408) | 0 | 1001 | 0 | MCLK/4 |
| | | 44.1 kHz (MCLK/256) | 44.1 kHz (MCLK/256) | 0 | 1000 | 0 | MCLK/4 |
| | | 88.2 kHz (MCLK/128) | 88.2 kHz (MCLK/128) | 0 | 1111 | 0 | MCLK/2 |
| 18.432 MHz | 36.864 MHz | 8 kHz (MCLK/2304) | 8 kHz (MCLK/2304) | 0 | 0011 | 1 | MCLK/6 |
| | | 8 kHz (MCLK/2304) | 48 kHz (MCLK/384) | 0 | 0010 | 1 | MCLK/6 |
| | | 12 kHz (MCLK/1536) | 12 kHz (MCLK/1536) | 0 | 0100 | 1 | MCLK/6 |
| | | 16 kHz (MCLK/1152) | 16 kHz (MCLK/1152) | 0 | 0101 | 1 | MCLK/6 |
| | | 24 kHz (MCLK/768) | 24 kHz (MCLK/768) | 0 | 1110 | 1 | MCLK/6 |
| | | 32 kHz (MCLK/576) | 32 kHz (MCLK/576) | 0 | 0110 | 1 | MCLK/6 |
| | | 48 kHz (MCLK/384) | 48 kHz (MCLK/384) | 0 | 0000 | 1 | MCLK/6 |
| | | 48 kHz (MCLK/384) | 8 kHz (MCLK/2304) | 0 | 0001 | 1 | MCLK/6 |
| | | 96 kHz (MCLK/192) | 96 kHz (MCLK/192) | 0 | 0111 | 1 | MCLK/3 |
| 16.9344 MHz | 33.8688 MHz | 8.0182 kHz (MCLK/2112) | 8.0182 kHz (MCLK/2112) | 0 | 1011 | 1 | MCLK/6 |
| | | 8.0182 kHz (MCLK/2112) | 44.1 kHz (MCLK/384) | 0 | 1010 | 1 | MCLK/6 |
| | | 11.025 kHz (MCLK/1536) | 11.025 kHz (MCLK/1536) | 0 | 1100 | 1 | MCLK/6 |
| | | 22.05 kHz (MCLK/768) | 22.05 kHz (MCLK/768) | 0 | 1101 | 1 | MCLK/6 |
| | | 44.1 kHz (MCLK/384) | 8.0182 kHz (MCLK/2112) | 0 | 1001 | 1 | MCLK/6 |
| | | 44.1 kHz (MCLK/384) | 44.1 kHz (MCLK/384) | 0 | 1000 | 1 | MCLK/6 |
| | | 88.2 kHz (MCLK/192) | 88.2 kHz (MCLK/192) | 0 | 1111 | 1 | MCLK/3 |

[1] BCLK frequency is for master mode and slave right-justified mode only.

**Table 31. Sampling Rate Lookup Table, USB Enabled (USB Mode)**

| MCLK (CLKDIV2 = 0) | MCLK (CLKDIV2 = 1) | ADC Sampling Rate (RECLRC) | DAC Sampling Rate (PBLRC) | USB | SR [3:0] | BOSR | BCLK (MS = 1)[1] |
|---|---|---|---|---|---|---|---|
| 12.000 MHz | 24.000 MHz | 8 kHz (MCLK/1500) | 8 kHz (MCLK/1500) | 1 | 0011 | 0 | MCLK |
| | | 8 kHz (MCLK/1500) | 48 kHz (MCLK/250) | 1 | 0010 | 0 | MCLK |
| | | 8.0214 kHz (MCLK/1496) | 8.0214 kHz (MCLK/1496) | 1 | 1011 | 1 | MCLK |
| | | 8.0214 kHz (MCLK/1496) | 44.118 kHz (MCLK/272) | 1 | 1010 | 1 | MCLK |
| | | 11.0259 kHz (MCLK/1088) | 11.0259 kHz (MCLK/1088) | 1 | 1100 | 1 | MCLK |
| | | 12 kHz (MCLK/1000) | 12 kHz (MCLK/1000) | 1 | 1000 | 0 | MCLK |
| | | 16 kHz (MCLK/750) | 16 kHz (MCLK/750) | 1 | 1010 | 0 | MCLK |
| | | 22.0588 kHz (MCLK/544) | 22.0588 kHz (MCLK/544) | 1 | 1101 | 1 | MCLK |
| | | 24 kHz (MCLK/500) | 24 kHz (MCLK/500) | 1 | 1110 | 0 | MCLK |
| | | 32 kHz (MCLK/375) | 32 kHz (MCLK/375) | 1 | 0110 | 0 | MCLK |
| | | 44.118 kHz (MCLK/272) | 8.0214 kHz (MCLK/1496) | 1 | 1001 | 1 | MCLK |
| | | 44.118 kHz (MCLK/272) | 44.118 kHz (MCLK/272) | 1 | 1000 | 1 | MCLK |
| | | 48 kHz (MCLK/250) | 8 kHz (MCLK/1500) | 1 | 0001 | 0 | MCLK |
| | | 48 kHz (MCLK/250) | 48 kHz (MCLK/250) | 1 | 0000 | 0 | MCLK |
| | | 88.235 kHz (MCLK/136) | 88.235 kHz (MCLK/136) | 1 | 1111 | 1 | MCLK |
| | | 96 kHz (MCLK/125) | 96 kHz (MCLK/125) | 1 | 0111 | 0 | MCLK |

[1] BCLK frequency is for master mode and slave right-justified mode only.

## ACTIVE, ADDRESS 0x09

Table 32. Active Register Bit Map

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ACTIVE |

Table 33. Descriptions of Active Register Bit

| Bit Name | Description | Settings |
|---|---|---|
| ACTIVE | Digital core activation control | 0 = disable digital core (default)<br>1 = activate digital core |

## SOFTWARE RESET, ADDRESS 0x0F

Table 34. Software Reset Register Bit Map

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| RESET [8:0] | | | | | | | | |

Table 35. Descriptions of Software Reset Register Bits

| Bit Name | Description | Settings |
|---|---|---|
| RESET [8:0] | Write all 0s to this register to set all registers to their default settings. Other data written to this register has no effect. | 0 = reset (default) |

## ALC CONTROL 1, ADDRESS 0x10

**Table 36. ALC Control 1 Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| ALCSEL [1:0] | | MAXGAIN [2:0] | | | ALCL [3:0] | | | |

**Table 37. Descriptions of ALC Control 1 Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| ALCSEL [1:0] | ALC select | 00 = ALC disabled (default)<br>01 = ALC enabled on right channel only<br>10 = ALC enabled on left channel only<br>11 = ALC enabled on both channels |
| MAXGAIN [2:0] | PGA maximum gain | 000 = −12 dB<br>001 = −6 dB<br>… In 6 dB steps<br>111 = 30 dB (default) |
| ALCL [3:0] | ALC target level | 0000 = −28.5 dBFS<br>0001 = −27 dBFS<br>…<br>1011 = −12 dBFS (default)<br>… In 1.5 dB steps<br>1111 = −6 dBFS |

## ALC CONTROL 2, ADDRESS 0x11

**Table 38. ALC Control 2 Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | DCY [3:0] | | | | ATK [3:0] | | | |

**Table 39. Descriptions of ALC Control 2 Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| DCY [3:0] | Decay (release) time control | 0000 = 24 ms<br>0001 = 48 ms<br>0010 = 96 ms<br>0011 = 192 ms (default)<br>… (Time doubles with every step)<br>1010 = 24.576 sec |
| ATK [3:0] | ALC attack time control | 0000 = 6 ms<br>0001 = 12 ms<br>0010 = 24 ms (default)<br>… (Time doubles with every step)<br>1010 = 6.144 sec |

## NOISE GATE, ADDRESS 0x12

**Table 40. Noise Gate Register Bit Map**

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| 0 | NGTH [4:0] | | | | | NGG [1:0] | | NGAT |

**Table 41. Descriptions of Noise Gate Register Bits**

| Bit Name | Description | Settings |
|---|---|---|
| NGTH [4:0] | Noise gate threshold | 00000 = −76.5 dBFS (default)<br>00001 = −75 dBFS<br>… In 1.5 dB steps<br>11110 = −31.5 dBFS<br>11111 = −30 dBFS |
| NGG [1:0] | Noise gate type | X0 = hold PGA gain constant (default)[1]<br>01 = mute output<br>11 = reserved |
| NGAT | Noise gate control | 0 = noise gate disable (default)<br>1 = noise gate enable |

[1] X = don't care.

# OUTLINE DIMENSIONS

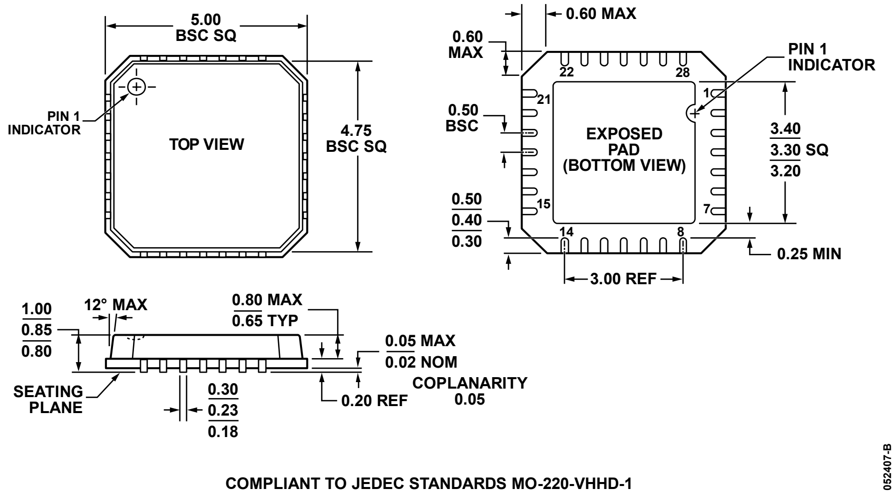



*Figure 32. 28-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*5 mm × 5 mm Body, Very Thin Quad*
*(CP-28-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| SSM2603CPZ-R2[1] | −40°C to +85°C | 28-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-28-4 |
| SSM2603CPZ-REEL[1] | −40°C to +85°C | 28-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-28-4 |
| SSM2603CPZ-REEL7[1] | −40°C to +85°C | 28-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-28-4 |
| SSM2603-EVALZ[1] | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

## NOTES