Amplifiers

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Signal Conditioning – Amplifiers

In the era of digital signal processing, capturing analog “real world” information and conditioning it for digital manipulation presents challenges to engineers less familiar with analog system design. Furthermore, preparing analog signals for conversion to digital data and recreating them from such data involves taking special care of details of little concern in traditional all-analog systems.

This section will address the concerns of signal conditioning for input and output signals. Specifically we will discuss the choice and use of amplifiers. The amplifiers discussed will include operational amplifiers, high speed operational amplifiers and audio power amplifiers.

Operational Amplifiers

Operational amplifiers (Op Amps) are the general purpose work horse of the signal conditioning world. Op Amps are used to build amplifiers, filters, to match impedances, to increase drive capabilities and numerous other functions associated with conditioning input and output signals.

The basic functionality of all op amps are very similar with varitions in performance, special features, and packaging. The questions then become why are hundreds of different op amps available? What are the differences? How do I choose?

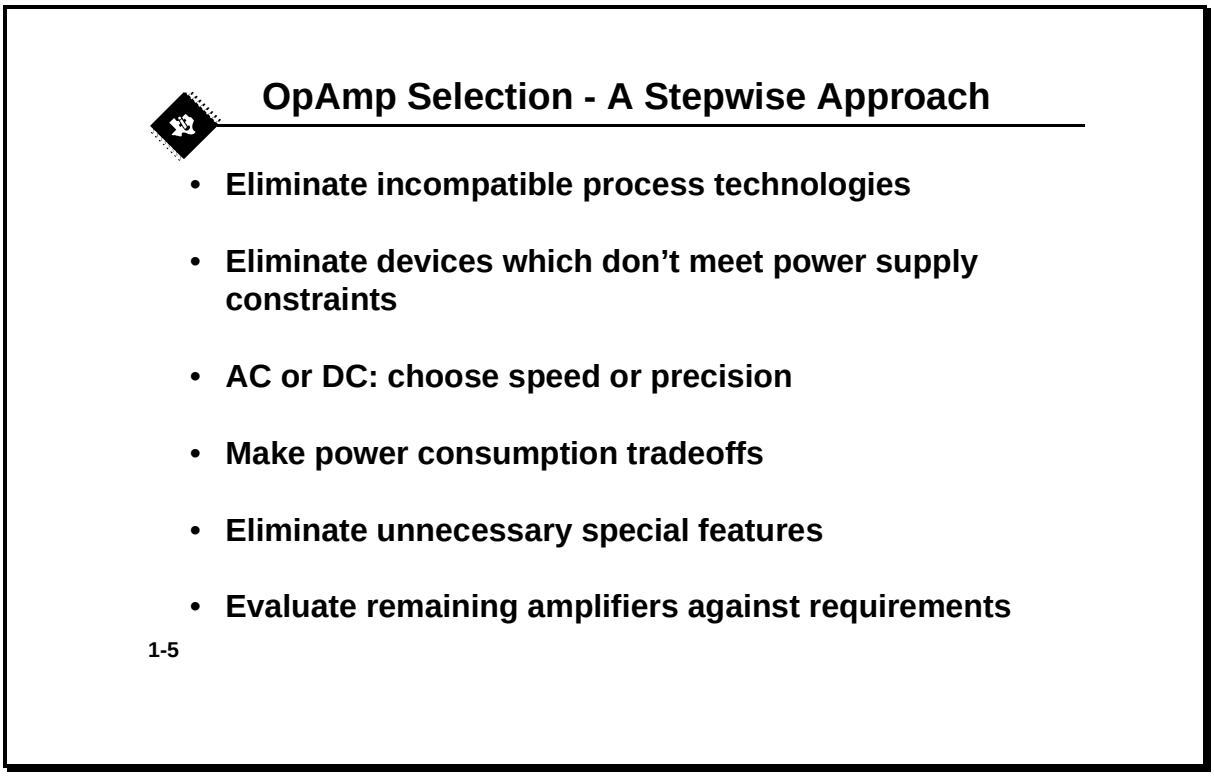
The following sections will address practical considerations such as:

- Choosing the best op amp for a specific application.
- Choosing between single and dual supply operation.
- Evaluating op amp circuits quickly even with surface mount components.

Additional reference material is provided on AC and DC characteristics, input - output considerations and data sheet specifications.

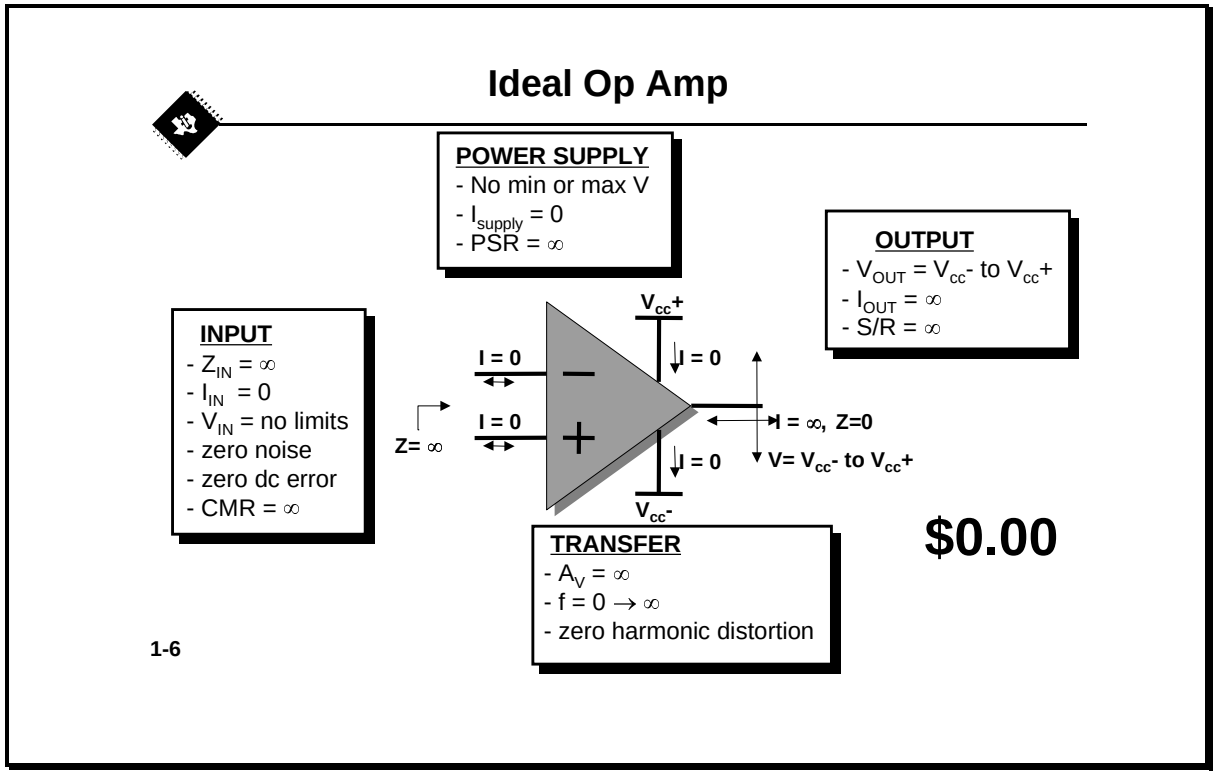
How Do I Select Op Amps? Practical Considerations

An op amp is an integral part of just about any signal chain. Ironically, the op amp has near standard pin-configuration, although there is no consistency of specifications from one manufacturer to the next, or even from one amplifier to the next by a given manufacturer. So which op amp are you going to use in your application? How do you take the hundreds of available op amps and select the one that will fit the criteria of your application the best. It may seem to be a daunting task, but if doesn’t have to be. Armed with a basic understanding of the fundamental characteristics of the op amp and the inherent tradeoffs within the manufacturing processes of the device, a stepwise approach can quickly narrow the choices for a given application down to a manageable few.



Op Amp Selection a Stepwise Aproach

First, eliminate incompatible process technologies. Then, eliminate devices which don't meet the power supply constraints of the application. Next, determine whether the application is ac or dc and understand the inherent power consumption tradeoffs that will come with the increased ac performance. Then eliminate any devices with unnecessary special features. Lastly, evaluate the remaining amplifiers against the requirements of the application. This section will address each of these steps in more detail.



The Ideal Op Amp Characteristics

Before examining the advantages and disadvantages inherent to amplifiers manufactured in the various fabrication technologies commonly used today, it may be helpful first to review the basic characteristics of an “ideal” op amp. And, it is convenient to group the characteristics into four categories: input characteristics, output characteristics, power supply characteristics, and transfer characteristics. These are the four basic facilities for evaluation in selecting a device for a given application as well.

Let’s start with the input characteristics. The ideal op amp would have infinite input impedance and no input bias currents causing no loading on the signal source. It would have infinite input differential as well as common mode voltage making no constraints on the properties of the input signal. There would be perfect matching of the input transistors leading to no dc input offset voltage, and there would be no noise sources with no noise voltage or current generated by the op amp.

Moving to the output characteristics, the ideal op amp would be able to source or sink in infinite amount of current with a rail to rail output swing with an infinite step response (no slew rate limitations) into any resistive, capacitive, or inductive load.

As to the characteristics of the power supply, there would be no minimum voltage requirement, nor a maximum voltage limit. The device would consume no power, dissipate no power and it would work in split- and single-supply systems. For the transfer characteristics, the ideal op amp would have infinite open-loop gain and run at any frequency with no distortion. And the most

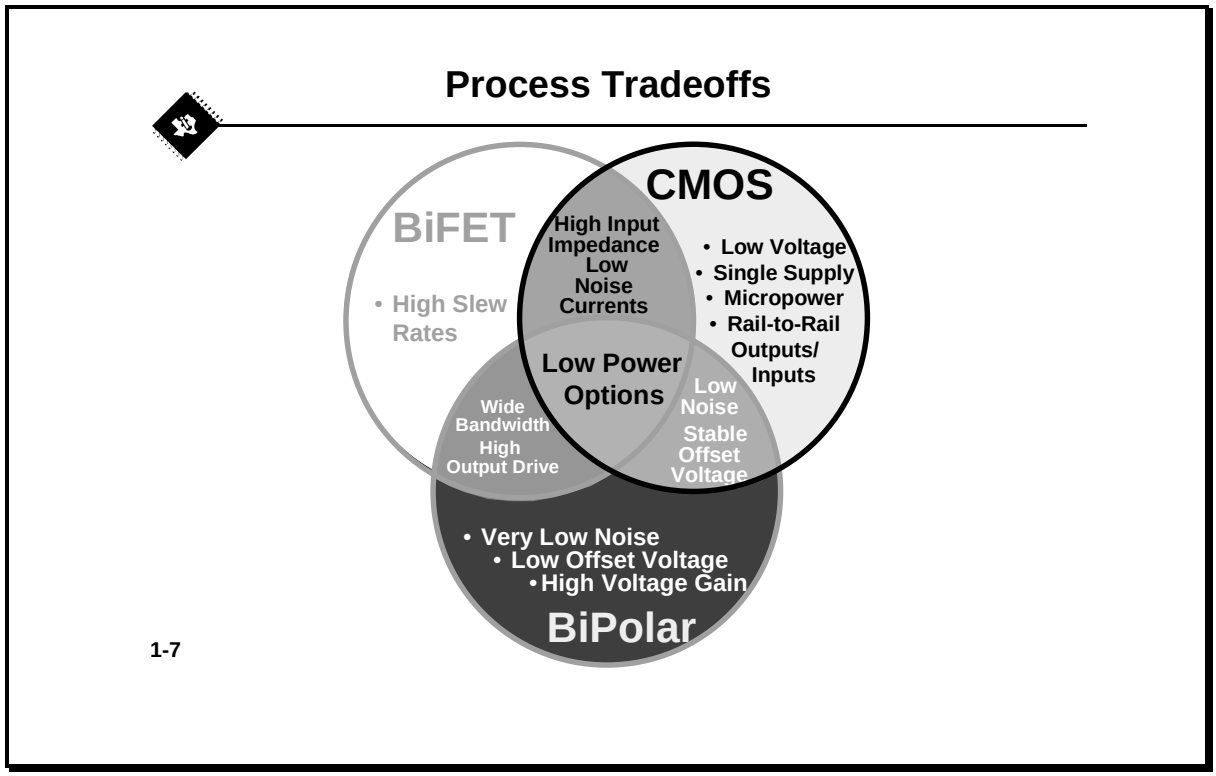
important aspect to any designer, or at least purchaser, it would be absolutely free.

Of course, no op amp exhibits any of these characteristics, but an understanding of them will enable the designer to narrow his choices for further evaluation.

	bipolar	**biFET**	**CMOS**
inputs			
Z_{IN}	low, MΩ	high, TΩ	high, TΩ
I_{IN}	high, nA - μA	low, 10s - 100s pA	low, pA
V_{IN}	usually < V+, sometimes = V-	sometimes = V+, never = V-	sometimes = V+, always = V-
V_N	lowest, < 5 nV avail	high, 20 - 80 nV	some low, 10 - 100 nV
I_N	high, f(I_{IN})	negligible	negligible
V_{IO}	lowest, μV - mV	highest, 10+ mV	varies, 100s μV - mV
outputs			
V_O	usually < V+, sometimes = V-	never = V+, never = V-	sometimes = V+, always = V-
I_O	good, 10 - 100 mA	good, 10 - 100 mA	low, 100s μA - 10s mA
SR	poor to fair, 0 V/ms - 10 V/μs	good, 10 V/μs	poor to fair, 0 V/ms - <5 V/μs
power supply			
V_{CC}	some 3V some single supply 40+ Vmax	min ± 3.5V no single supply 36 - 40+ Vmax	low voltage < 3V all single supply Vmax limited 5-18 V
I_{CC}	med to high, 100s μA - 10 mA	med to high, 100s μA - 3 mA	μpower to avg, μA, 10s μA, 100s μA
transfer			
BW	dc - ~5 MHz	dc - 10+ MHz	dc - 2 MHz

Relative Process Performance

This chart provides a relative indication of various amplifier performance by various technologies. Thes values are given as guidelines with the knowledge that in specifis instances these values are exceeded.



Process Technology Tradeoffs

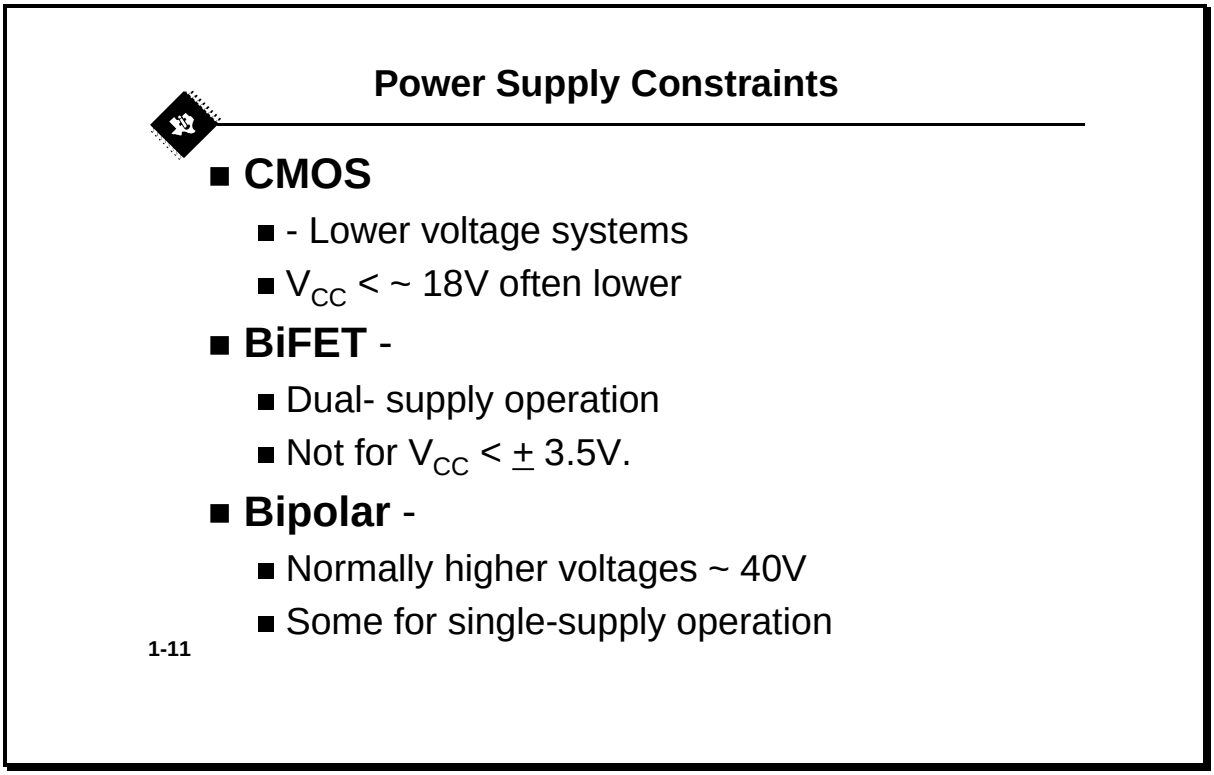
As stated earlier, there are three processes in which most of today's op amps can be categorized: bipolar, biFET, and CMOS. There are inherent tradeoffs within each process which facilitates a natural method for eliminating broad classes of devices, significantly narrowing the designer's choices.

In the bipolar process, an op amp will generally have low voltage noise and the lowest input offset voltage of the three families. The device will have pretty good bandwidth with a fair amount of output drive. However, to achieve this precision, some tradeoffs are made. A bipolar device has low input impedance, high current noise and generally consume a large amount of current from the power supply.

In the biFET process, an op amp will generally have high input impedance and low input bias currents. It will provide pretty good output drive with exceptional slew rate and bandwidth. However, again, other characteristics are sacrificed for these advantages. A biFET device will have high voltage noise and demonstrate the highest input offset voltage. There are constraints on the power supply and they consume a fairly large amount of current.

As for op amps fabricated in the CMOS process, they exhibit the highest input impedance and lowest input bias current of the three classifications. They have the widest input and output voltage ranges with respect to the supply rails and they are micropower devices. Conversely they have poor output drive, poor to fair slew rates and low bandwidths.

It should be noted these are not to be taken as absolutes. Process limits can be exploited and design techniques used to extend process capabilities. But beware of the tradeoffs necessary for the additional advantages .



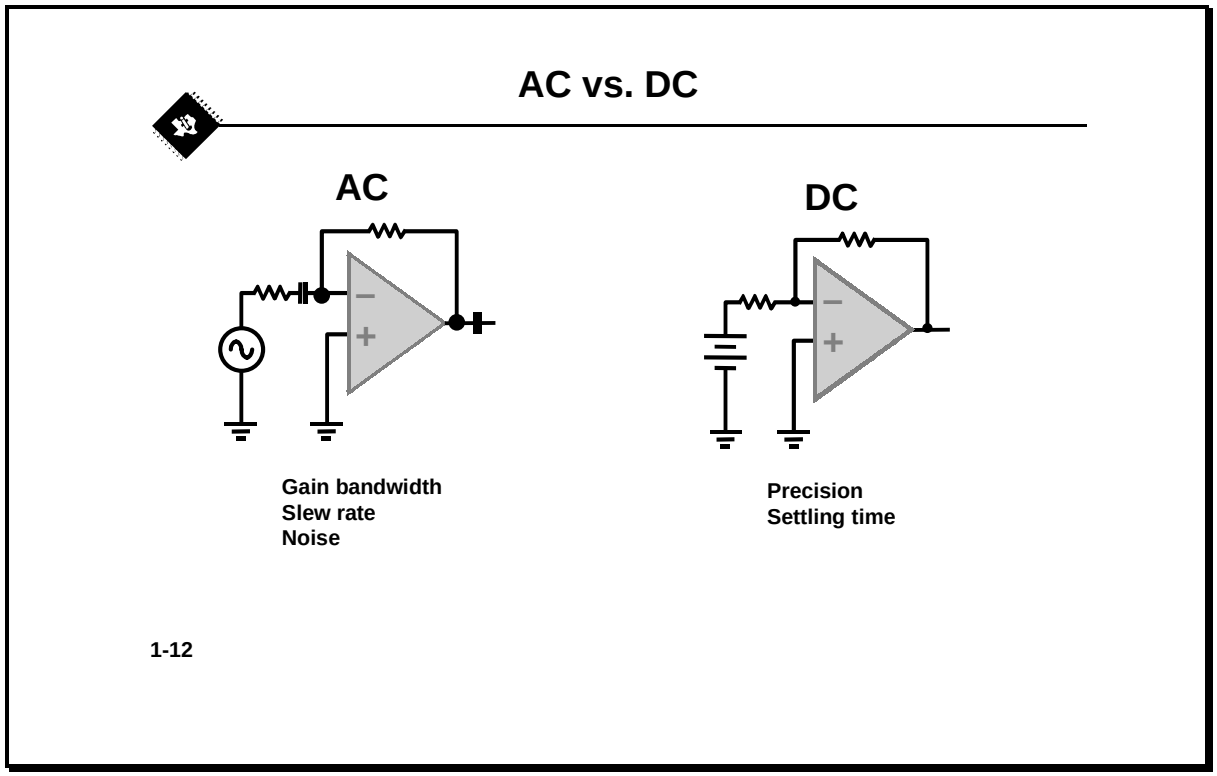
Power Supply Constraints

Armed with this basic understanding of process-related strengths and weaknesses, the easiest first cut against available amplifiers is made based on power supply voltage, minimum or maximum. Some conclusions can be made by considering the supply voltage characteristics as previously stated:

CMOS amplifiers are not suited for higher-voltage systems. The maximum supply voltage is generally around 18V and in many cases even as low as 7V. CMOS op amps are well-suited for single-supply, low-voltage systems.

BiFET op amps will not work in low voltage systems. If your system is less than ± 3.5V, a biFET op amp is a choice. The input common mode voltage is 3.5V from the top supply rail to 3.5V from the bottom supply rail. Even with the smallest signal, the op amp is useless with a supply range of less than 7V. Of course, some biFETs are better than others but this is generally true. They are not designed for single-supply systems. However, they can be used if the supply voltage is adequate and careful attention is paid to signal and load referencing.

Bipolar op amps are the most forgiving when it comes to power supply requirements. The bipolar process is generally capable of higher voltages, usually around 40V, and some can even be used in single supply systems. However, they generally have lower common mode input voltage ranges than a CMOS device which would generally be the more logical place to start looking unless other characteristics were more critical. By eliminating or focusing on one or more technologies, you not only remove hundreds of amplifiers from contention, but frequently also limit the number of manufacturers you consider. Many manufacturers offer only bipolar amplifiers; a select few are prolific in CMOS; and biFETs are similarly distributed.

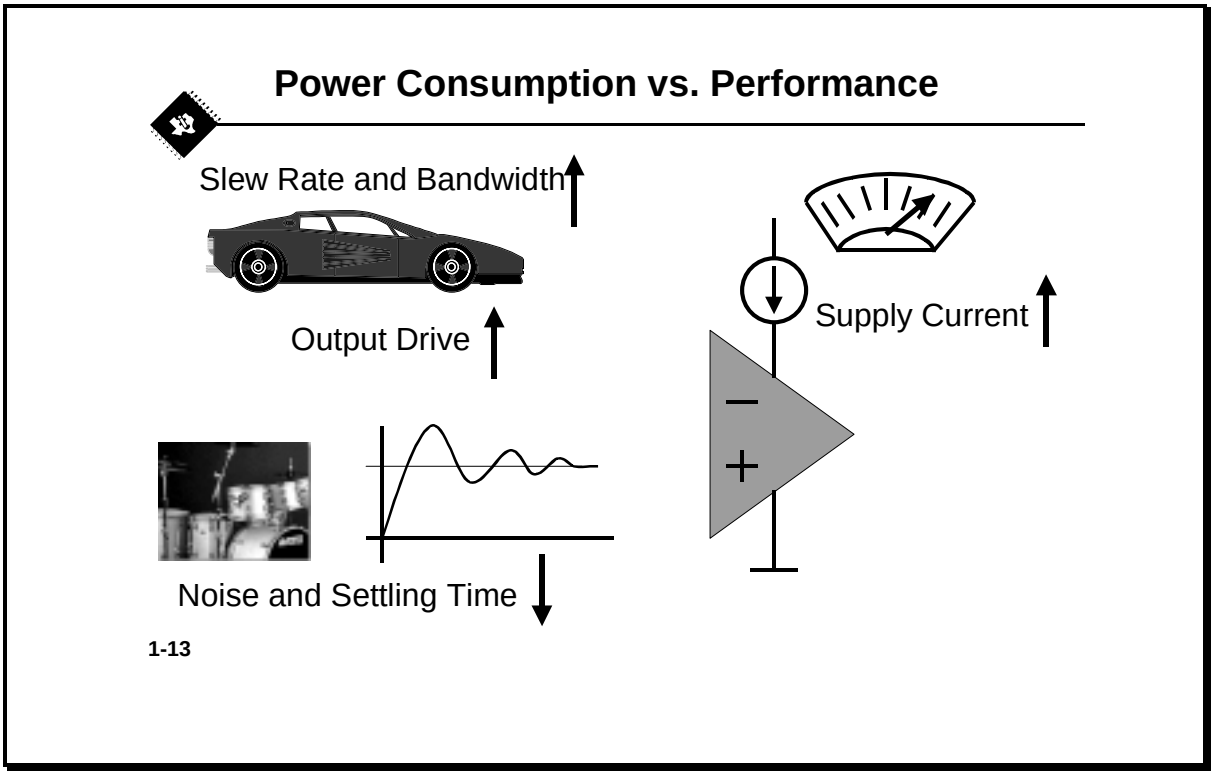


Signal Characteristics AC vs DC.

Another guide for choosing an amplifier for a given sub-circuit is to classify that circuit as primarily ac or dc. In a dc system, the signals are generally slow moving and typically require little bandwidth. Unless there is a step function, slew rate and settling time are also of lesser importance. In an ac circuit the signal places significant requirements on gain-bandwidth and slew rate, whereas dc precision is generally unimportant. A signal which is ac-coupled does not require a precision grade op-amp; however a dc-coupled ac signal may.

Obviously, small signals require higher-precision amplifiers. Precision and low noise become especially critical in digital systems as the number of bits of resolution increases. A designer of a mixed signal application will have an error budget essential to the performance of his system. As a fellow application engineer has stated to me on several occasions, you can't run a Cadillac engine with a Yugo front end. The op amp conditioning the source signal for the A to D must have less error than the resolution of that A to D, or that resolution is decreased.

AC performance comes with tradeoffs, not the least of which is power consumption. In fact, power consumption frequently becomes the pivotal parameter in finalizing op amp selection, especially in the ever-growing market of battery powered applications.



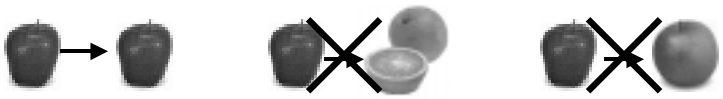
Power Consumption vs Performance

Engineers often find themselves having to make difficult decisions trading power consumption for required performance. There are some first-order relationships that drive these decisions.

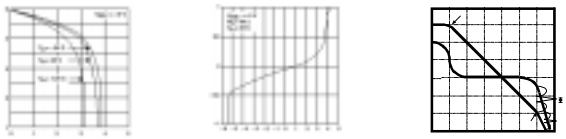
AC performance such as slew rate, bandwidth, and settling time come at the expense of increased power consumption. The noise figure varies inversely to the first stage current; so to achieve a lower noise op amp, higher supply current must be sacrificed. Also, in many families of amplifiers, output drive is proportional to the supply current as well.

Frequently manufacturers offer two or more power options of the same op amp. Making the judicious tradeoffs between lowest power and required ac performance, noise, or output drive is often among the most important decisions a designer must make.

The Final Cut



1. Always compare apples to apples



2. Graphed performance often provides valuable insight

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The final step in choosing an amplifier is usually a matter of a more thorough comparison of key specifications and performance graphs to determine the best fit. A few words of caution:

While op amp configurations are largely standardized, parametric specifications are not. Test conditions may vary, usually to showcase the amplifier at its best. This is called specsmanship. Compounding this is the technology mix: selecting an amplifier based on a comparison of a few specifications fails to comprehend the sometimes subtle but critical characteristics of bipolar, biFET, or CMOS fabrication processes. In this, especially, electronic selection guides can be misleading, yielding a mix of incompatible amplifiers as a consequence of searching a database of raw numbers, as I pointed out earlier. Paper selection guides are often a better place to start as factory “experts” typically group amplifiers so that an “apples to apples” comparison can be made. Be careful not to make apples to oranges comparisons or even apples to different types of apples. They may have the same flavor, but have entirely different texture.

Second, NEVER choose an op amp based solely on specifications! It is a rare circuit that operates with signals and load conditions that are identical to the configurations that the parameters are specified under. It’s no coincidence that op amp datasheets are heavy with graphs plotting performance against a number of variables. Unspecified, and sometimes undesirable, characteristics typically turn up in these curves. Understanding how your op amp is configured and extrapolating from the curves back to the specifications is critical in ensuring your selection will perform as expected.

The Final Cut

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3. Added features come with a price

4. Amplifier models often fail to describe real performance

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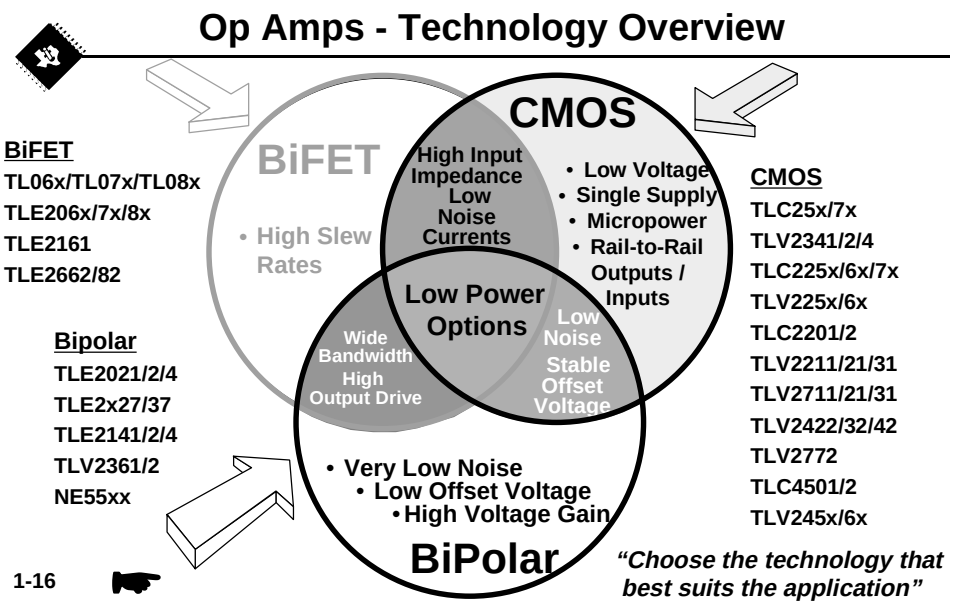
Be aware, but beware, of special features or added performance. They come at a price and, almost always, with some tradeoff in performance. Don't be hasty to pay for features you don't need.

And finally, a note about models: amplifier models are a poor tool for simulating performance of a real circuit. They are at best useful for making sure nothing has been left disconnected. Models available today are typically derived from the datasheet specifications such that if the test circuit were modeled, the simulator would output the specifications. They completely fail to comprehend boundary conditions or second-order effects, and are of little use in predicting behavior of anything but the most textbook configurations. With op amps, there is no substitute for evaluating the real circuit in the lab.

In summary, choosing an op amp doesn't need to be an intimidating task. Making common sense decisions can lead the design engineer to a few devices from which a more studied selection can be made.



Op Amp Selection Table - What is Available?

Low Noise Operational Amplifier Selection Guide

	#amplifiers	V_{CC} (V) (min/max)	V_{IO} (µV) (typ/max)	I_{CC} (mA) (typ/max)	$V_{n, typ}$ (nV/Hz) (@1kHz)	SR (V/µs) (typ)	GBW (MHz) (min/typ)
Bipolar							
THS4001	S	±2.5/±16	2000/8000	7.80/9.50	12.5	400	-- /270
TLE2027	S	±4/±22	20/100	3.80/5.30	2.5	2.8	7.0/13.0
TLE2037	S	±4/±19	20/100	3.80/5.30	2.5	7.5	35.0/50.0
TLE2227	D	±4/±22	100/350	7.30/10.60	2.5	2.5	7.0/13.0
TLE2237	D	±4/±19	100/350	7.30/10.60	2.5	5.0	35.0/50.0
TLE2141	S	±2/±22	200/900	3.50/4.50	10.5	45	6.0/ --
TLE2142	D	±2/±22	290/1200	6.90/9.00	10.5	45	6.0/ --
TLE2144	Q	±2/±22	600/2400	13.80/18.00	10.5	45	6.0/ --
TLV2361	S	±1/±2.5	1000/6000	1.40/2.25	9	2.5	-- /6.0
TLV2362	D	±1/±2.5	1000/6000	2.80/4.50	9	2.5	-- /6.0
TLC2654	S	±1.9/±8	5/20	1.50/2.40	13	2.0	-- /1.9
BiFET							
TLE2071	S	±2.5/±19	490/4000	1.70/2.20	11.6	40	8.0/10.0
TLE2072	D	±2.5/±19	1100/6000	3.10/3.60	11.6	40	8.0/10.0
TLE2074	Q	±2.5/±19	1600/5000	6.50/7.50	11.6	40	8.0/10.0
TLE2081	S	±2.5/±19	490/6000	1.70/2.20	11.6	40	8.0/10.0
TLE2082	D	±2.5/±19	1100/7000	3.10/3.60	11.6	40	8.0/10.0
TLE2084	Q	±2.5/±19	1600/7000	6.50/7.50	11.6	40	8.0/10.0
TLE2682	S	3.5/15	1100/7500	8.90/ --	11.6	40	8.0/10.0

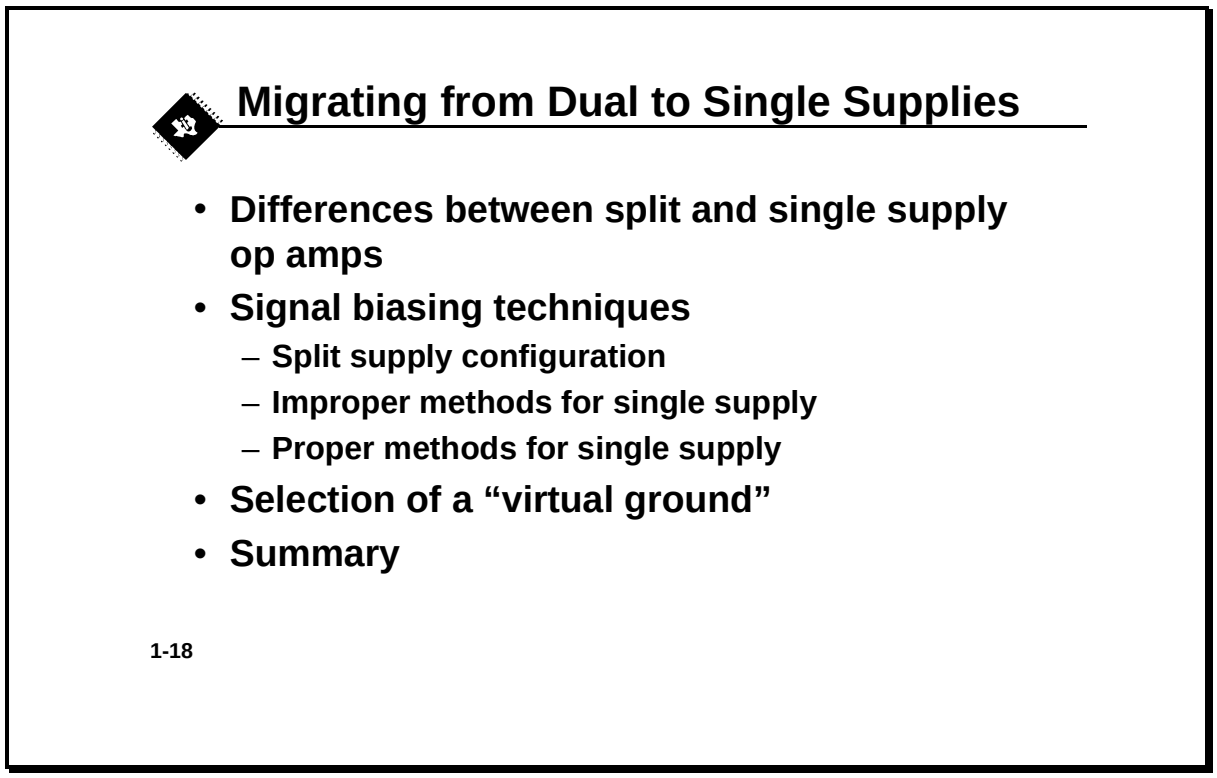
Low Noise Operational Amplifier Selection Guide (continued)

	#amplifiers	V_{CC} (V) (min/max)	V_{IO} (µV) (typ/max)	I_{CC} (mA) (typ/max)	$V_{n, typ}$ (nV/Hz) (@1kHz)	SR (V/µs) (typ)	GBW (MHz) (min/typ)
CMOS							
TLC2201	S	4.6/16	100/500	1.00/1.50	8	2.5	-- /1.8
TLC2202	D	4.6/16	100/1000	1.70/2.60	8	2.5	-- /1.9
TLC2252	D	4.4/16	200/1500	0.070/0.125	19	0.12	-- /0.2
TLC2254	Q	4.4/16	200/1500	0.14/0.25	19	0.12	-- /0.2
TLC2262	D	4.4/16	300/2500	0.40/0.50	12	0.55	-- /0.82
TLC2264	Q	4.4/16	300/2500	0.80/1.00	12	0.55	-- /0.71
TLC2272	D	4.4/16	300/2500	2.20/3.00	9	3.6	-- /2.18
TLC2274	Q	4.4/16	300/2500	4.40/6.00	9	3.6	-- /2.18
TLC4501	S	4/6	-- /80	1.00/1.50	12	2.5	-- /4.7
TLC4502	D	4/6	-- /100	2.50/3.60	12	2.5	-- /4.7
TLV2772	D	2.2/5.5	360/2500	2.00/4.00	17	10.5	-- /5.1
TLV2252	D	2.7/8	200/1500	0.068/0.125	19	0.1	-- /0.187
TLV2254	Q	2.7/8	200/1500	0.135/0.25	19	0.1	-- /0.187
TLV2262	D	2.7/8	300/2500	0.40/0.50	12	0.55	-- /0.67
TLV2264	Q	2.7/8	300/2500	0.80/1.00	12	0.55	-- /0.67
TLV2442	D	2.7/10	300/2000	1.50/2.20	18	1.3	-- /1.75
TLV2231	S	2.7/10	750/3000	0.75/1.00	16	1.25	-- /1.9
TLV2731	S	2.7/10	700/3000	0.75/1.50	16	1.25	-- /1.9

Precision Op Amp Selection Guide

	#amplifiers	V_{CC} (V) (min/max)	V_{IO} (µV) (typ/max)	I_{CC} (mA) (typ/max)	I_{IB} (nA) (typ,max)	CMRR (dB) (min/typ)	$V_{n, typ}$ (nV/Hz) (@1kHz)
Bipolar							
TLE2021	S	±2/±20	120/500	0.20/0.30	25/70	100/115	15
TLE2022	D	±2/±20	150/500	0.55/0.70	35/70	95/106	15
TLE2027	S	±4/±22	20/100	3.80/5.30	15/90	100/131	2.5
TLE2037	S	±4/±19	20/100	3.80/5.30	15/90	100/131	2.5
TLE2227	D	±4/±22	100/350	7.30/10.60	15/90	98/115	2.5
TLE2237	D	±4/±19	100/350	7.30/10.60	15/90	98/115	2.5
TLE2141	S	±2/±22	200/900	3.50/4.50	700/1500	85/108	10.5
TLE2142	D	±2/±22	290/1200	6.90/9.00	700/1500	85/108	10.5
TLC2654	S	±1.9/±8	5/20	1.50/2.40	50/ --	-- /125	13
CMOS					**I_{IB} (pA)**		
TLC1078	D	1.4/16	160/450	0.020/0.034	0.6/ --	-- /95	68
TLC1079	Q	1.4/16	190/850	0.040/0.068	0.6/ --	-- /95	68
TLC277	D	3/16	200/900	1.40/3.20	0.6/ --	-- /80	25
TLC279	Q	3/16	200/900	2.70/6.40	0.6/ --	-- /80	25
TLC2201	S	4.6/16	100/500	1.00/1.50	1/ --	-- /110	8
TLC2202	D	4.6/16	100/1000	1.70/2.60	1/ --	-- /100	8
TLC2252	D	4.4/16	200/1500	0.070/0.125	1/ --	-- /83	19
TLC2254	Q	4.4/16	200/1500	0.14/0.25	1/ --	-- /83	19
TLC2262	D	4.4/16	300/2500	0.40/0.50	1/ --	-- /83	12
TLC2264	Q	4.4/16	300/2500	0.80/1.00	1/ --	-- /83	12
TLC2272	D	4.4/16	300/2500	2.20/3.00	1/ --	-- /75	9
TLC2274	Q	4.4/16	300/2500	4.40/6.00	1/ --	-- /75	9
TLC4501	S	4/6	-- /80	1.00/1.50	1/ --	90/100	12
TLC4502	D	4/6	-- /100	2.50/3.60	1/ --	90/100	12
TLV2252	D	2.7/8	200/1500	0.068/0.125	1/ --	-- /65	19
TLV2254	Q	2.7/8	200/1500	0.135/0.25	1/ --	-- /65	19
TLV2262	D	2.7/8	300/2500	0.40/0.50	1/ --	-- /65	12
TLV2264	Q	2.7/8	300/2500	0.80/1.00	1/ --	-- /65	12
TLV2422	D	2.7/10	300/2000	0.10/0.15	1/ --	-- /83	23
TLV2432	D	2.7/10	300/2000	0.195/0.25	1/ --	-- /83	22
TLV2442	D	2.7/10	300/2000	1.50/2.20	1/ --	-- /75	18

Design Considerations Migrating from Dual to Single Supplies



Introduction

As companies are continuously striving to develop more portable and cost effective products, the number of analog engineers being asked to migrate their split supply amplifiers to a single supply voltage is increasing. The use of amplifiers with a single supply voltage introduces some issues that didn't necessarily need to be considered with split supply designs. Violation of the common-mode input range is one of the most common mistakes. Therefore, proper input signal biasing using a dc bias voltage is a major key to success in single supply systems. This dc bias voltage (sometimes called a virtual ground) can be generated using several methods; each with its own advantages and disadvantages.

Split versus Single Supply

- **Majority of all amplifiers can be used with either configuration**
- **Differences are in common-mode input voltage range (V_{ICR}) and output voltage(V_O)**
- **Split supply op amps have a few volts of "headroom" from the rails**
- **Single supply op amps' V_{ICR} and V_O include ground**

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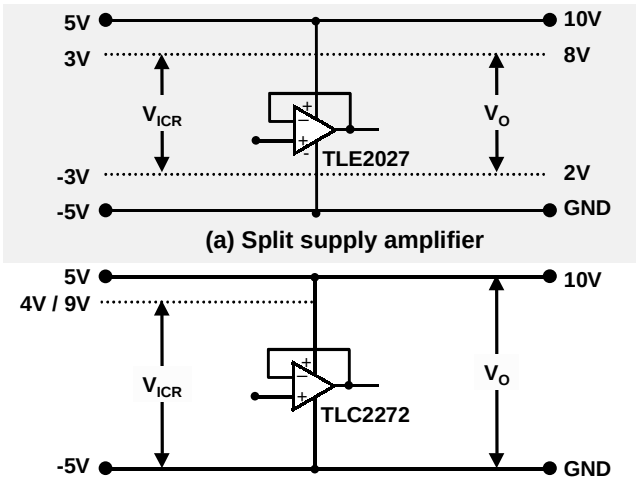
Split supply and single supply amplifiers…is there a difference?

Many questions arise when the discussion of whether or not amplifiers specified for split supply can be operated with a single supply and vice versa. Actually, the overwhelming majority of operational amplifiers on the market today can be used with either. The amplifier can be powered by any combination of split or single supply voltages as long as the total voltage across the amplifier doesn't exceed the absolute maximum ratings. The only real differences between split supply amplifiers and those designed for single supply operation are their common-mode input voltage range and output voltage swing. The common-mode input voltage range of an amplifier is defined as the range of input voltages common to both terminals that if exceeded may cause the op amp to cease functioning properly. It is usually symbolized in the datasheet as V_{ICR} or V_{CM}. The output voltage range (V_O) can be broken up into a high level (V_{OH}) and low level value (V_{OL}) and defines the maximum voltage range the output of the amplifier can swing.

Split vs. Single Supply Amplifier



1-20

A split supply amplifier typically has a common-mode input voltage range and output voltage swing that extends to within a few volts of the supply rails. The figure above shows a TLE2027 configured as a voltage follower. Operating from +/-5 V supplies, the amplifier is able to swing +/ 3 V on the input and output; therefore providing 6 volts of dynamic range. If a small signal biased just above ground is fed into the input, the amplifier will operate on it without issue. Now powering the amplifier with a +10 V single supply, the user will also get 6 volts of usable signal range, since the total voltage applied to the amplifier is the same. However, the common-mode input voltage range and output voltage now swings from +2 V to +8 V. The same signal is now outside of the linear operating range of the amplifier and therefore will not be operated on properly.

A single supply amplifier is designed so the common-mode input voltage range and output voltage swing includes the negative rail (or ground in a single supply system) and extends to within one or two volts of the positive rail. There are also rail-to-rail amplifiers available that have a V_{ICR} and V_O that includes both supply rails. Figure 1b shows the TLC2272 rail-to-rail output amplifier in the same voltage follower configuration. The common-mode input voltage range is 0V to 9V and the output swings from 0 V to +10V with a +10 V single supply (or V_{ICR}= –5 V to 4V and V_O=-5V to 5V with +/-5 V supplies). Therefore, any signals near ground are still within the operating region of the amplifier and will be passed.

Signal biasing techniques for single supply op amps

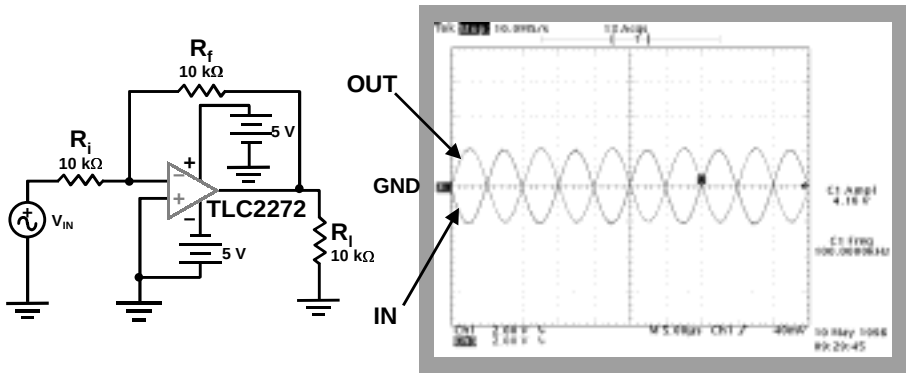
- **One of the most common mistakes**
- **Split supply amplifiers are usually referenced to ground**
- **Need to generate a bias voltage (virtual ground) for single supply systems**
- **Bias voltage of $V_{ICR}/2$ will provide max. dynamic range**

1-21

Biasing of the input signal in single supply applications

One of the most frequent calls we receive at the factory is from split supply amplifier users having problems using an amplifier with a single supply voltage. The root of the problem usually comes from the violation of the common-mode input voltage specifications of the amplifier. Proper biasing of the input signal, especially in single supply applications is extremely important.

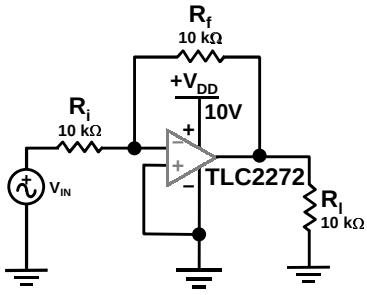
Op amp configured with an inverting gain of 1 powered by dual +/-5V supplies

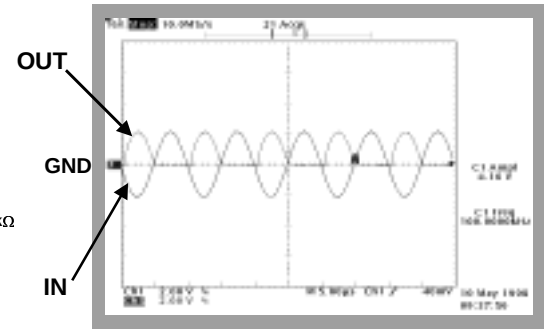


1-22

The figure above shows the TLC2272 in an inverting configuration with a gain of -1. The positive input pin and load are tied to ground. The input waveform is a 4 V peak-to-peak, 100kHz-sine wave referenced to ground. Since the amplifier is using +/-5 V supplies, the signal is well within the linear region and the output is therefore an inverted version of the input.

Improper signal biasing for a single supply amplifier (#1)



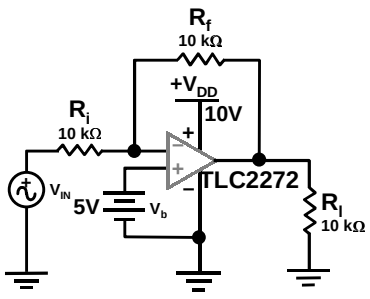


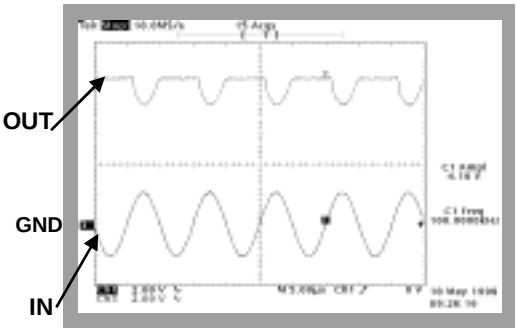
- **Amplifier is powered by a +10V supply with the input waveform, IN+, and R_L referenced to GND**
- **V_{IN} = 4.0V_{pp} @ 100kHz**
- **Output is a half-wave rectified signal**

1-23

The figure above shows this same amplifier with a gain of –1 now operating from a single +10 V supply. The same ground referenced signal is applied to the amplifier and, both the positive input and load are tied to ground. The resulting output waveform is now a half-wave rectified version of the input. This is obviously not what we are looking for. The amplifier is unable to operate on the positive portions of the waveform since the resulting output is at a voltage potential more negative than the lower supply rail. This causes the output to saturate just above the negative supply rail (ground in this case). All negative input voltages will drive the output into its normal positive output swing.

Improper signal biasing for a single supply amplifier (#2)





- Voltage is applied to IN+ in an attempt to bias the input signal
- Both dc and ac are gained up causing the output to saturate into the top rail

$$V_O = V_B\left(\frac{R_f}{R_i} + 1\right) - V_i\left(\frac{R_f}{R_i}\right)$$

1-24

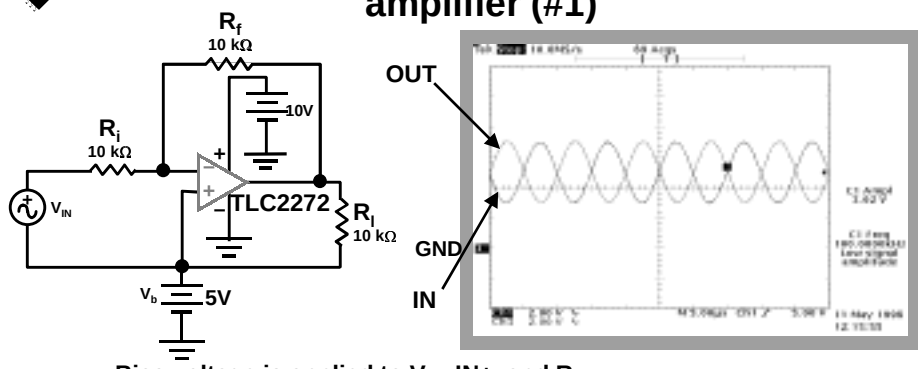
This figure shows, the amplifier with a dc bias voltage (virtual ground) equal to half of the supply voltage (in this case +5 V) applied to the positive input pin in an attempt to bias up the input signal to mid rail. Using Kirchhoff's junction rule at the negative input of the op amp, the following equation can be derived for the output voltage of this amplifier.

$$V_O = V_B\left(\frac{Rf}{Ri} + 1\right) - Vi\left(\frac{Rf}{Ri}\right)$$

The second portion of the equation represents the gain of the amplifier at the inverting input terminal. It can be easily identified as the gain equation usually used for inverting amplifier configurations. The first term represents the gain at the non-inverting input terminal. In a split supply application, the positive input is usually connected to ground and therefore the dc bias voltage (V_B) is zero, leaving the typical inverting amplifier gain equation. However, since we are biased at a point other than ground this term must be taken into consideration. In our example, this dc voltage is gained up and causes the output to saturate just below the positive supply rail. The output remains saturated for all negative portions of the input signal. All positive inputs on the inverting terminal will subtract from the dc output voltage. Again, this is clearly not what we had hoped for. The resulting waveform can be seen in figure 3b.

The previous figure illustrates two very common mistakes made when attempting to bias the input signal in a single supply application. Now we will analyze a few simple methods of proper biasing.

Proper signal biasing for a single supply amplifier (#1)

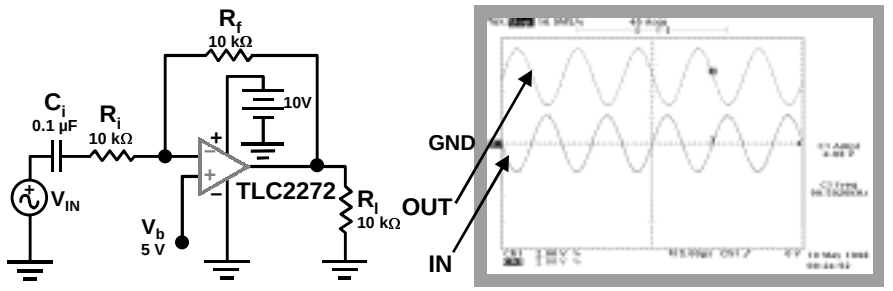


- **Bias voltage is applied to V_{IN}, IN+, and R_L**
- **Input and output waveforms swing freely about V_B**
- **Amplifier sees the same scenario if powered by +/-5V and ground referenced**

1-25

This figure shows the same inverting gain stage we have been discussing in the previous examples. The input waveform, positive input pin and load are now connected to a virtual ground equal to $V_{CC}/2$. With the virtual ground being set at $V_{CC}/2$, the circuit is now equal distant from both supply rails, allowing for maximum dynamic range. The signal is able to swing freely about the virtual ground without clipping.

Proper signal biasing for a single supply amplifier (#2)



- Capacitor (C_i) blocks the flow of dc current
- Output is an inverted version of the input referenced to VB
- $V_O = V_B\left(\frac{\frac{R_f}{\frac{1}{sCi}+R_i}+1\right) - V_i\left(\frac{\frac{R_f}{\frac{1}{sCi}+R_i}\right)$
- Capacitor makes the system frequency dependent
- Low frequency cutoff point; $f = 1/2pC_iR_i$ ($f = 159Hz$)

1-26

Another example of proper input signal biasing is shown in the figure 4b. The configuration is almost identical to the one analyzed in figure 3b, but a capacitor has been added to the input. The capacitor blocks the flow of dc current and prevents the amplifier from gaining up the dc bias voltage on the non-inverting input pin. All ac current passes through the capacitor, so the output waveform is an inverted version of the input biased at V_B (in this case + 5V). This can also be explained using the output voltage equation derived earlier. Adding the impedance of the capacitor, the equation is as follows.

$$V_O = V_B\left(\frac{Rf}{\frac{1}{sCi}+Ri}+1\right) - Vi\left(\frac{Rf}{\frac{1}{sCi}+Ri}\right)$$

Again, the first term represents the gain of the non-inverting input terminal. Assuming our virtual ground is a pure dc voltage (i.e. no ac noise, etc), the impedance of the capacitor is essentially infinite, which makes the gain factor in this equation go to zero, leaving only V_B. Therefore the dc output of this amplifier will be equal to the bias voltage. The gain at the inverting terminal of the op amp remains the same with one exception. With the inclusion of the capacitor, the gain of this circuit is now frequency dependent. There is an RC high pass filter created on the input by Ri and Ci. The values of these components determine the low frequency cutoff for the system. The frequency

at which the gain has been attenuated by –3dB can be calculated using the following equation.

$$f(-3dB) = 1/2\pi RiCi$$

For our circuit Ci = 0.1μF and Ri = 10kΩ, making a low frequency cutoff point of 159Hz. Any signals lower than this frequency will be attenuated at 20dB/decade.

In figure 4c, a capacitor has also been added at the output of the amplifier. This output capacitor blocks all dc current across the load. This changes the dc bias point across the load from V_B to ground. The capacitor forms an RC network with the load resistor and will also cause signal frequencies near its low frequency limit to attenuate. In this example, the capacitor and resistor values are the same as in figure 4b so the low frequency cutoff point is again 159 Hz. With the inclusion of the second RC network, signals at the cutoff frequency will now be attenuated by –6dB instead of –3dB.

The three previous examples demonstrate the proper way to bias the input signal in a single supply application. The first example is probably the most desirable as no external components are required (other than the virtual ground). However, if the application doesn't allow the input waveform, load, and positive input pin of the amplifier to be referenced to a virtual ground, then examples two and three would be more suitable. The designer must always keep in mind the addition of capacitors make the circuit frequency dependent.

Selection of a “virtual ground”

- Critical to select the proper method for the application
- Key parameters for effective virtual ground
  - Power dissipation
  - Load/supply Regulation
  - Output impedance
- What are the key concerns and how much are you willing to pay?

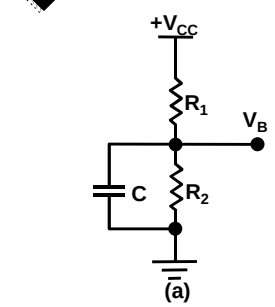
1-27

Methods for generating a virtual ground

We have spent some time discussing both proper and improper methods for biasing single supply amplifiers using a dc bias voltage. However, little time has been dedicated to how this virtual ground is generated. In the examples presented earlier we were assuming this dc bias voltage was ideal. We all know this is never the case though. We will now look at several examples of virtual grounds and their inherent advantages and disadvantages.

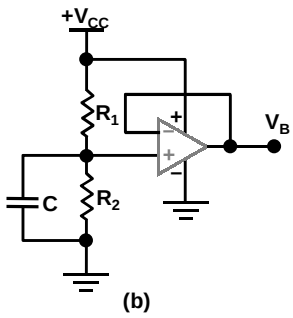
Some parameters that should be evaluated when selecting a virtual ground are power dissipation, load and input regulation, and output impedance. Ultimately, the decision on which virtual ground to use will come down to what key care-abouts the engineer has for his/her particular application and how much they are willing to pay for them.

Generating a "Virtual Ground"



Advantages	Disadvantages
• Low Cost	• Supply rejection
	• Power dissipation
	• High Z_O
	• Load regulation

1-28

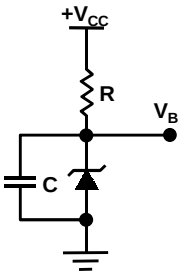


Advantages	Disadvantages
• Load regulation	• Supply rejection
• Low Z_O	• Increase in board space
	• Component cost
	• Power dissipation

Probably the most widely used technique for generating a virtual ground is a resistor divider plus a bypass capacitor. It is also probably the most cost effective solution available, as the price of resistors and capacitors are usually much less than integrated circuits. However, among its disadvantages are poor load regulation and low supply rejection. If the load is tied to the virtual ground, any high source or sink current requirements will cause errors in the dc bias voltage. Also, any type of noise ripple generated from the power supply will feed through the divider and introduce errors into the system. The level of power dissipation of the divider can be calculated using the total series resistance of the divider and the supply voltage. For a 1-kΩ divider with a +5 V power supply, the power dissipation is 12.5 mW. This is shown in section a of the figure above.

Using an amplifier to buffer this resistor divider will solve the load regulation problem. The amplifier is able to handle load current demands much more effectively than the divider network. Unfortunately, an additional component is needed which will increase the cost of your system. A large increase in board space used to be a major concern of designers when considering this method. However, with the recent introduction of amplifiers in extremely small packages, like SOT23, the extra real estate needed is minimized. The supply current of the additional amplifier also takes away from battery life in portable applications. This configuration is shown in section b.

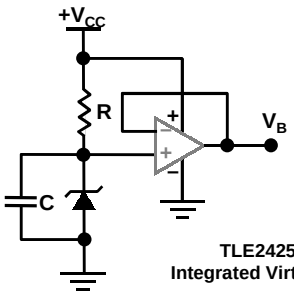
Generating a "Virtual Ground"



(c)

Advantages
- Load regulation
- Supply rejection

Disadvantages
- Power hungry
- High Z_O



TLE2425/26
Integrated Virtual Gnd.

(d)

Advantages
- Load regulation
- Supply rejection
- Low Z_O

Disadvantages
- Component cost
- Power dissipation
- Board space increase

1-29

Another method for generating a virtual ground is by using a voltage reference. This can be seen in the figure above (c.). The active device significantly increases input regulation over the previous two methods. However, a drawback of the voltage reference is its high power consumption. For the reference to offer a very stable dc voltage, enough bias current must be available at all times. This equates into constant levels of dc current, which increases your total power consumption. For this reason, this is not the most ideal case especially in portable applications.

This reference can also be buffered with an amplifier. The input and load regulation from the reference and amplifier respectively is by far the best among the four solutions. Added components, power dissipation and cost are the penalties. The figure above (d) shows this configuration.

The selection of a virtual ground is really dependent on the needs of the particular application. If the system will demand high source and sink current capabilities from the virtual ground then one may need to select an option with a buffer. If input regulation is a critical parameter then use of a voltage reference might be the best option. Less demanding applications may only need a simple, low cost divider network.

Summary

- Split and single supply amplifiers vary in V_{ICR} and V_O
- Improper signal biasing is a common mistake
- Single supply amplifiers should be biased with a virtual ground
- Selection of a virtual ground depends on key concerns and cost goals

1-30

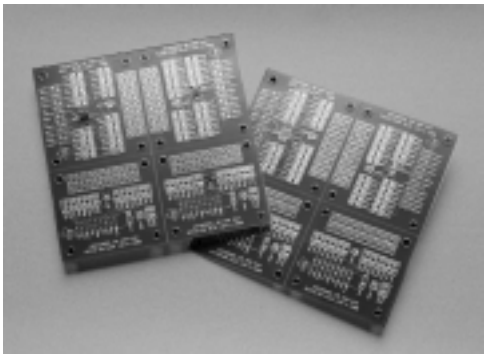
Conclusion

The number of designers migrating from split supply to single supply amplifiers is at an all time high. When using a single supply voltage, the engineer will be introduced to new design issues. In order to be successful designing with these single supply products, a good understanding of V_{ICR} limitations and input signal biasing is critical. Proper selection of a virtual ground is also important. Several examples were presented that cover a majority of single supply applications.

Universal Op Amp EVM

- Quick circuit evaluation with surface mount parts
- Standard circuit elements plus prototyping area.
- 2 Layer ground plane PWB
- 4 Snap-apart areas
- Multiple package types
- Area 100 & 200:
  - Dual op amps
  - SOIC, TSSOP, MSOP
- Area 300 & 400
  - Single op amps
  - SOT23-5

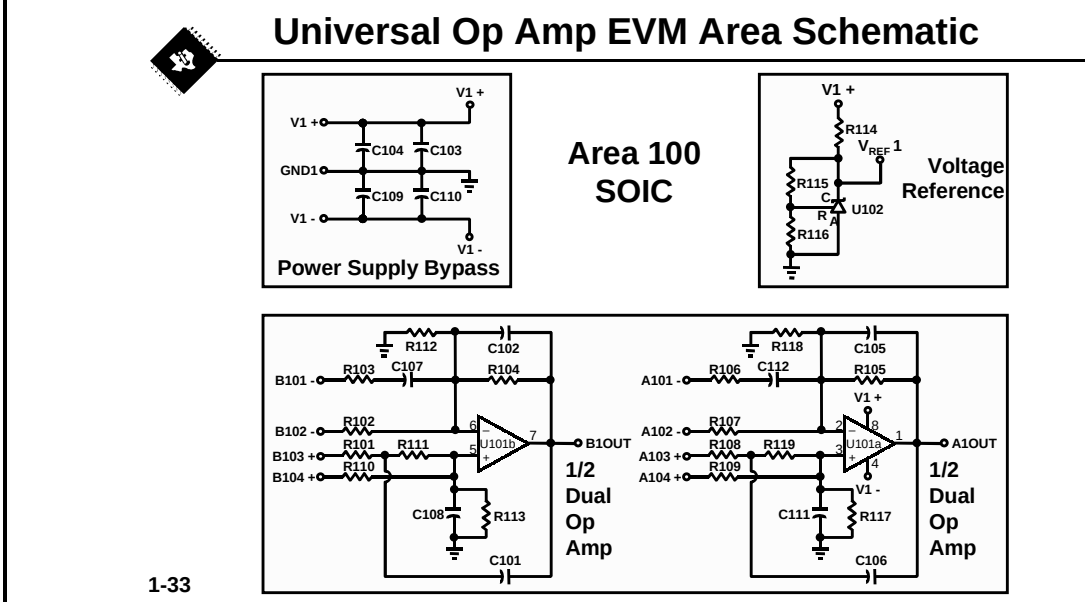
1-32



Universal Op Amp EVM Description

Evaluating applications circuits using operational amplifier normallly requires the use of a breadboard or prototype printed wiring board(PWB). A breadboard quite often does not aproximate real application due to lack of ground planes and proper signal routing. Breadboards do not normally lend themselves to the use of surface mount components. A prototype PWB is often a time and resource consuming effort. The Universal Op Amp Evaluation Module (EVM) is desgined to provide quick easy evaluation of surface mount op amps with excellent signal and noise performance.

The EVM consists of four separate circuits on a snap apart PWB. Each section contains an identical circuit. The sections provide different package layouts to accommodate dual op amps in SOIC, TSSOP and MSOP packages. Single op amps in the SOT23-25 packages are also accomodated.



Universal Op Amp EVM Schematic

The schematic above is for one of the four EVM sections. This is the first section (100). Section 100 accomodates dual op amps and provides connections for standard biasing and feedback resistors. Resistors and capacitors associated with amplifier compensation and filter circuits are also provided. All of the passive components are accomodated in surface mount packaging. Additionally a prototype area with uncommitted PWB pads allows additional circuit configurations. Each section has the same circuit configuration. Sections 100 & 200 have dual circuits. Sections 300 & 400 have single circuits.

A complete application report is available describing the EVM and the implementation of standard amplifier and filter circuits.

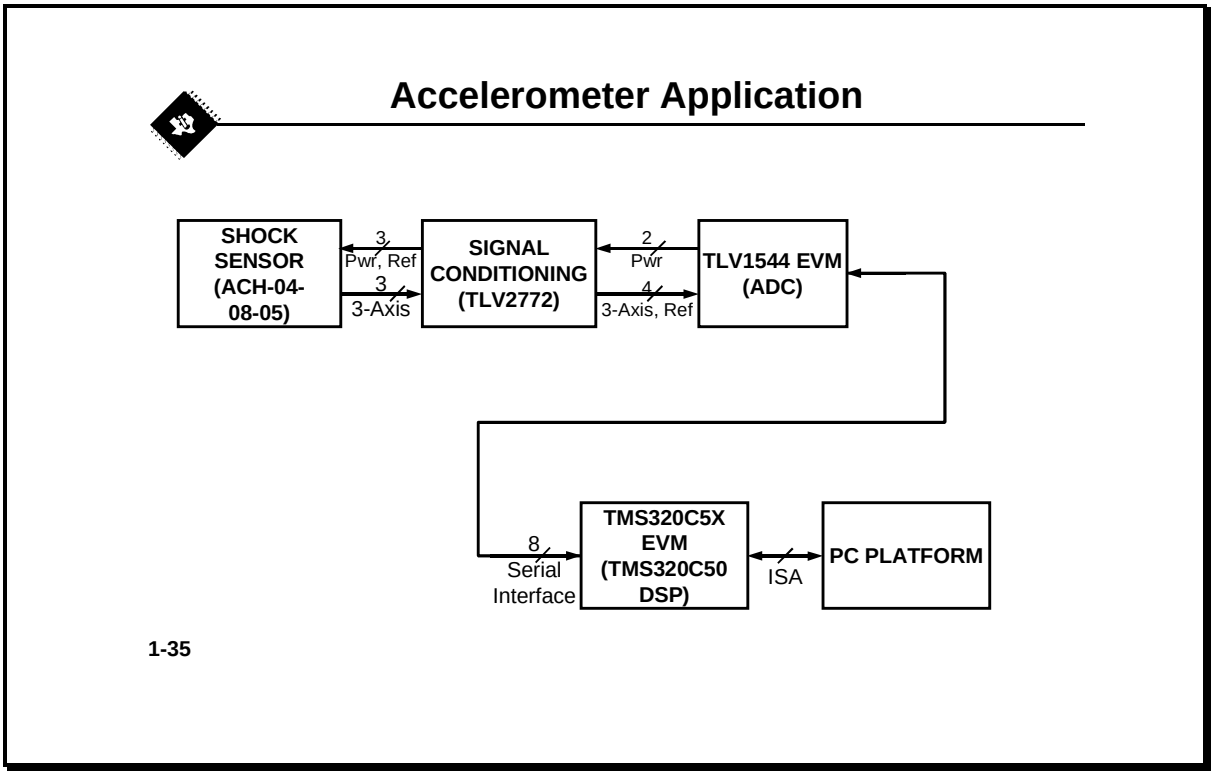
Accelerometer Application

- Typical application example
- Three axis accelerometer circuit
- Constructed & tested using Universal op Amp EVM
- Detailed information published in application report SLVU006

1-34

Universal Op Amp EVM - Accelerometer Application

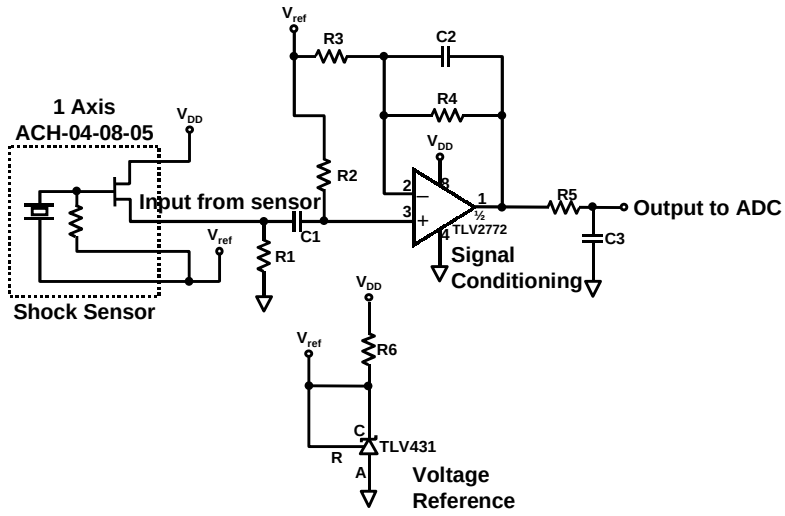
An application circuit interfacing a three axis accelerometer to the input of an analog to digital converter is available. This application report describes a practical implementation of the EVM and the circuit performance. The application report describes a complete system for measuring acceleration in three axis.



Accelerometer System Diagram

The accelerometer system consists of the accelerometer (shock sensor), sensor signal conditioning, analog to digital conversion, digital signal processing and user interface. The system implemented using three EVMs. Two sections of a Universal Op Amp EVM are used for signal conditioning of the sensor output. A TLV1544 EVM provides the analog to digital conversion function. The digital output of the TLV1544 EVM interfaces directly to a TMS320C5X EVM for the Digital Signal Processing function. A PC connects to the DSP EVM and provides user interface.

Accelerometer Schematic



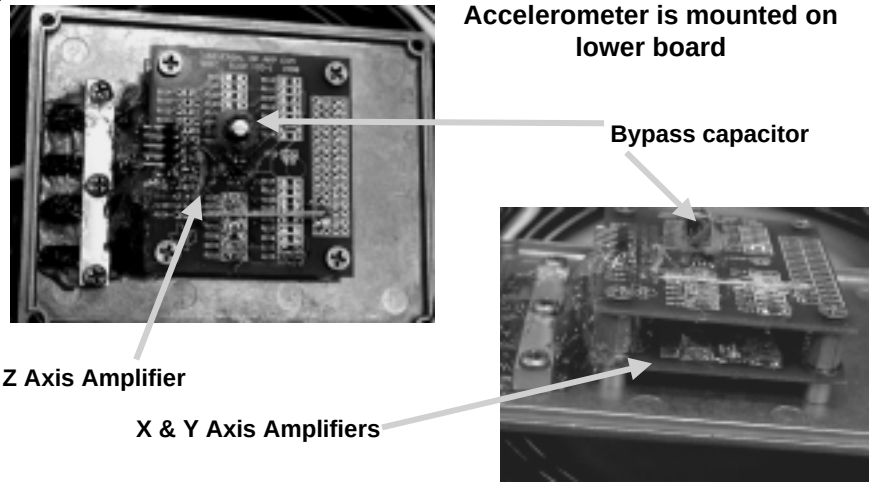
1-36

Sensor Signal Conditioning

The shock sensor consists of accelerometers (X,Y & Z axis) mounted in a single package. The schematic above shows the signal conditioning for one of the sensors outputs. The sensor output signal is from an FET buffer located in the sensor assembly. The signal is amplified and filtered with a single TLV2272 op amp channel using the Universal Op Amp EVM. This is a single supply circuit. The sensor is biased with a virtual ground generated with a TLV431 shunt regulator.

A complete circuit description, software routines, linearity performance and sensitivity data are included in the complete application report.

Op Amp EVM - Accelerometer Circuit



1-37

The illustration above is a photograph of the amplifier circuits consturcted for the accelerometer signal conditioning. The three circuits were built using two Op Amp EVM sections mounted in a sandwitch configuration. The sensor is mounted on the lower board and is not visible. After construction and initial testing clear RTV was applied to the boards prior to runing vibration tests.

High Speed Amplifiers

High speed amplifiers, although similar in basic function to the general purpose op amp, are very different in both performance and application. This section will cover:

What is a high speed amplifier?

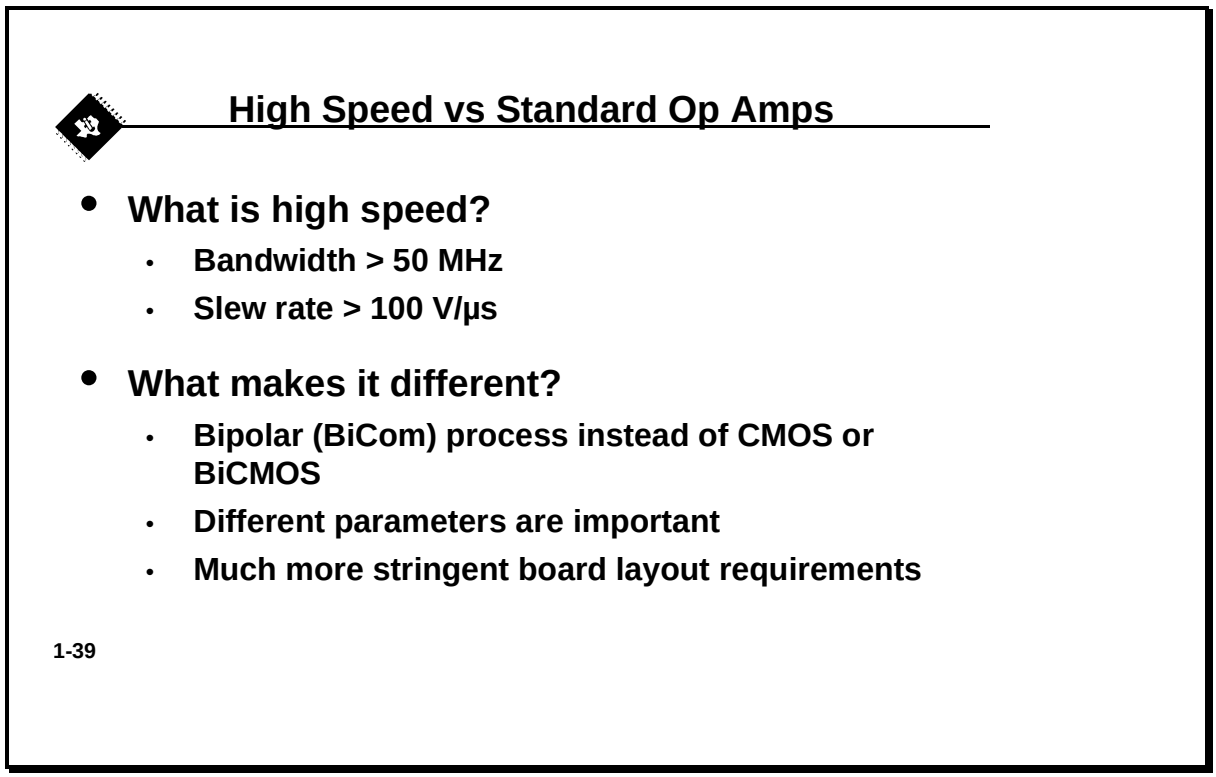
What parameters are important?

What are the two configurations and their advantages?

Several new high speed amplifier products.

A high speed amplifier application in a data acquisition system.

When someone says to you, “I need an op-amp” what do you think of? If your like most people, you think of classic op-amp. But what if you needed to amplify a video signal or receive a communications signal? These classic op-amps will not suffice. This presentation will serve to focus your attention on the next generation of operational amplifiers - High Speed.



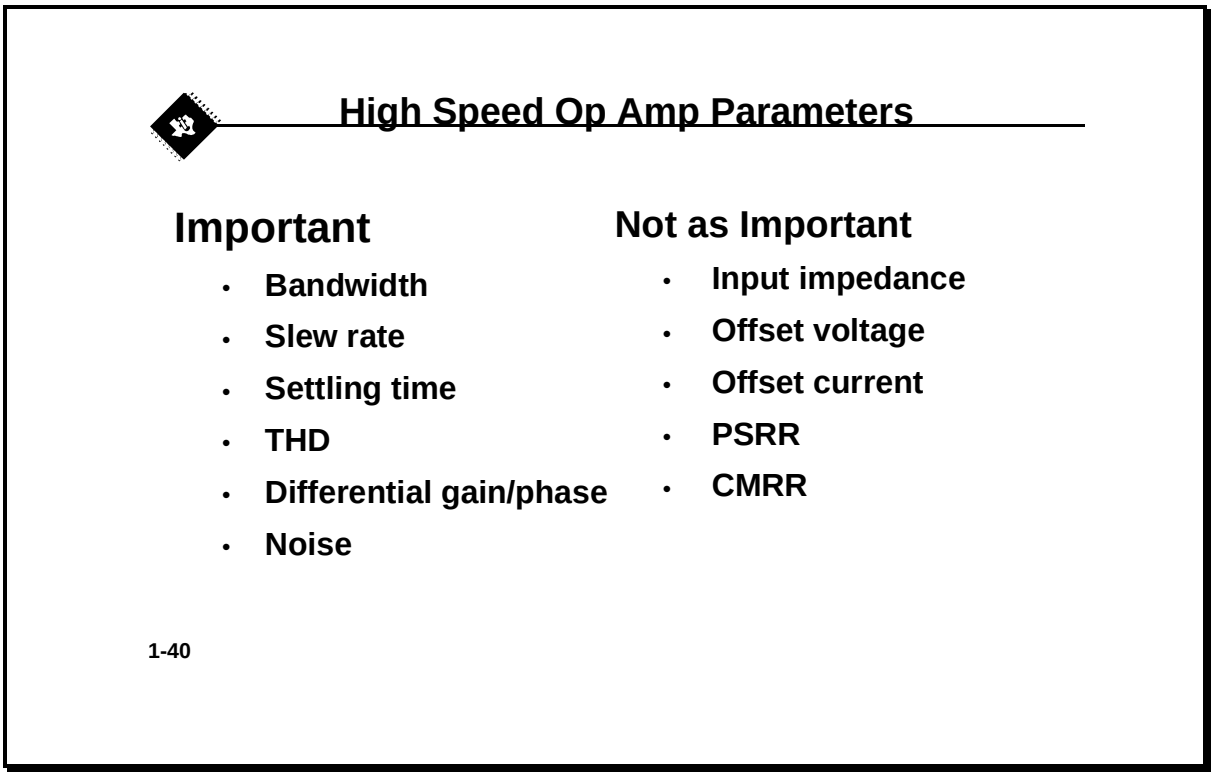
What is a high speed amplifier?

In the operational amplifier market, High Speed is generally defined as having a bandwidth of 50 MHz or greater and a slew rate of at least 100 V/uS. CMOS or BiCMOS is typically limited to 15 MHz and below. These processes are not fast enough to fit into this High Speed category.

Welcome to the world of the BiCOM process (Bi-polar complementary). BiCOM-I is a 30-Volt process which incorporates transistors that have a f_{max} of several GHz. This is the backbone of the High Speed Amplifier line at Texas Instruments.

Because the frequencies of interest start at 50 MHz, PCB requirements have to change. We have to worry about line impedance matching, reflections, stray capacitance, and lead inductance. This requires a new way of thinking when laying out a circuit. This presentation is not intended to clarify all of these issues, but it is still an important change from the classic op-amp of yesterday.

Now that we have all of this speed, there are going to be a few changes in the way we classify an op-amp. The parameters carry over from the classic op-amp, but the order of importance is changed.



What parameters are important?

The most important parameter of a High Speed Op-amp is the bandwidth. This is typically the -3dB point of the output signal and is the first step in classifying the device.

The slew rate is the next most important parameter. This tells us how fast the output can change within a given amount of time. The typical units are Volts per micro-second, with high-speed stipulating a minimum of 100 V/uS.

The settling time can also be a very important factor in sampling systems. This lets you know when the output has settled to within 0.1% or 0.01% of the final value. The most obvious use for this knowledge is in Analog-To-Digital converters.

Passing a pure signal through an amplifier without any distortion is almost always an important parameter. There are several things which influence distortion. These are: current out of the op-amp, frequency, amplitude, and whether the system is a single-ended or differential output. The differential output system will generally minimize the second-order harmonics of the amplifier and causes the thrid-order harmonics to dominate.

In conjunction with distortion, differential gain and differential phase come into play. This is generally utilized for video systems (such as NTSC or PAL).

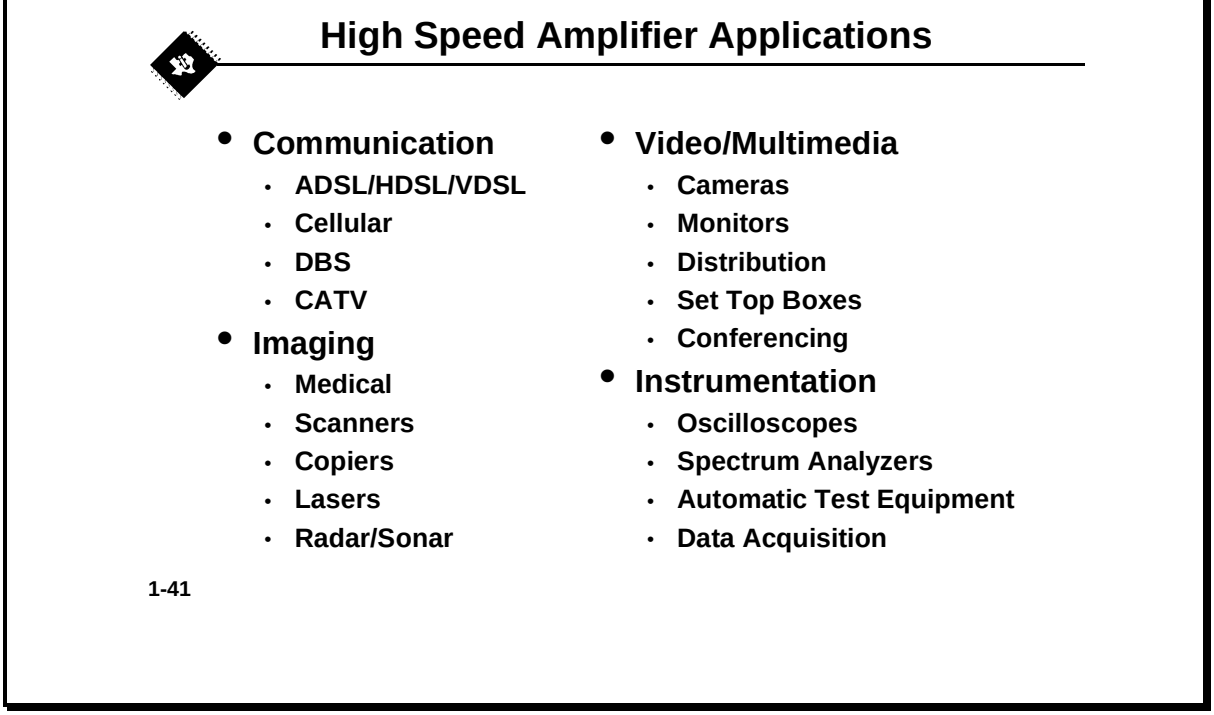
One final important parameter to high-speed amplifiers is the internal noise. This is especially important for receiving very small signals from an antenna or sensor. In-order to maximize the Signal-To-Noise Ratio (SNR), this receiver amplifier has to have a low internal noise source in conjunction with a high gain.

Typically, the input impedance is not important for high-speed systems. This is because most high-speed systems use either 50-ohm or 75-ohm termination resistors. This is done to reduce reflections over a transmission line.

Most high-speed systems AC couple the signals by utilizing a DC blocking capacitor. Obviously then, the input offset voltage and input offset currents are not very important parameters.

When dealing with signals over 10 MHz, EMI radiation typically occurs. Coupled with the fact that bypass capacitors have a limited frequency usefulness and trace inductance, it is easy to see why the Power Supply Rejection Ratio (PSRR) of the op-amp is not a very important factor. This typically has to be controlled external to the device and can involve some serious trial and error to find a proper solution.

Finally, Common Mode Rejection Ratio (CMRR) is not a very important parameter. This is due to the fact that most interference signals within a deferential system do not require a CMRR greater than 60dB (1000 to 1 SNR).



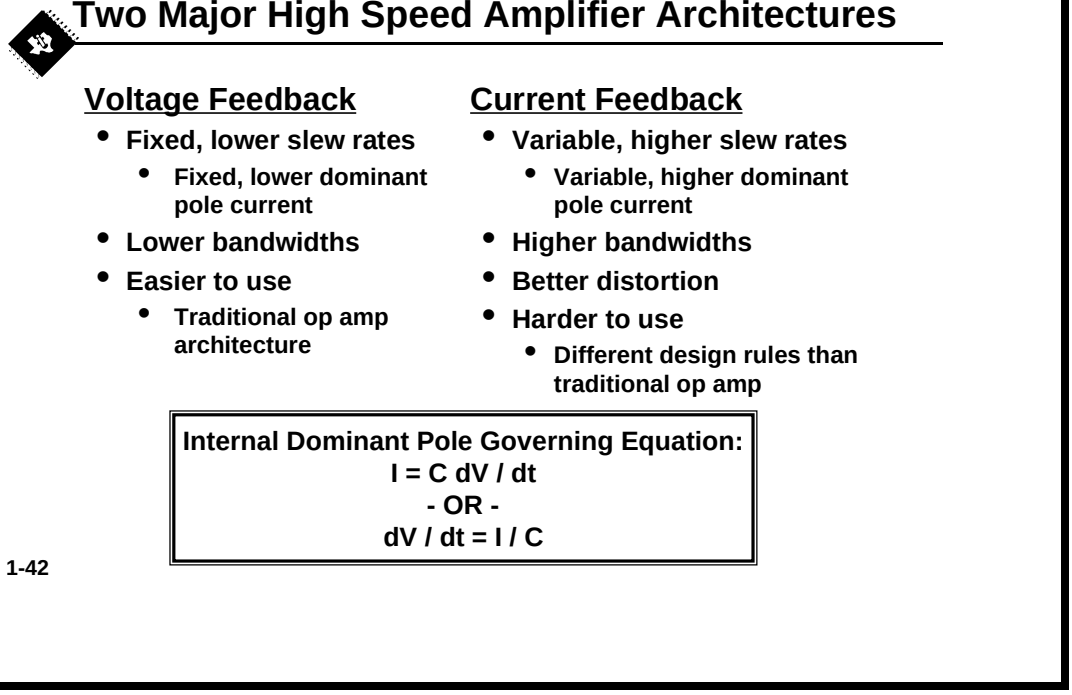
Where do you use high speed amplifiers?

So where do you find High Speed Amplifiers? They are found everywhere. Some are obvious, such as within video equipment and communication systems. Others or not so obvious and rather obscure. This can include things such as the front end of an oscilloscope or within imaging systems.

The list shows a partial list of where High-Speed amplifiers can be found. This is by no means a complete list, but it should get you thinking about where high speed amplifiers are found.

As you can see in the list, one of the areas of interest is ADSL, HDSL, and VDSL communications. High Speed amplifiers are generally used within the line interface of these systems. Texas Instruments has a whole line dedicated to these systems and it is beyond the scope of this discussion. For more information about this, please talk with the High Speed Marketing representative listed at the end of this presentation.

Now that we have discussed some general parameters of high speed amplifiers and where to find them, let's look a little closer at the op-amp itself.



Amplifier Architectures

The first thing you will notice when you dive into this field is that there are actually two main types of High Speed amplifiers. This includes the Voltage Feedback amplifier (VFB), which includes 99.9% of the classic amplifiers, and the Current Feedback amplifier (CFB). For most people, this CFB amplifier is a brand new concept and most people shy away from it, but it is not that bad. In fact, the CFB amplifier was actually one of the first amplifiers ever to be created. Ease of use and lack of applications caused the architecture to be left behind in the dust.

So why do we need it now? To answer this we need to recall what the definition of high speed was … a bandwidth greater than 50 MHz and a slew rate of greater than 100 V/uS. VFB amplifiers can do pretty well, especially with new technology and processes, but there are internal limits based on the architecture alone.

Because the inputs of a VFB amplifier are high impedance, the internal compensation capacitor (a.k.a the dominant pole) has to be charged and discharged by the internal bias currents which are fixed. Utilizing physics, the fastest slew rate is governed by the following equation:

$$I = C\, dV/dt$$

Knowing that C and I are internal and fixed and solving for the slew rate we get:

$$dV/dt = I / C$$

This is fixed and real values show a typical slew rate of 200 to 1000 V/uS. Obviously there are other factors which influence slew rate, but this is probably one of the most important aspects. The slew rate of a voltage feedback amplifier will work for a lot of applications, but not all of them.

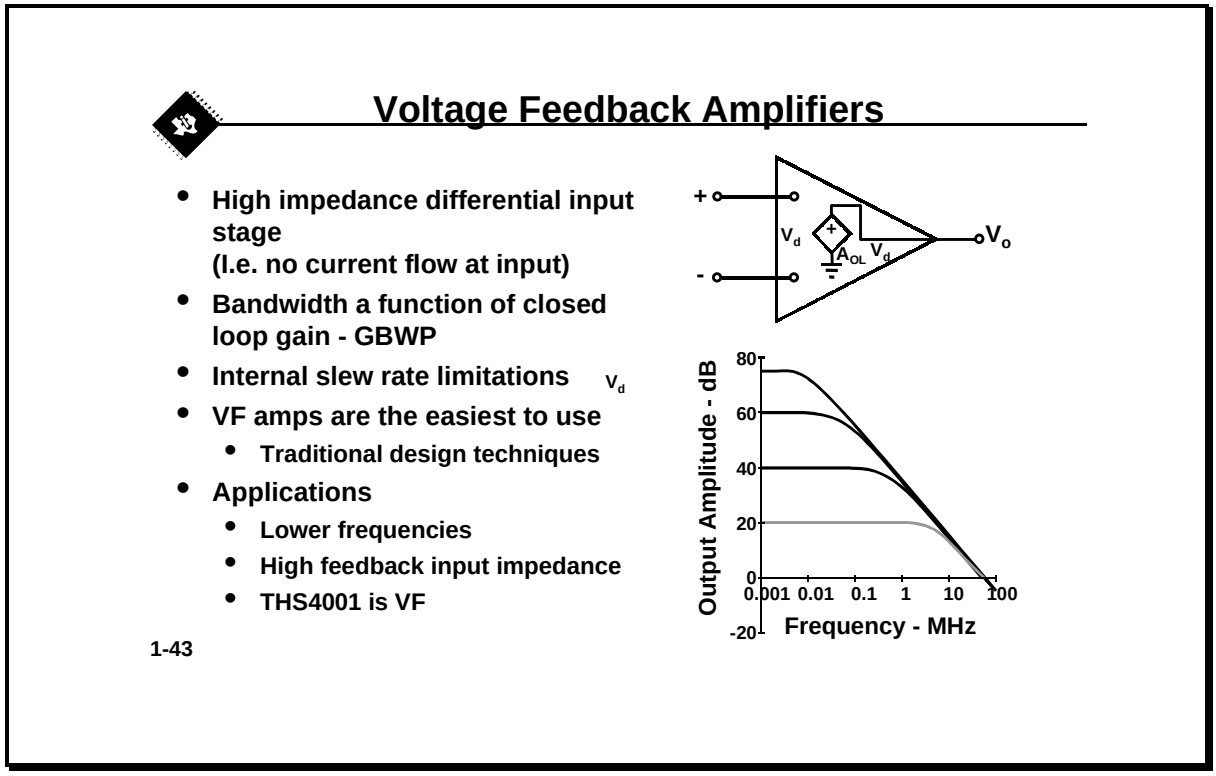
Current Feedback Amplifiers, on the other hand, utilize a low impedance input front-end. It uses the feedback current to charge and discharge the internal compensation capacitor. Thus, the limitation of a fixed charge current is eliminated and the slew rate can be greatly enhanced. In fact, the slew rate is directly proportional to the amplifier output voltage swing and inversely proportional to the feedback resistor.

Because bandwidth is set by the same internal capacitor, bandwidth is generally based on the same principles as stated above. Thus, VFB amps generally have lower bandwidths than CFB amps.

With a higher slew rate and a higher bandwidth, CFB amplifiers generally have an advantage when it comes to distortion. This is due to the fact that they can respond quicker to any non-linearities within their own architecture, thus eliminating distortion.

So why not use a current feedback amplifier all of the time? The problem is that a CFB amp uses the feedback current to charge and discharge the dominant pole capacitor. If you allow too much current to flow into the feedback, the dominant pole frequency gets shifted to a much higher frequency than it was designed for. This will cause the output to overshoot and eventually oscillate. Thus, you cannot use a CFB amplifier as a pure buffer with the output shorted to the inverting node. In addition, you cannot have a capacitor directly in this feedback path. The capacitor's impedance will become very small at it's resonant frequency and the op-amp **will** oscillate.

Now that we understand the concepts behind the two architectures, let's look at each one in more detail individually.



Voltage feedback

First, let's talk about the classic voltage feedback amplifier. The voltage feedback amplifier (VFB) has a high impedance input stage. The amplifier first looks at the difference in voltage (V_d) at the inverting and non-inverting terminals. The output then multiplies the difference (V_c) by the open loop gain (A_{OL}). With negative feedback from the output to the inverting node, we get a closed loop amplifier.

One of the main characteristics of a VFB amplifier is the bandwidth is indirectly related to the gain. As the gain is increased, the bandwidth is divided by the gain. This is known as Gain Bandwidth Product - or GBWP.

For example, if we look at the graph on the lower right corner, it shows a -3dB bandwidth of about 100 MHz at a gain of one. If we set the gain to 40 dB, or 100, then the bandwidth is divided by 100, or 100Mhz / 100 = 1 MHz.

As stated previously, the VFB amplifier does have internal slew rate limitations based on it's architecture. Because of this, VFB amps are generally used in lower bandwidth systems. And because it has high input impedances, the VFB amplifier is extremely easy to use. Making an integrator or a simple buffer is no problem with a VFB op-amp. This is because the op-amp does not rely on the current flowing into or out of the input stage.

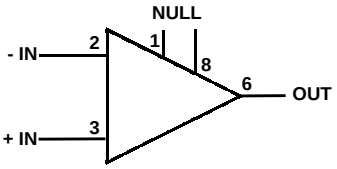
Now that we know what a voltage feedback amplifier is, let's take a look at Texas Instruments first amplifier, the THS4001.

THS4001 High Speed Voltage Feedback Amplifier

- **Very High Speed**
  - 300 MHz Bandwidth (Gain = 1, -3dB)
  - 400 V/µs Slew Rate
  - 30-ns Settling Time (0.1%)
- **High Output Drive**
  - I_o = 100mA
- **Very Low Distortion**
  - THD = -72 dBc @ 1 MHz
- **Gain & Phase Accuracy**
  - Differential Gain Error = .04%
  - Differential Phase Error = .15°
- **Evaluation Modules Available**

Fastest 30-V Voltage Feedback Amplifier on the Market.

THS4001



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The THS4001 is a 300 MHz, 400 V/uS voltage feedback amplifier. This is the world's fastest 30-Volt voltage feedback amplifier on the market today. Coupled with a 30 ns 0.1% settling time, the THS4001 can make an excellent front-end amplifier in an Analog-to-Digital converter system.

The high output current drive of 100 mA makes this a very versatile op-amp. It can be used to drive heavy loads or termination lines at full output voltages.

Another key aspect of the THS4001 is it's distortion. It has a Total Harmonic Distortion (THD) of -72dBc at 1MHz. This is a very respectable number for this class of amplifier and can be utilized to ensure signal integrity.

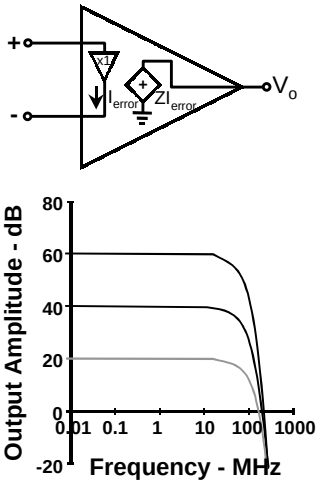
This brings up the next feature of the THS4001, a strong video specification. It has a differential gain error of 0.04% and a differential phase error of 0.15 degrees. What this means is that when a NTSC or PAL carrier frequency is DC shifted from 0 volts to 0.7 Volts (or 100 IRE), the gain and phase of the carrier is changed by the aforementioned specifications. Again, these are very respectable numbers. In fact, customer feedback has shown that coupled with the high output drive of this amplifier, differential gain and phase remain fairly constant when going from one distribution line (150 ohm load) to two distribution lines (75 ohm load).

This is all fine and dandy, but most designers hate to create a high speed test board with surface mount op-amps. To circumvent this, TI has created an Evaluation Module (EVM) for the THS4001. This is a pre-built, tested circuit which allows a designer to evaluate the THS4001 within minutes of receiving the EVM.

That concludes the voltage feedback portfolio, but we still need to discuss the current feedback system. So, let us first look at some key features of the current feedback amplifier in greater detail.

Current Feedback Amplifiers

- Much higher slew rates
- Unity Gain Buffer Input Stage
  - + input has high impedance
  - - has low impedance (i.e. current flow)
- Internal transimpedance stage
- Much higher slew rates
- Bandwidth 'independent' of gain
- Harder to use
  - *Must* have feedback resistor
  - *NO* capacitor in feedback path
- Applications
  - ADSL, HDSL, VDSL
  - THS3001 and THS6002 are CF



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Current feedback

The first thing you will notice is that the input stage is quite different. The non-inverting input has a high input impedance, just like the VFB amplifier. But the inverting stage is low impedance, typically less than 20 ohms. This means that current **will** flow into this pin. The output will then multiply the error current (I_{error}) by the open loop transimpedance (Z). With a feedback resistor placed between the output and the inverting pin, we form a closed loop system.

The first thing you will notice is that the feedback resistor limits the amount of current flow into or out of the inverting pin. And because bandwidth is determined by the amount of current available to charge the internal compensation capacitor, the feedback resistance plays the key role in determining the bandwidth of the system. Typically, as the feedback resistor is increased, the bandwidth will be decreased.

Additionally, the slew rate will also be affected by this same concept. To find out exactly what the feedback current will be, we get the following equation:

$$I_{FEEDBACK} = (V_{OUT} - V_{INVERTING\ NODE}) / R_{FEEDBACK}$$

Remember that the slew rate is determined by the current available to charge the internal dominant pole capacitor. Thus, the slew rate is determined by the output swing and the feedback current into the inverting node.

The last key feature of this system can be seen in the frequency response graph of a typical current feedback amplifier. There is not a gain bandwidth product like there is in a VFB amplifier. Thus, once you get an acceptable response out of a CFB amplifier, you simple need to change the gain resistor to change the overall system amplification, not the feedback resistor. Again, the feedback resistor controls the response of the CFB amplifier.

As stated before, the drawback to the CFB amplifier is the fact that it can be harder to use. But, careful planning will make this amplifier as easy to use as the VFB amplifier. So, if you need an extremely high slew rate, gain independent, high bandwidth amplifier, the CFB amplifier makes a logical choice.

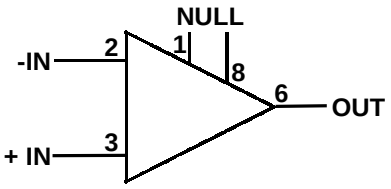
Now that we better understand what a current feedback amplifier is, let's take a look at Texas Instruments first CFB amplifier, the THS3001.

THS3001 High-Speed Current Feedback Amplifier

- Very High Speed
  - 420 MHz Bandwidth (Gain = 1, -3dB)
  - 6500 V/µs Slew Rate
  - 40-ns Settling Time (0.1%)
- High Output Drive
  - I_o = 100mA
- Very Low Distortion
  - THD = -96 dBc @ 1 MHz
- Gain & Phase Accuracy
  - 115 MHz -0.1dB BW (Gain = 2)
  - Differential Gain Error = .01%
  - Differential Phase Error = .02°
- Evaluation Modules Available

Fastest 30-V Current Feedback Amplifier on the Market.

THS3001



1-46

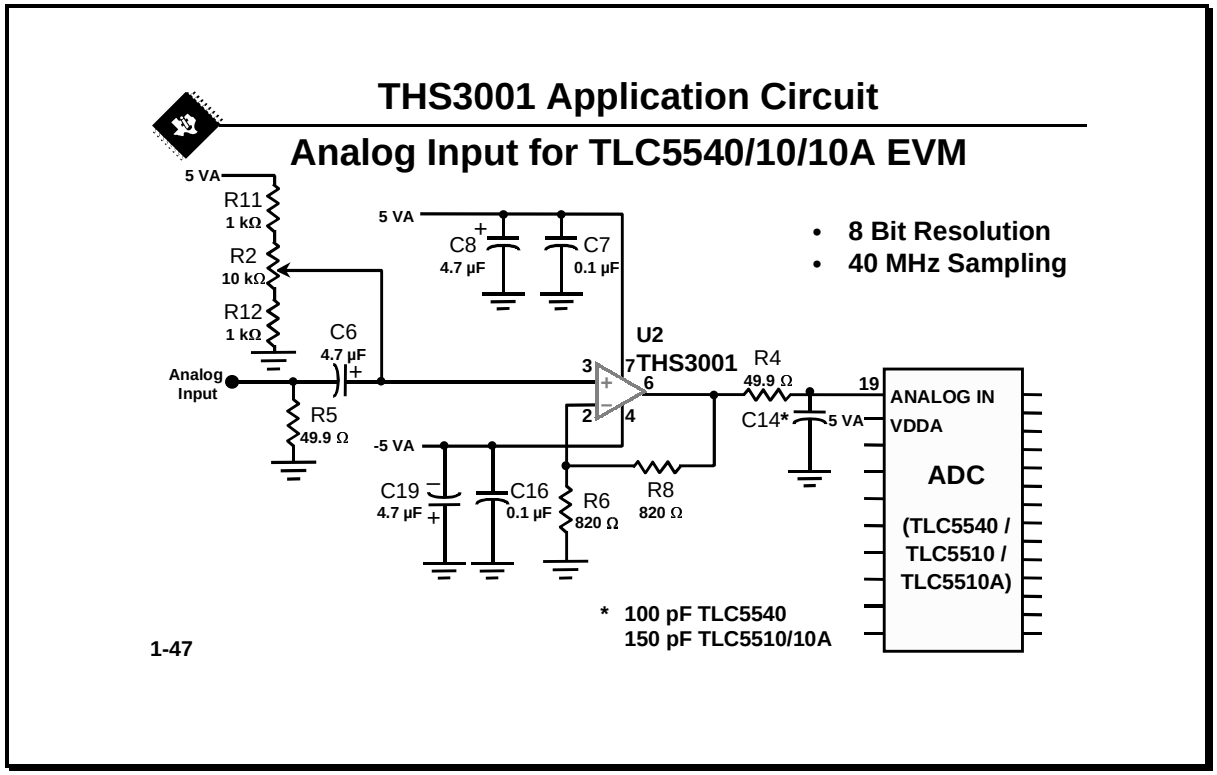
The THS3001 is a 420 MHz, 6500 V/uS current feedback amplifier. This is the world's fastest 30-Volt current feedback amplifier on the market today. Coupled with a 40 nSec 0.1% settling time, the THS3001 can make an excellent front-end amplifier in an Analog-to-Digital converter system.

Another key aspect of the THS3001 is it's distortion. It has a Total Harmonic Distortion (THD) of -96dBc at 1MHz. This is an extremely good distortion specification and can be utilized to ensure signal integrity. Not many amplifiers on the market today can boast such a good specification.

This low distortion brings up the next feature of the THS3001, the video specifications. It has a differential gain error of 0.01% and a differential phase error of 0.02 degrees. Additionally, the THS3001 has a -0.1dB bandwidth of 115 MHz with a gain of 2, which is what most video systems are utilizing. Again,

these are extremely good numbers. Coupled with an output current drive of 100 mA, the THS3001 can be used to drive multiple transmission lines with very little signal degradation.

Just like the THS4001, the THS3001 has an Evaluation Module (EVM) available. This is also a pre-built, tested circuit which allows a designer to evaluate the THS3001 in gains of +2 or -1. This simple EVM will allow the designer to quickly evaluate the THS3001 with very little effort.



High Speed Amplifier Application

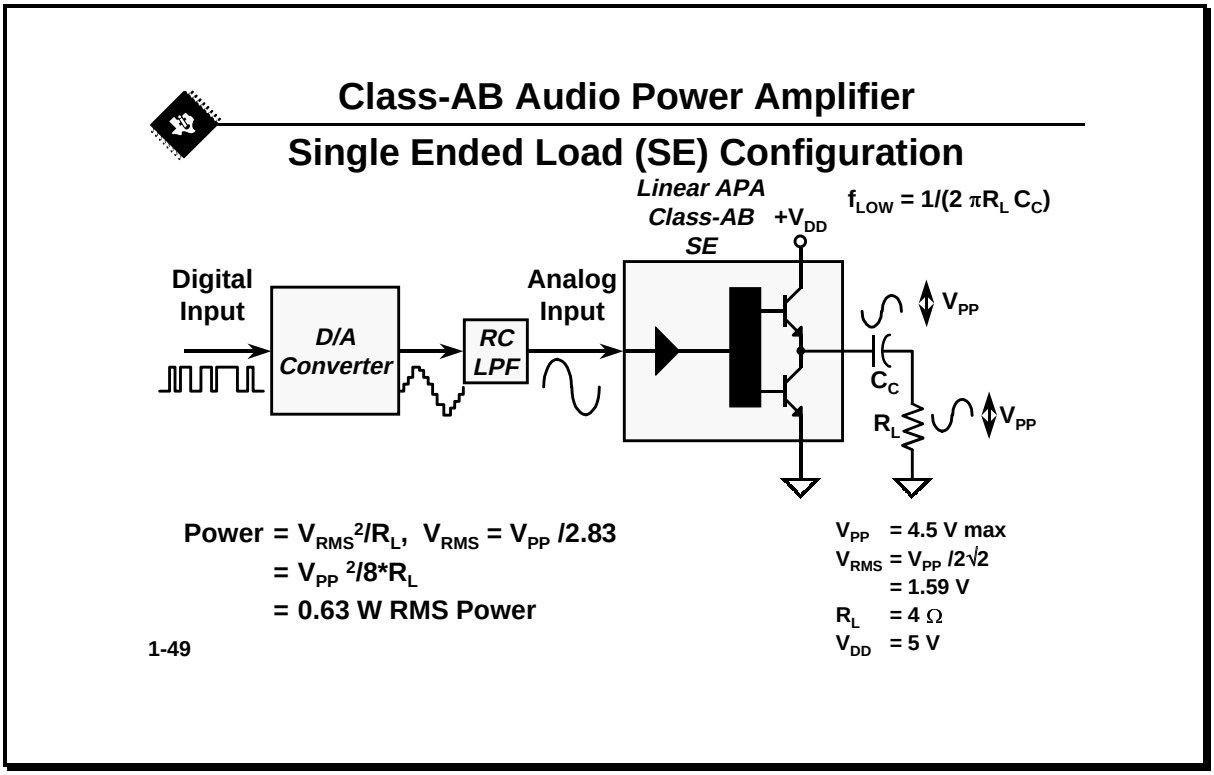
Here you can see the front-end of an analog - to - digital converter (ADC). This particular converter requires a single supply and thus the input signal must also be uni-polar. To create this, the THS3001 is DC shifted to the mid-rail, creating a virtual ground to the ADC input. A signal is then AC coupled into the THS3001. The THS3001 will then amplify the DC bias and AC input signal by two. To help eliminate any glitches, a simple low pass filter is placed between the THS3001 and the ADC. This also helps in isolating the capacitive load placed on the THS3001. Without the 49.9 ohm resistor (R4) the THS3001, with just about every other high speed amplifier, will have a tendency to oscillate.

Some general rules should be discussed at this point. The first is that proper power supply bypassing must be used with a high speed amplifier. This is done by placing bulk capacitors C8 and C19 on the power supply busses. Additionally, high frequency capacitors, such as the 0.1uF capacitors used above, should be placed as close as possible to the amplifier's power input pins. This will help supply the high-frequency currents required by the amplifier. Failure to do so will result in ringing or an increase in distortion.

One final rule which is **very** important is that the inverting node trace of the high speed amplifier must be as short as possible. This will help minimize any stray capacitance at this node. Additionally, removing a ground plane underneath this trace will also help decrease the stray capacitance. Failure to do so will cause peaking to occur in the frequency response. This will create an unstable system which will have a tendency to overshoot and possibly oscillate.

There are numerous other high frequency design rules which should be adhered to, but they are beyond the scope of this presentation. More information can be found within the application sections of the THS datasheets.

Audio Power Amplifiers



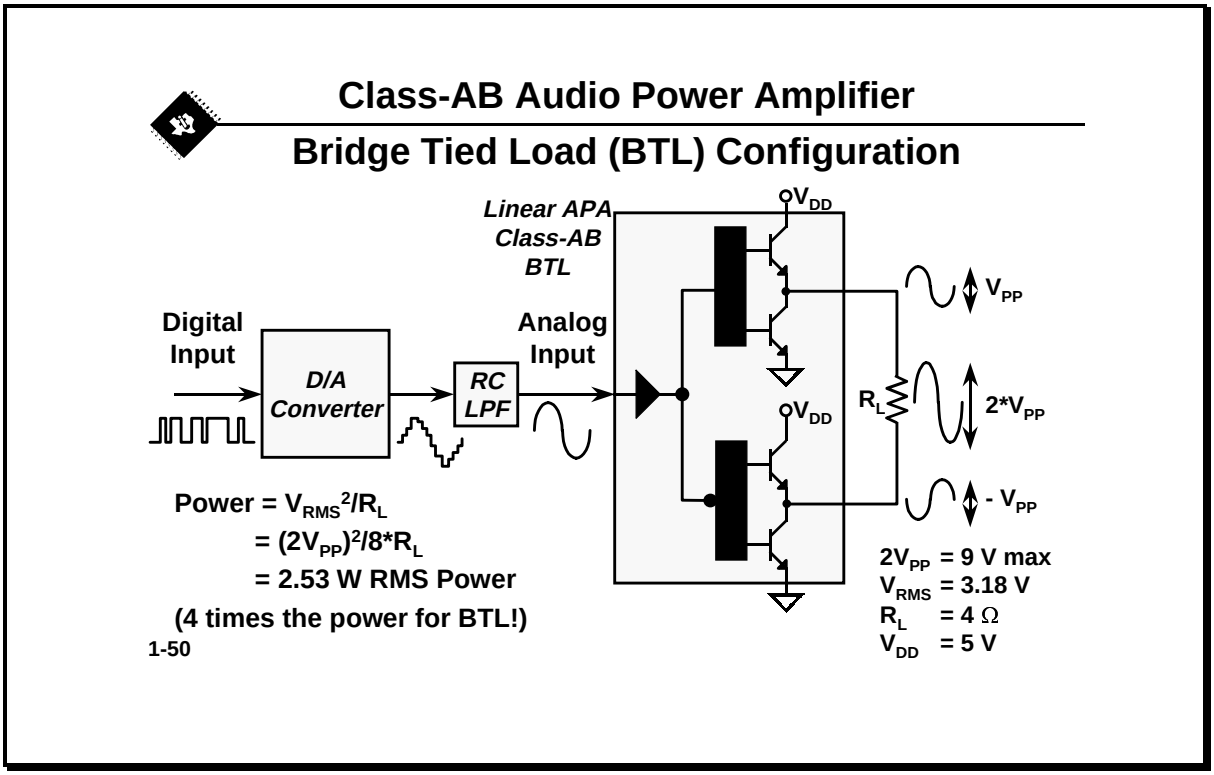
Class-AB With Single Ended Load (SE) Configuration

Audio Power Amplifiers (APA) are a special type of Operational Amplifier optimized to drive low impedance loads, typically speakers or headphones, at frequencies from 20 to 20 kHz. In the diagram you see a representation of a typical computer audio output channel employing the most common type of APA, the Class AB linear amplifier. From the title, you can see that we call it Single Ended; this refers to the fact that the amplifier drives only one end of the load while the other end is typically connected to ground.

In the diagram, the D/A Converter accepts digital sound data from the Sound Chip, or other source, and converts it into a linear representation of the original sound waveform. The RC Low Pass Filter removes conversion noise from the D/A output and provides an analog waveform to the APA.

In terms of power provided to the load, the equation is straight forward if you remember to convert the Voltage to an RMS value by dividing the peak to peak number by 2*(2)^1/2 or 2.83. Then it is just Vrms squared divided by R. Also remember, that when determining the peak power capability of an amplifier, that most APAs can not approach the supply rails or distortion is significantly increased (Clipping). So, for a +5 volt supply into a 4 ohm speaker we get about 4.5 Volt maximum peak to peak swing which translates into 1.59 volts RMS (quite a difference in peak vs rms power if you happen to forget to make the conversion). Plugging the numbers into the equation you get 0.63 Watts of RMS power into a 4 ohm load from a +5 Volt power supply. If you change the speaker to an 8 ohm type then you get half the power -- down to 0.32 Watts whereas if you change the load to 2 ohms then you could expect 1.26 Watts of power into the load. Not all amplifiers, however, can handle 2, 4 or 8 ohm loads -- be sure to check the specifications of the candidate devices.

Another way of providing more power into the load rather than lowering the impedance of the speaker is a technique called “bridging.”



Class-AB With Bridge Tied Load (BTL) Configuration

In this diagram we see a linear APA in a Bridge Tied Load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load differentially. There are several potential benefits to this configuration but, for now, let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the available voltage swing on the load. When you the plug twice the voltage into the power equation, where voltage is squared, then you get 4 times the output power from the same supply rail and load impedance.

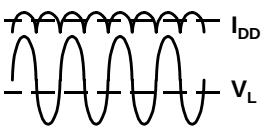
In a typical computer sound channel running from 5 volts supplies, bridging raises the power into a 4 ohm speaker from .63 watts to 2.5 Watts. In sound power, that is a 6 dB improvement - which is loudness you can really hear. Other advantages are there also. In the single supply SE configuration a coupling capacitor is required to block the DC offset from reaching the load (unless you are using bipolar supplies). These capacitors can be quite large (in the neighborhood of 40 to 1000 uF) so, are expensive and have the additional drawback of limiting low frequency performance. This limiting effect happens due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with the equation FL = 1 divided by 2 pi RC. For example, a 120 uF cap with a 4 ohm speaker would attenuate low frequencies below 330 Hz -- no bass drums in that output! The BTL configuration cancels the DC offsets which eliminates the need for the blocking

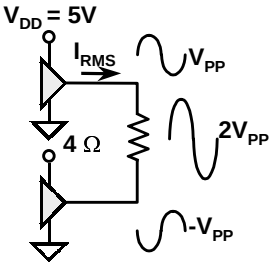
caps. Low frequency performance is then limited only by the input network and speaker response.

BTL does carry a penalty though and that penalty is increased internal power dissipation - up by a factor of four over SE configurations of the same supply voltage. In the next slide we will investigate power dissipation of linear amps in greater detail by looking at the issue of amplifier efficiency.

Class-AB Amplifier Efficiency

BTL Waveforms





Linear BTL Amplifier (Class AB)

Eff. = P_L /P_{SUP}

(....after many many steps....)

$Eff._{BTL}$ = πV_P / $2V_{DD}$ = π $(P_L R_L /2)^{1/2}$/ $2V_{DD}$

= 22 % @ P_L = .25 W, P_{dis} = 0.89 W

= 31 % @ P_L = .5 W, P_{dis} = 1.11 W

= 44 % @ P_L = 1 W, P_{dis} = 1.27 W

= 63 % @ P_L = 2 W, P_{dis} = 1.17 W

= 70 % @ P_L = 2.5 W, P_{dis} = 1.07 W

1-51

Class-AB Amplifier Efficiency

Linear amplifiers are notoriously inefficient. The primary cause of inefficiency in a linear amplifier is the voltage drop across the output stage transistors. The drop occurs for two reasons, one is that even at maximum output swing from a 5 volt supply we said the output voltage would only swing 4.5 volts and the other is due to the sinewave nature of the output waveform. The equation to calculate efficiency starts out simply enough as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the rms values of power in the load, and in the amplifier, you must understand the shapes of the current and voltage wave forms as shown above. Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full wave rectified, this means rms conversion factors are different. Examination of the transistor block diagrams in the previous slide will help clarify the point, keeping in mind that for most of the waveform both the push and pull transistor are not on at the same time.

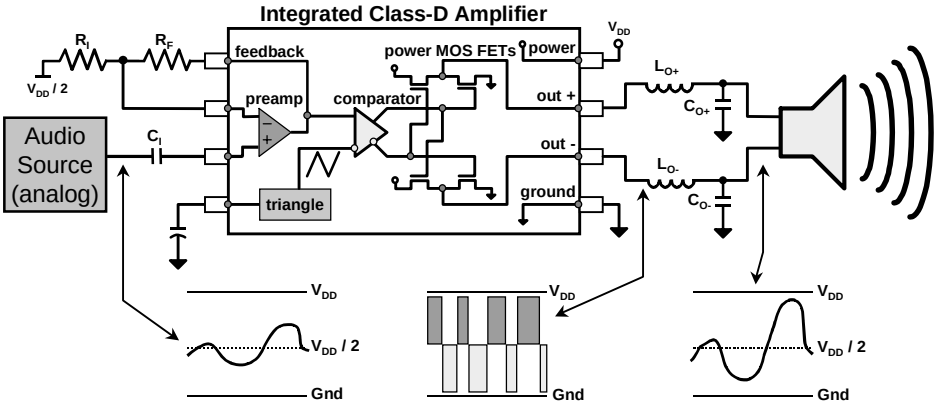
What we see from the example calculations is that the efficiency is quite horrible for lower power levels resulting in a nearly flat internal power dissipation over the normal operating range. What is a little surprising at first is the fact that the internal dissipation at full output power is less than in the half power range. Try using that as an explanation to a neighbor next time they complain about your loud music. "Sorry man, just trying to reduce the power dissipation in my amplifiers." Also remember that the above example is mono - double everything for stereo! So, for a stereo 2.5 W audio system with a 4 ohm load and 5 V supply the maximum draw on the power supply will be almost 7.25W. Also, this equation only works for pure sine waves, and not too many real people listen to sine waves (we at TI do but we are strange characters for the most part).

A final "all is not lost" point to remember about linear amplifiers, whether they be SE or BTL configured, is how to manipulate the terms in the efficiency equation to your advantage when possible. Note that in the efficiency equation V_{CC} is in the denominator. This means that as V_{CC} goes down, efficiency goes up. Consider this example, if you replaced the 5 V supply with a 12 V supply in the above calculations, then efficiency at 2.5 W would fall to 29% and internal power dissipation would rise to 6.12 W. Use the right supply voltage and speaker impedance for your application - over kill will kill you over and over!

All this poor efficiency is exactly what drove TI to develop a different type of amplifier - Class-D.

Integrated Class-D Power Amplifier

Analog Input



1-52

Integrated Class-D Power Amplifier

Class-D amplifiers are switch-mode power delivery circuits much like switch-mode voltage regulators. Where regulators have a DC reference that sets the output voltage Class-D amplifiers use the audio input signal as the reference and therefore the output follows the input signal. Being similar to switch-mode power supplies much of the theory of how switch-mode power supplies operate applies directly to Class-D amplifiers. This is helpful since there is not a wealth of information available on Class-D - yet!

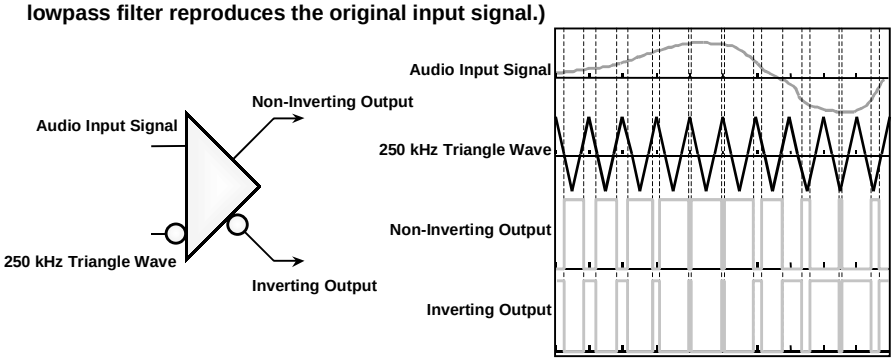
In the diagram above above you see one implementation of an integrated Class-D amplifier. The word “integrated” is important. Discrete implementations of Class-D have been around for many years but until recently the technology required to place the sensitive analog circuitry on the same piece of silicon with a high Power FET was not available.

Class-D relies on a technique called Pulse Width Modulation (PWM) to sample the input and then recreate the Audio Signal at the load. PWM resemble digital data in that is has an on state and an off state. This is the key to efficiency - when the FET is on, it has a low resistance and therefore delivers power efficiently. When it is off it delivers no powers and so there is no loss. So, the Class-D amplifier turns on for a period of time (a pulse width) that is determined by the level of the input signal, grabs an efficient pulse of power, and then delivers it to the load. An output filter then smoothes these pulses of power back into a time linear signal before it gets to the speaker.

Recap - The integrated Class-D amplifier samples the input waveform and creates discrete time pulses that represent the level of the signal. The pulses are then used to modulate the power FETs on and off to take efficient pulses of power from the supply and deliver them to the load. The output filter then smoothes the output back into a time linear waveform.

Basic PWM Generator

Where the triangle crosses the input signal the comparator switches, creating a PWM waveform of the input signal at the frequency of the triangle wave. **(Passing the PWM waveform through a lowpass filter reproduces the original input signal.)**



1-53

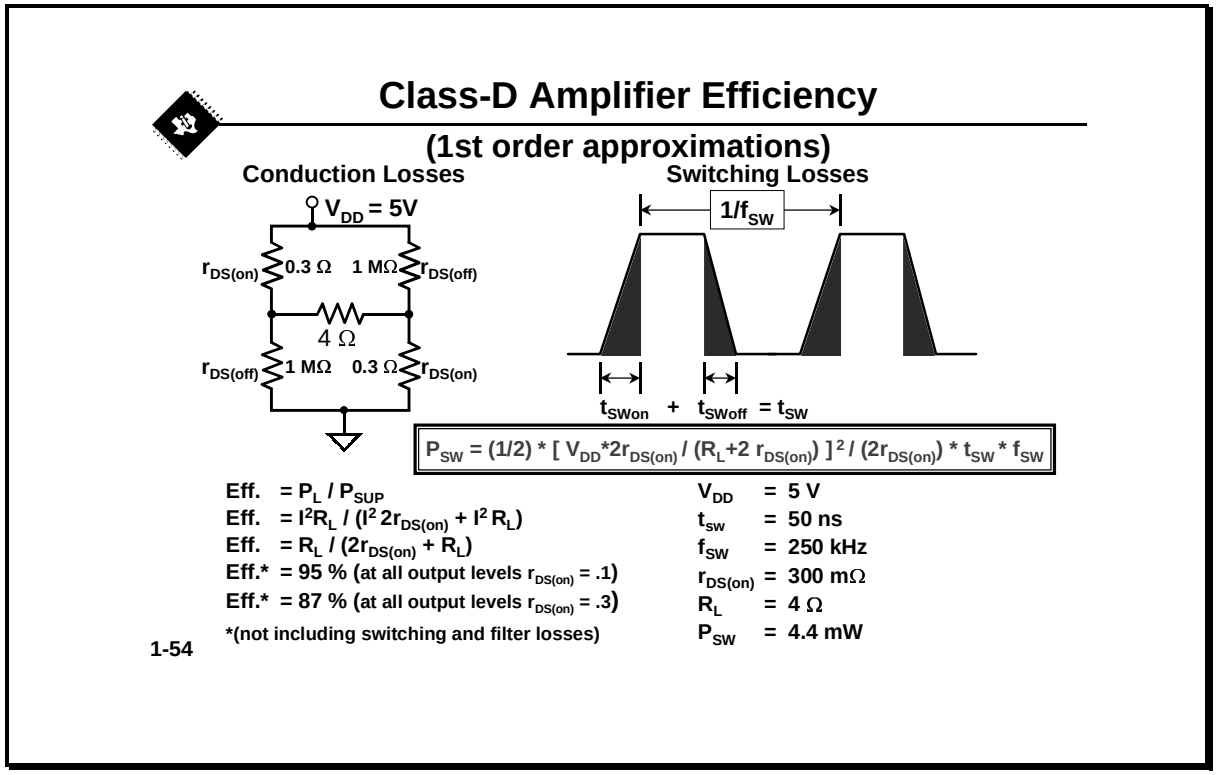
Basic PWM Generator

One must feel comfortable with the concept of PWM and how it is generated in order to have a good understanding of class-D operation. The diagram above presents a linear approach to PWM. A comparator simply compares a triangle wave with the input signal to create a “sampled” PWM representation of the waveform.

In the linear implementation the widths of the individual pulses can be infinitely variable -- there fore this is not technically a “digital” amplifier. The PWM signal can be created by sampling the input signal with an A/D converter (or using the digital output of a CD player for example) and creating a number for the signal level at a point I time. This number can then be use to generate a pulse width proportional to the magnitude of the number. This pulse could then replace the linear PWM in the block diagram on the previous page. One would then have a “digital” amplifier since the output pulse widths would then be limited in dynamic range by the resolution of the number (i.e. - number of bits).

Either technique is valid - depending on the architecture of the system. The linear input Class-D that uses either the compartor or the data converter front end is more drop-in compatible with current linear Audio Power Amps whereas

the Digital input Class-D would be more applicable to systems where all of the music is already in a digital format.



Class-D Amplifier Efficiency

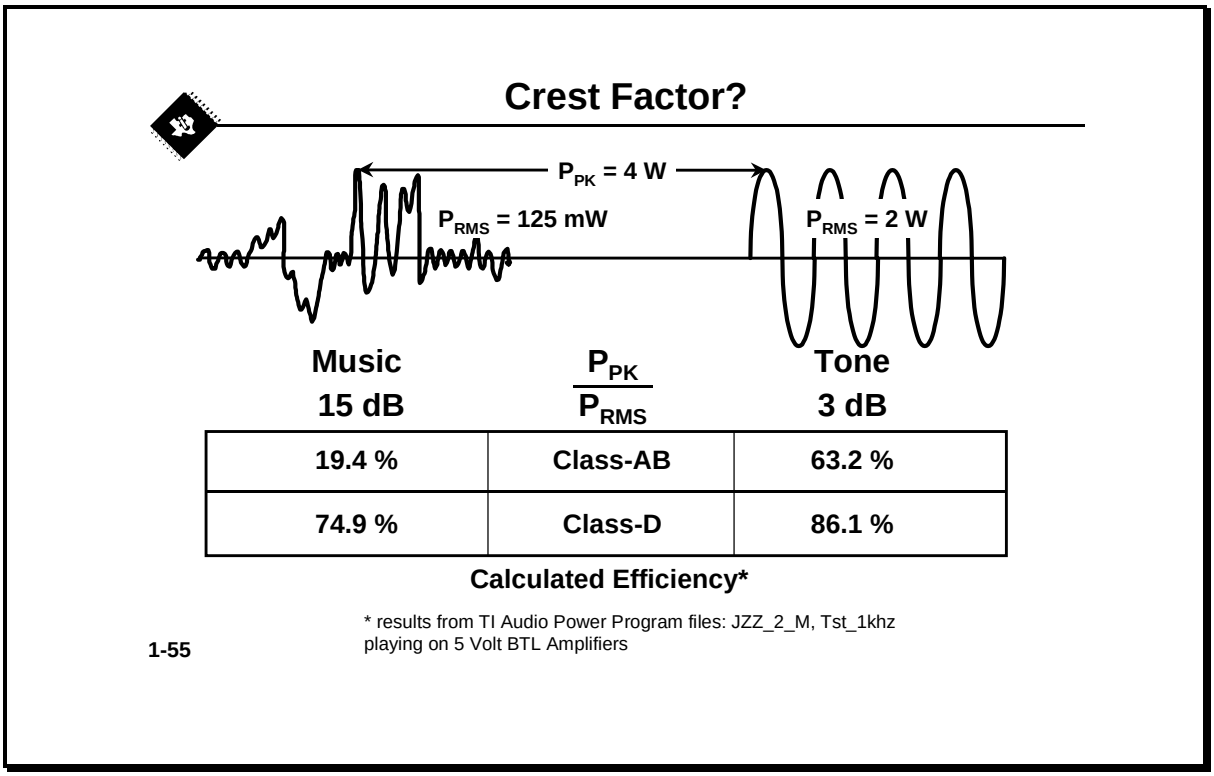
Previously, we stated that the switch-mode amplifier grabs pulses of power and efficiently delivers them to the load. We are now going to look at two of the major factors that limit the efficiency in Class-D amplifiers - $r_{DS(on)}$ losses and switching losses.

If the power FETs had an on resistance (DS(on) - Drain to Source on resistance) and they switched from off to on and on to off instantly, then Class-D amplifiers would be 100% efficient. $R_{DS(on)}$ robs the system of a set percentage of efficiency. The formula basically comes down to a ratio of the FET on resistances and the load resistance.

Switching losses are more complicated. As the FET ramps on and off it goes through a mid-resistance level that dissipates a lot of power. The longer the ramp, the more power it dissipates. Also, the switching frequency controls the switching losses. If one changes the switching speed from 250 kHz to 500 kHz then there are twice as many transitions in a given period of time and therefore the switching losses double!

The switching loss calculated above (4.4 mW) does not seem significant when compared to an amplifier that puts out 2 Watts for example. But, an amplifier that is rated for 2 W rms probably only runs at a fraction of that power when playing music. Amps are normally rated with Sine waves which have very little dynamic range from the peak to average power ratings (3 dB for a sin wave -

known as the Crest Factor). Music though, can typically run at ratios of 15 to 21 dB (factors of 32 to 128). So, for a full power music signal the average power can be low - on the order of the switching losses. This is especially true when listening to the amplifier at less than full volume (which most of us normally do).



Crest Factor

The diagram above is an example of how real music differs from sine waves (tones) in assessing the performance of an amplifier in terms of efficiency. The waveforms indicate that a tone has a nicely behaved envelope whereas the music has a widely varying envelop. This is typically referred to as dynamic range. The dynamic range of a signal is measured by Crest Crest factor which is:

Crest Factor = 10LOG(Ppk/Prms)

A high crest factor means that the difference between the peaks and the normal loudness is very high. You may also hear this referred to as Headroom at times. Since the switching losses of Class-D amplifiers are negligible in comparison to full power sine waves the efficiency at first appears quite high, but it is also high for linear amplifiers. When real music is applied then the efficiency number change quite drastically.

The example above is derived for two full power cases. The results are even more dramatic at normal listening levels. Consider your home stereo - it is a good bet that you rarely turn the volume up beyond about level 3 of 10 (unless you are listening to Bolero!). That means that peak powers are probably 6 or 9

dB down so for the example above that makes the music rms power drop from 125 mw to 15 to 30 mW. That 4.4 mW of switching losses then becomes a big loss percentage wise.

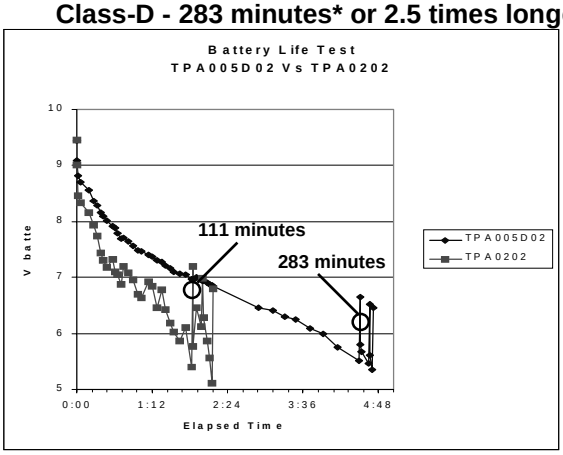
But, also keep in mind that linear amplifier efficiency drops faster than does class-D. Our analysis generally show that over normal listening levels Class-D maintains 2 to 3 times the efficiency. The next diagram documents a real live test we performed to prove out our simulated results.

Battery Life

Linear - 111 minutes*

Class-D - 283 minutes* or 2.5 times longer

*Times measured to first under-voltage lockout of DC/DC module on PnP



A head to head test of TI's Linear and Class-D 2W stereo solutions:**

Linear - TPA0202

Class-D - TPA005D02

Both set-up on the PnP platform with Bass/Treble volume control modules, DC/DC converter modules and Rayovac 9-V Alkaline batteries.

**** Standing supply current for both setups adjusted to 44 mA. Peak power ~ 1.5W.**

1-56

Battery Life

For the test we configured two PnP evaluation platforms. One with a TPA005D02 EVM and the other with a TPA0202 EVM. Using a standard Rayovac 9-Volt battery in each system and routing the exact same audio signal into both systems we let it run and monitored the battery voltage.

The DC/DC converter module will automatically shutdown when the battery voltage drops below about 5.2 volts (Under Voltage Lockout - UVLO) so we used that as an indicator that the battery had crapped out. The spikes you see on the battery voltage waveforms happen when the UVLO event happen the load o the battery goes away and the voltage drifts up until the load is reapplied. We reset the system, allowing three UVLOs to determine a good level of deadness.

Just like we had simulated with the Audio Power Program, the Class-D amplifier lasted 2.5 times longer. The Audio Power Program displays on the results screen rms current. If you know the AmpHr rating of the battery then, knowing the amps you can easily determine how long the battery will last.

In an application like Notebook Computer the battery life is probably more affected by the processor and other high power devices inside other than the APA. In boombox mode however (mode where processor does not come on the play CDs) the APA does become the primary source of power drain so one could expect longer battery life.

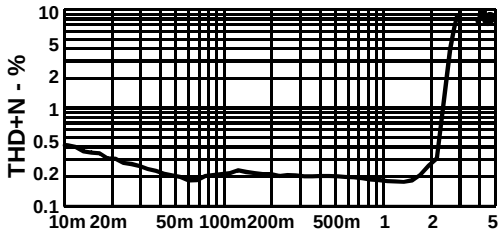
Class-D technology also makes things like rechargeable outdoor speakers for parties that use a walkman as the audio source a good possibility. Any application where the APA is a large percentage of the power drain makes Class-D attractive.

Other than battery life, heat is yet another big factor in APA system design. Increased efficiency leads to higher powers for a give heat level or smaller heat sinks which could mean smaller enclosures - lots of things become more feasible with increased efficiency!

TPA005D02 Class-D Stereo APA

Product Highlights

- **Industry's first fully integrated stereo Class-D amplifier**
- **Extremely efficient Class-D operation triples operating battery life**
- **Shutdown control ensures minimum power consumption**
- **2-W stereo bridge-tied load (BTL) output with low THD+N (0.5%) provides clear, powerful sound levels**



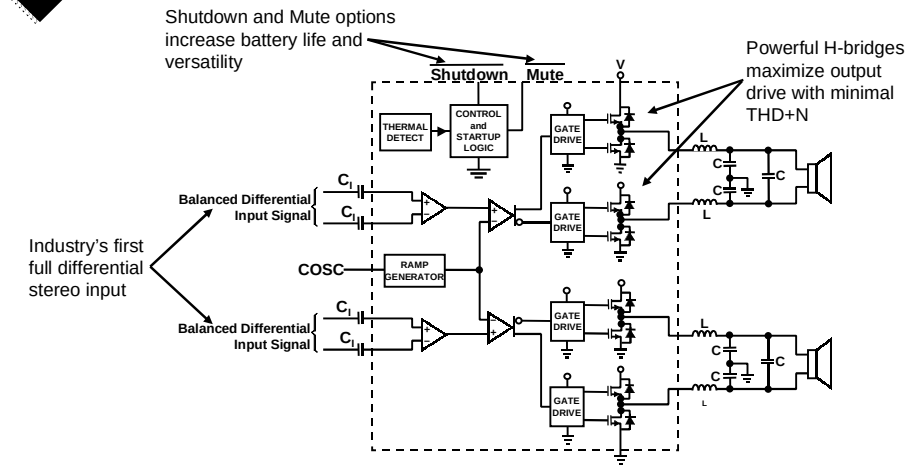
RMS Output Power - Watts

Test Conditions:
- 5-V supply
- 1-kHz frequency
- 4-Ω load

1-58

TI announced the industry's first, stereo Class-D amplifier on August, 17 1998. TI's 20+ years in designing switch-mode power supplies and experience with linear audio are two of the factors that helped expedite the release date. Another is TI's leading DMOS process which enables the low THD+N levels, high output drive and feature rich devices!

TPA005D02 Block Diagram



1-59

This is a simplified block diagram of the TPA005D02. The key things to point out the shutdown control and mute options. The shutdown control nulls supply current (quiescent current) to only 400 µA while the mute adds another option for the designer to incorporate. The TPA005D02 also has thermal and undervoltage protection.

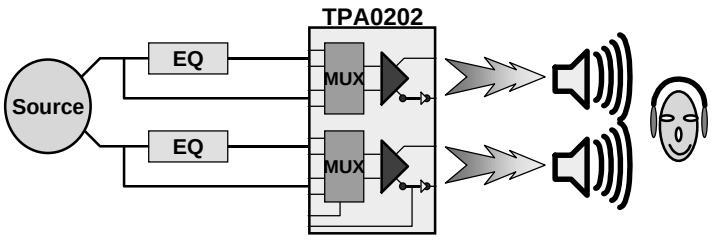
TPA0202 2-W Stereo APA

Features

- SE/BTL switch
- Stereo MUX
- Low THD+N ... 0.05%
- TSSOP PowerPAD™ package
- Depop circuitry
- Shutdown control ... I_{DD} = 5 µA
- EVM available (4/98)

Benefits

- Drives both headphones and speakers
- Allows two sets of stereo inputs
- High fidelity
- Consumes less board space
- Minimizes clicking and popping
- Maximizes battery life
- Minimizes design time



1-60

The TPA0202 is the latest generation designed for Note PCs. However, its differentiated feature set has won it design-ins in several mass market applications including P.O.S. terminals.

Key specs include 2-W output drive, SE/BTL switch, low 0.05% THD+N and versatile stereo input MUX. Designers also like the small thermally enhanced TSSOP PowerPAD package. As PCBs become more and more tightly packed, package sizes must continue to shrink. The dilemma is how to dissipate the heat generated in the amplifier as the surface area of the chip continues to shrink. This can be accomplished in two ways, make the amplifier more efficient (Class-D) and/or design innovative packaging to pull the heat from the die without large expensive heat sinks (PowerPAD).

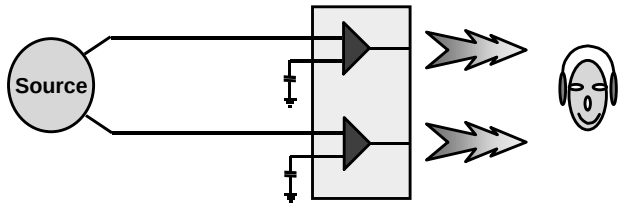
TPA1x2 APA Headphone Drivers

Features

- Ultra-low THD+N: <0.005% & High PSRR: 81db @ 1kHz (TPA152)
- 75-mW to 150-mW stereo output drive
- Internal mid-rail generator
- Depop circuitry
- Multiple pinouts

Benefits

- Low THD+N and high PSRR provide high-fidelity sound
- Powerful output drive for any headphone application
- Minimizes external components
- Nulls “pops” and “clicks”
- Drops into many existing sockets



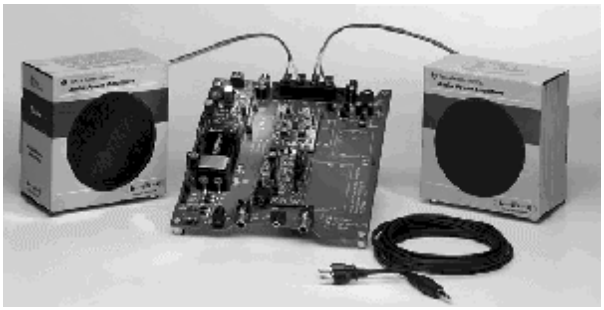
1-61

The TPA1x2 family includes the hi-fi TPA152, TPA102, TPA112, and TPA122. This family is targeted at headphone applications. These devices were designed with the most popular pinouts to help facilitate the design.

The TPA152 provides the best performance in the family with THD+N levels below 0.005% and PSRR above 81dB. Every member includes an internal mid-rail generator which minimizes external components by integrating the voltage divider circuit. Other improvements include integrated depop circuitry that eliminates the “popping” and “clicking” when the device switches power levels.

Plug-n-Play Audio EVMs

Easy to Use **Complete System**



Roadmap Compatible **Total Modularity**

1-62

TI's APA Plug 'n Play kit is a one of kind and another example of the innovation driving the audio roadmap.

This kit allows designers to quickly evaluate ANY released TI audio power amplifier in seconds. And every new TI APA will have an EVM that plugs directly into the base platform. Each EVM comes with a user's guide which includes the reference design used on the board and a bill-of-materials. All you need to quickly evaluate and choose which TI APA works best for your application.

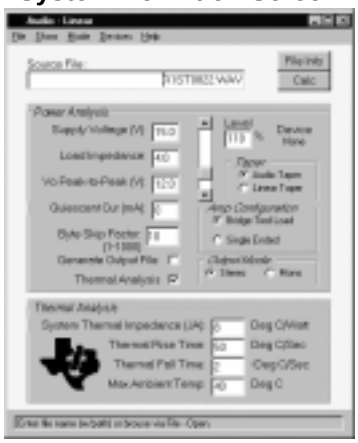
You can order the APA kit from your local authorized TI distributor or directly from TI's web site at:

http://www.ti.com/sc/docs/msp/tools/audio.htm

Audio Power Analysis Program

- **Power/thermal analysis**
- **Real music .WAV files**
- **System flexibility**
- **Windows based**
- **Free from the WEB**

System Definition Screen



www.ti.com/sc/docs/msp/pran/app_supp.htm

1-63

The Audio Power Analysis Program allows designers to quickly and accurately calculate power consumption and thermal data from real audio waveforms. Determining these results by hand involves very time consuming, complex calculas or grossly simplified sinewave approximations that often mislead the designer to over build part of the circuit.

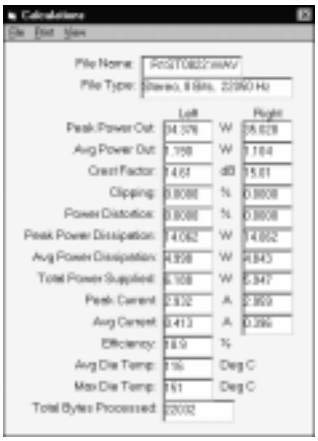
The software package is completely Windows based, will perform calculations on any .wav file and is downloadable FREE from TI's website! The web URL is:

http://www.ti.com/sc/docs/msp/pran/app_supp.htm

Results for a typical .wav file are shown on the following foil.

Audio Power Program - results

System Results Screen



- **Output power**
- **Crest factor**
- **Distortion**
- **Power dissipation**
- **Power supply currents**
- **Efficiency**
- **Die temperatures**

1-64

This graphic and the prior one are actual screen captures from the Audio Power Analysis Program. As you can see the program displays the results in a neat, clean tabular format. Everything a designer needs; from crest factor to the die temperature is included.

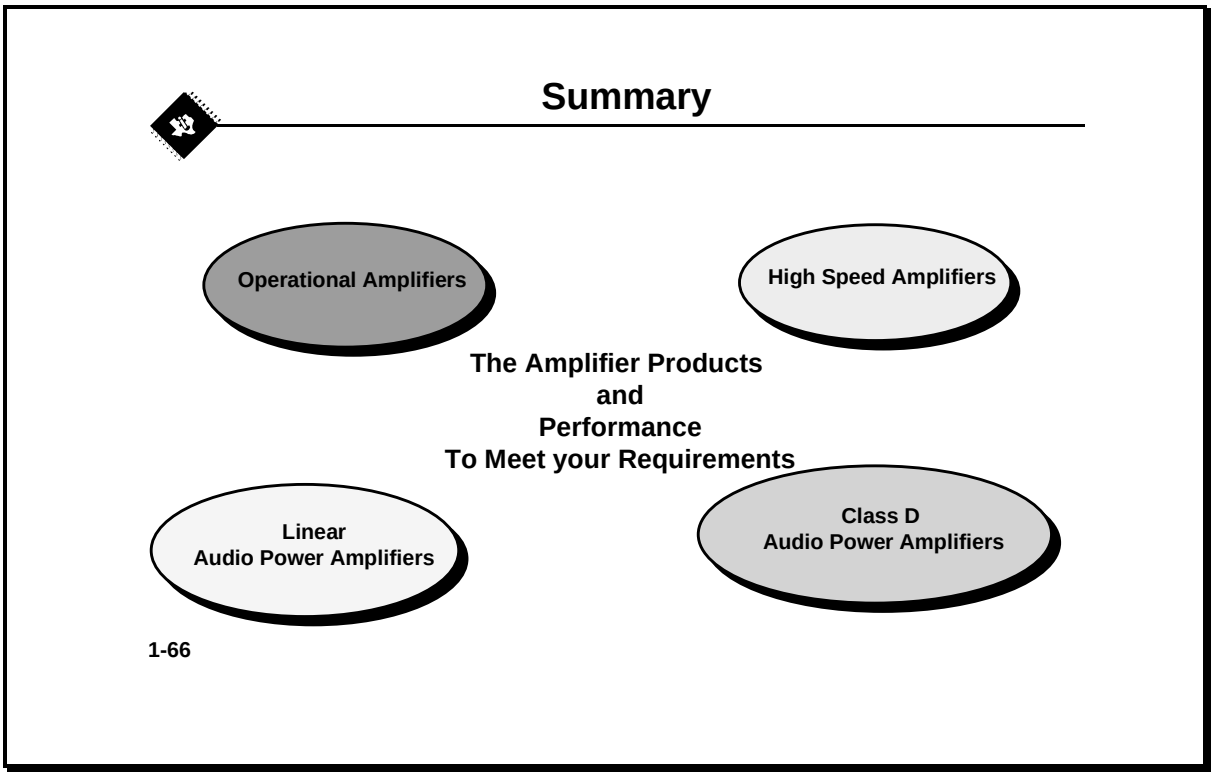
Time to market directly impacts the success of our customers. The emphasis on our APA suite of design tools is focused on helping customers design first-to-market, innovative solutions.

Audio Power Amplifiers - TPA

	V_{CC} (V)	I_{DD} (mA)	Output/ch (W)	THD+N @ 1kHz (%)	K_{SVR} (dB)	I_{SD} (µA)	Head-phone	Device Description	Data Sheet
TPA152	4.5 / 5.5	5.5	0.075	0.02	81	-	y	75 mW stereo, SE	SLOS210
TPA102	2.5 / 5.5	1.5	0.150	0.05	76	10	y	150 mW stereo, SE	SLOS213
TPA112	2.5 / 5.5	1.5	0.150	0.05	76	-	y	150 mW stereo, SE	SLOS212
TPA122	2.5 / 5.5	1.5	0.150	0.08	76	10	y	150 mW stereo, SE	SLOS211
TPA302	2.7 / 5.5	4	0.3	0.3	65	0.6	y	350-mW stereo SE	SLOS174A
TPA301	2.5 / 5.5	0.7	0.35	0.3	78	0.15	y	350-mW mono BTL	SLOS208
TPA311	2.5 / 5.5	0.7	0.35	0.3	78	7	y	350-mW mono SE/BTL	SLOS207
TPA701	2.5 / 5.5	1.25	0.7	0.3	78	0.005	n	700-mW mono SE	SLOS229
TPA711	2.5 / 5.5	1.25	0.7	0.3	78	50	y	700-mW mono SE/BTL	SLOS230
TPA721	2.5 / 5.5	1.25	0.7	0.3	78	50	n	700-mW mono SE	SLOS231
TPA4860	2.7 / 5.5	3.5	1	0.3	75	0.6	n	1-W mono BTL	SLOS164
TPA4861	2.7 / 5.5	3.5	1	0.3	75	0.6	n	1-W mono BTL	SLOS163
TPA0102	3 / 5.5	19	1.5	0.05	75	5	y	1.5-W stereo SE/BTL	SLOS166D
TPA0103	3 / 5.5	19	1.75	0.05	75	5	y	1.75-W mono SE/BTL	SLOS167
TPA0202	3 / 5.5	19	2	0.05	75	5	y	2-W stereo SE/BTL	SLOS205
TPA005D02	4.5 / 5.5	25	2.0	0.4	40	400	n	2-W Class-D stereo	SLOS227
TPA1517	9.5/18	40	6, 4.5	10, 0.2	65	7	n	6-W stereo BTL	SLOS162A

1-65 **(all data @ +5V, 25°C, typ)**

Audio Power Amplifier Selection Chart

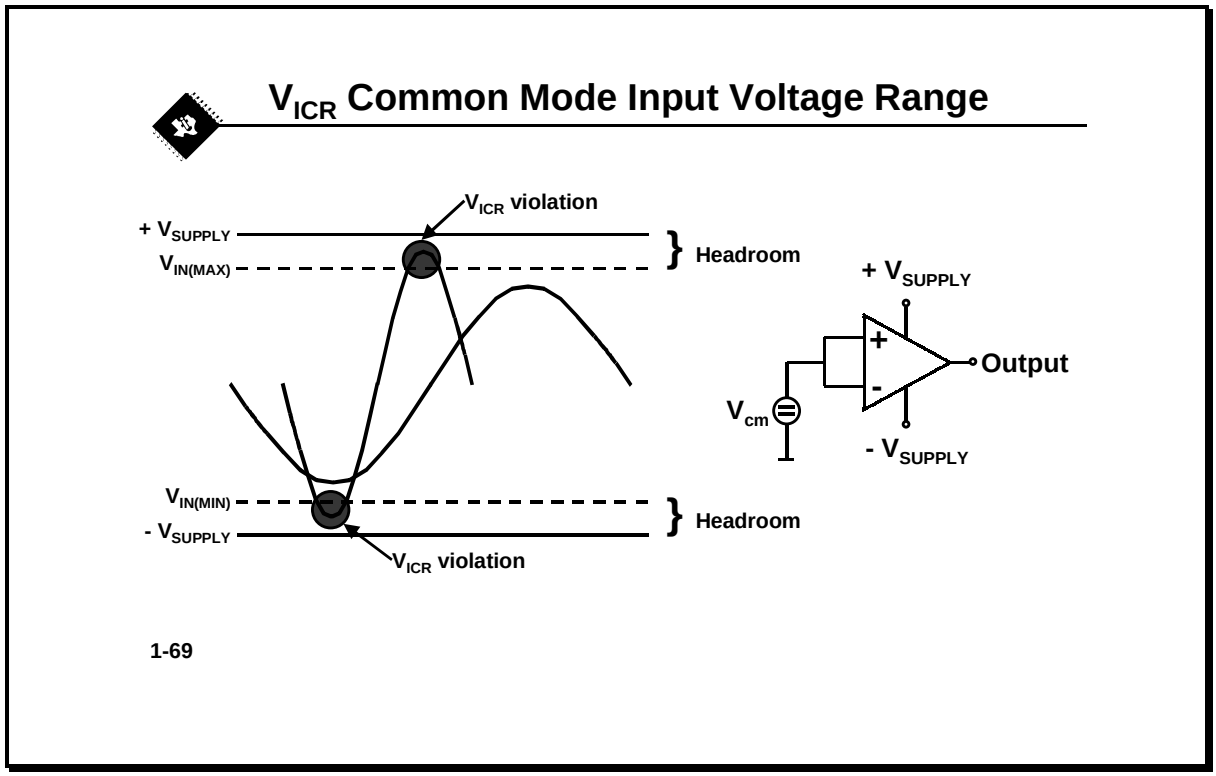


Conclusion

Texas Instruments has the amplifiers you need. The task is to select the functionality required, then identify and rank the key care abouts for your system. The properties you identify can then be matched against available technologies and performance. Selecting the right amplifier is not difficult when aproached systematically, and the right amplifier selection is key to optimum performance in signal conditioning.

Reference Material

Input Stage Considerations



Common-Mode Input Voltage Range V_{ICR}

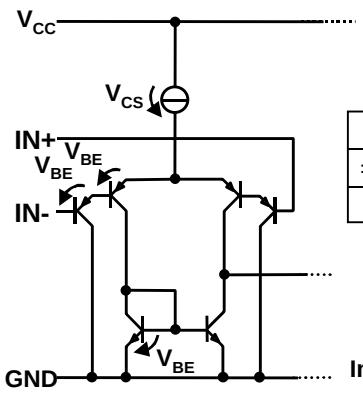
Op amp input topologies typically require some voltage headroom from either the positive or negative supply rail, or both, for proper biasing. Taking a signal outside the specified common-mode voltage range (V_{ICR}) can cause unanticipated behaviour ranging from an exponential increase in dc offset error to phase inversion at the output. Failure to recognise V_{ICR} restrictions, especially when moving from wide split supplies to lower voltage single supply designs is probably the most common error designers make. This is especially true when using BiFET op amps, which are ill suited for low voltage single supply designs.

The problems which are caused by the Common-Mode Input Voltage Range are often neglected or even unknown.

Therefore, the next pages cover a discussion of the Common Mode Input Voltage Range for each of the today‘s different technologies and their limitations.

V_{ICR} Common Mode Input Voltage Range

Bipolar Op Amp



V_{CC}	V_{ICR} min @ 25 °C	Unit	Device
± 15 V	-15 to 13.5	V	TLE2021/2/4
5 V	0 to 3.5	V	LM124/324, LM2904

Typical V_{ICR} values

Input stage schematic of the LM324/2902

1-70

V_{ICR} - Bipolar Op Amp -

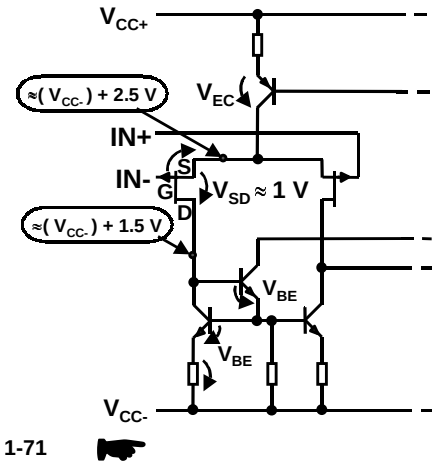
In many applications, it is important to be able to handle input voltages down to the negative supply, or especially down to ground in a single supply application. This goal can easily be achieved in a bipolar design by using an input differential amplifier, which consists of PNP transistors. The picture above shows the input stage schematic of the LM324/LM2902. Since the input consists of PNP transistors, a linear operation is only possible if the voltage at the base is 0.7 V more negative than the voltage at the emitter. Therefore, it is possible to apply an input voltage which goes down to the negative supply.

However, on the other hand we can see directly the limitation of the V_{ICR} in the positive direction. The picture shows the voltage drop V_{CS} at the current source ($\approx$ 400 mV for a bipolar, non cascaded current source) and the two voltage drops V_{BE}, each of 0.7 V. The resulting maximum voltage at the input of the op amp is therefore around 2 V below the positive supply voltage.

The table shows the behaviour of different op amps and different supply voltages. It can be seen that the headroom from the positive supply is nearly independent of the supply voltage.

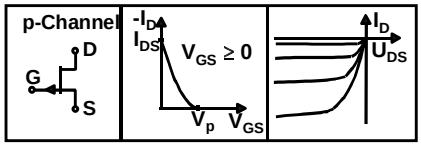
V_{ICR} Common Mode Input Voltage Range

BiFET Op Amp



V_{CC}	V_{ICR} typ @ 25° C	Unit	Device
± 15 V	-11.9 to 15	V	TL071, TLE2071
± 5 V	-1.9 to 5	V	TLE2071/81

Typical V_{ICR} values



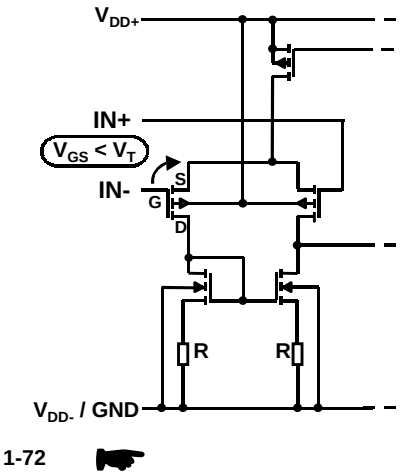
FET Characteristics

V_{ICR} - BiFET Op Amp -

Texas Instruments BiFET op amps combine P-type JFETs on the input stage with bipolar transistors. The picture above shows the input stage of the BiFET op amp TL071/82. For this kind of op amp, a linear operation is only possible, if the gate-source voltage $V_{GS} \geq 0$. Therefore, the V_{ICR} includes the positive supply rail, but **not** the negative supply rail. The picture shows the voltage drop at the resistor R, the two voltages V_{BE} at the current mirror which is built up by two NPN transistors (each of them with a 0.7 V base-emitter voltage) and the voltage V_{SD} at the FET transistor. To operate a FET transistor in the area where its drain current I_D is mostly dependent on the gate-source voltage V_{GS} and not on the source-drain voltage V_{SD}, a minimum voltage V_{SD} of ≈ 1V is required. This can be seen in the characteristic V_{SD} versus I_D. The resulting headroom to the negative supply voltage at the input of the op amp is around V_{CC-} + 2.5 V.

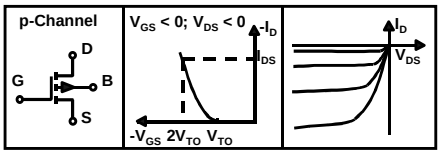
V_{ICR} Common Mode Input Voltage Range

Advanced LinCMOS™



V_{CC}	V_{ICR} min @ 25° C	Unit	Device
± 5 V	-5 to 4	V	TLC2252/62/72
3 V	0 to 4	V	TLV2252/62

Typical V_{ICR} values



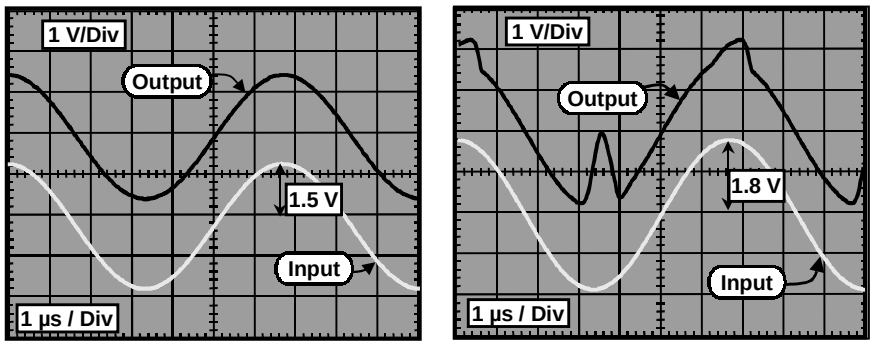
MOS Transistor Characteristics

V_{ICR} - CMOS Op Amp -

Texas Instruments CMOS op amps combine p-channel MOS transistors in the input stage. The picture above shows the input stage of the TLC/TLV2262 CMOS op amp. A linear operation is only possible, if the voltage $V_{GS} < V_T$ (see the characteristic of this p-channel MOS transistor). This means that the applied common-mode voltage may reach the negative supply/GND while functioning properly.

TI CMOS op amps are therefore well suited for single supply applications where small signals near ground have to be measured and amplified. However, the common-mode voltage in the positive direction is limited by the threshold voltage V_T of the input transistors. The table shows the headroom to the positive supply of around 800 mV to 1.5 V.

TLV2362 - Common-Mode Input Voltage Range



Input: ± 1.5 V Input: ± 1.8 V

V_{CC} = ± 2.5 V, V_{ICR} = ± 1.5 V

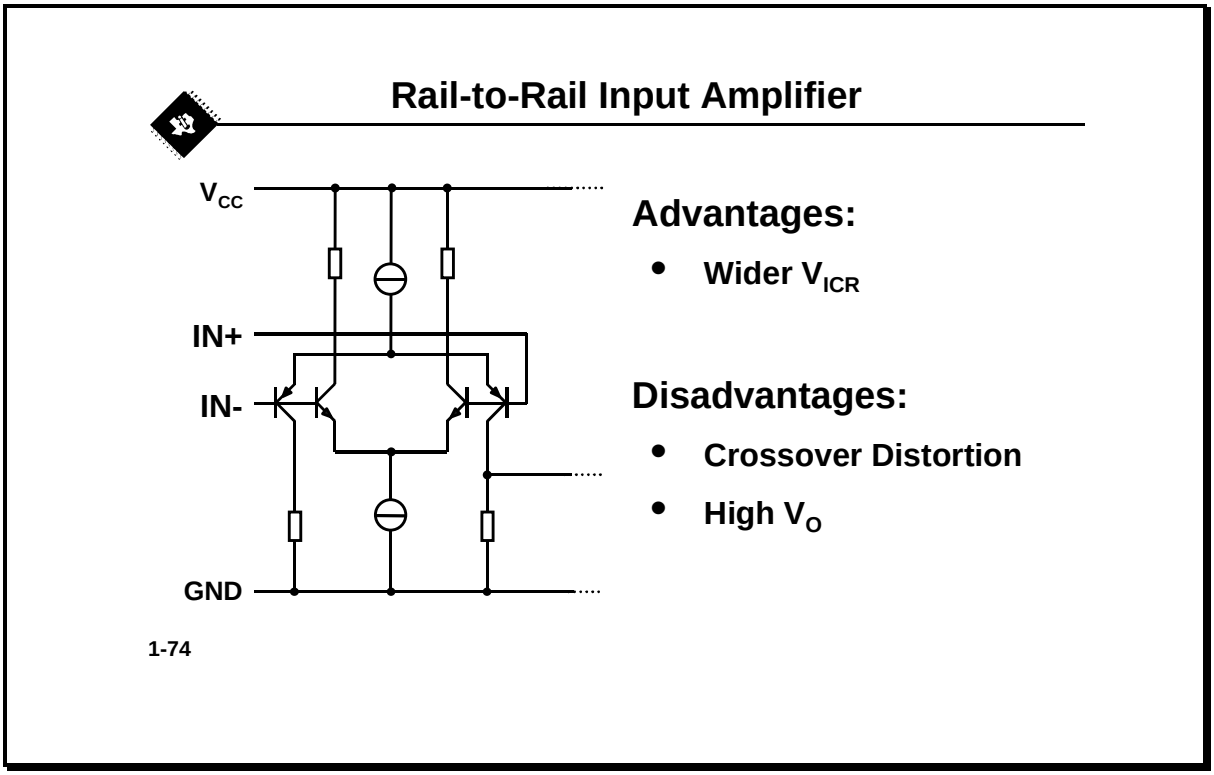
1-73

TLV2362 – Common-Mode Input Voltage Range

The reasons for restrictions in the Common-Mode Input Voltage Range V_{ICR} were explained in detail for the different technologies on the pages before. The effect of an input voltage which exceeds the V_{ICR} can be seen on this picture. The measurement shows the curves of the input and output of the op amp TLV2362 which is operated as a voltage follower. The common-mode input voltage range of the TLV2362 is specified with ±1.5 V when operating at ±2.5 V supplies with a temperature of 25°C. The picture on the left shows that the output provides the expected output voltage with an input voltage of 1.5 V_P. However, if the input voltage is increased to 1.8 V_P, which means that the common-mode input voltage range is exceeded, the output voltage shows a phase inversion. This can be seen in the picture on the right.

The main specifications of this op amp are:

- Low Supply Voltage Operation $V_{CC\pm}$ = ±1 V Min
- Wide Bandwidth, 7 MHz typ at $V_{CC\pm}$ = ±2.5 V
- High Slew Rate 3V/µs typ at $V_{CC\pm}$ = ±2.5 V
- Wide Output Voltage Swing, ±2.4 V typ at $V_{CC\pm}$ = ±2.5 V, R_L = 10kΩ
- Low Noise, 8 nV/$\sqrt{Hz}$ typ at f = 1 kHz
- Available in SOT-23 (TLV2361) and TSSOP (TLV2362) packages



Rail-to-Rail Input Amplifier

The problem with the limited Common-Mode Input Voltage Range V_{ICR} can be overcome with a so called Rail-to-Rail input stage. Such an input stage allows an input voltage from the negative supply voltage to the positive supply voltage. This feature can be achieved with two differential input pairs, one built up from PNP transistors and the other from NPN transistors. Therefore, the input switches its operation from one input pair to the other input pair depending on the input voltage.

However, in such designs the input offset voltage may increase dramatically in comparison to the conventional input stage. Especially in DC-applications where a low input offset voltage is required, a Rail-to-Rail input op amp may not fulfil the requirements in terms of DC-parameters. In addition to that, there exists a crossover distortion in the switching region between the two input pairs. The applications for a Rail-to-Rail input are limited. These could be high level sensing applications or an op amp which is configured to work as a buffer.

Nevertheless, Texas Instruments is also developing the full Rail-to-Rail input op amp, because in some specific applications this feature is important.

TLV24x2 - Wide-Input-Voltage Op Amp

TLV24xx

Rail-to-Rail Output

V_{ICR} = 0 to 4.5 V (min), V_{CC} = 5 V

V_{IO} = 950 µA max at T_A = 25° (TLV24xxA)

R_O = 600 Ω

TLV2432

125 µA / channel (max)

Gain Bandwidth = 0.5 MHz typ

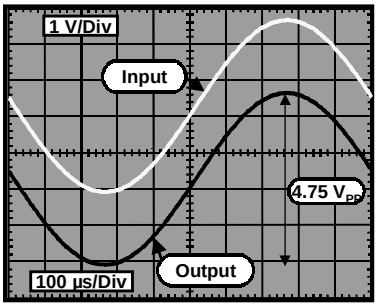
Low noise 18 nV /√Hz typ at 1 kHz

TLV2442

750 µA / channel (typ)

High Gain Bandwidth = 1.8 MHz typ

Low noise 16 nV / √Hz typ at 1 kHz



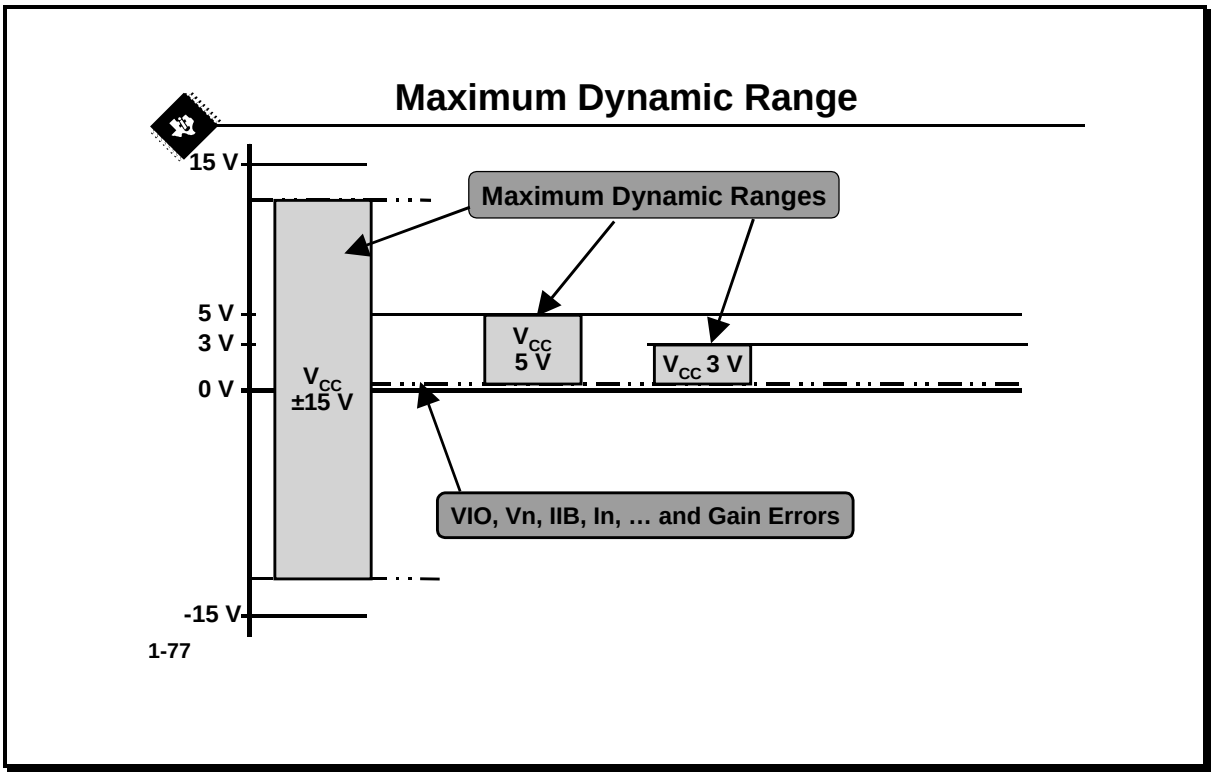
1-75

TLV24x2 – Wide-Input-Voltage Op Amp

As discussed already, the true Rail-to-Rail input op amp often shows a degraded "DC behaviour" because of the two differential input pairs. Texas Instruments has developed op amps which feature a "wide input" by using only a single differential input stage without degradation of the DC behaviour. These are the TLV2432 and the TLV2442. They are dual low-voltage operational amplifiers. The common-mode input voltage range for this device has been extended over that of typical standard CMOS amplifiers making it suitable for a wider range of applications. In addition, the devices exhibit Rail-to-Rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterised for 3-V and 5-V supplies and is optimised for low-voltage operation. The TLV2432 requires only 100 µA (typ) of supply current per channel, making it ideal for battery powered applications. Both the TLV2432 and the TLV2442 have also an increased output drive over previous Rail-to-Rail operational amplifiers to drive 600-Ω loads for telecom applications.

Output Stage Considerations

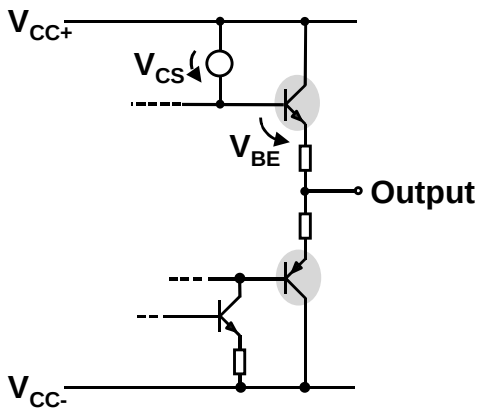
The op amp output stage is critical to performance and therefore must be considered when choosing an op amp. Maxumim dynamic range, rail-to-rail operation and drive capability are all related to the output stage and are discussed in the following section.



Maximum Dynamic Range

A very important parameter in system design is the signal-to-noise ratio (SNR) and the dynamic range. These are first of all limited by the supply voltage used. The diagram shows the maximum dynamic range for the different supply voltages of ± 15 V, single supply + 5 V and + 3 V. It can be seen that the reduction to + 5 V or + 3 V reduces the maximum dynamic range of the op amp considerably and will ultimately limit the performance of the system. In addition to the supply voltage, the dynamic range is limited to the sum of the op amp's errors caused by the input offset voltage, input bias current, gain, etc. It is obvious that for a single supply voltage of + 5 V or + 3 V, it is important that as much of the reduced supply voltage is available for a useful signal output swing of the op amp. This can be obtained by using Rail-to-Rail amplifier. The output of the Rail-to-Rail op amps can be driven up to the supply voltages.

Emitter Follower Output Stage of an Op Amp



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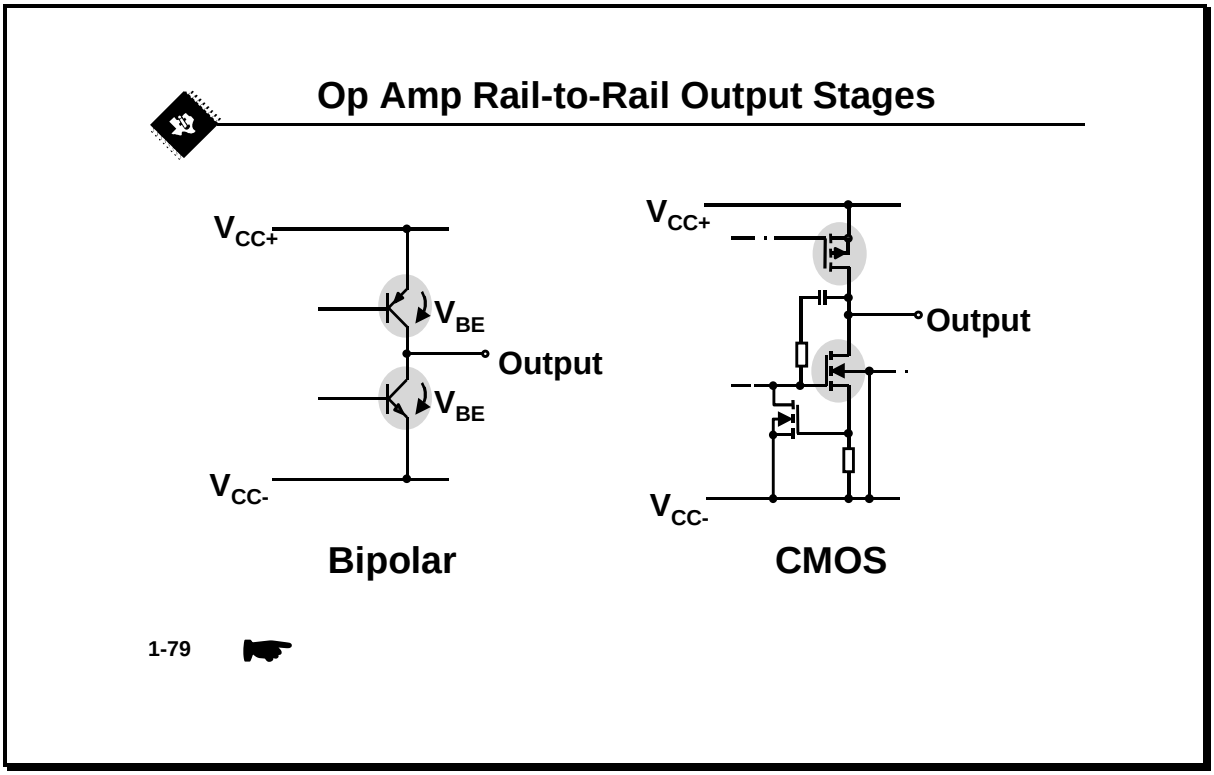
Emitter Follower Output Stage of an Op Amp

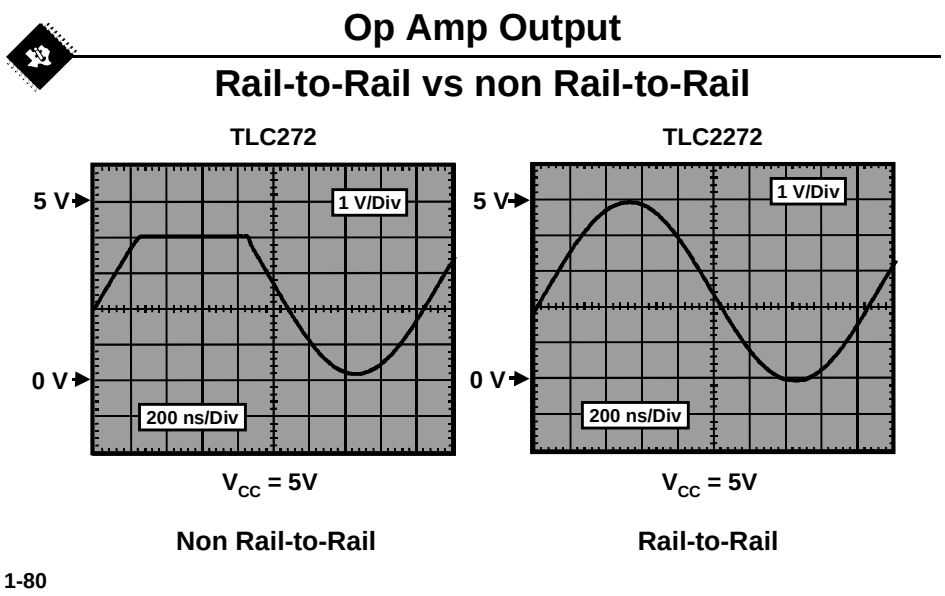
The circuit diagram shows a typical emitter follower stage which is widely used in op amps. The output voltage of this op amp is limited, because of the voltage drop of a few hundred mV (≈ 400 mV for a bipolar, non-cascaded current source) across the current source and the forward voltage of the output transistor's base-emitter diode of 0.7 V. Therefore the available signal peak-to-peak swing at the output of the op amp is reduced. This is not a problem if a power supply of ±15 V or ±12 V is used in a system. However, if a single supply of +5 V or even +3 V is used, the headroom between signal and supply rail will dramatically reduce the output swing of the op amp and will therefore also reduce the dynamic range and the SNR of the system.



Rail-to-Rail Output Stage of an Op Amp

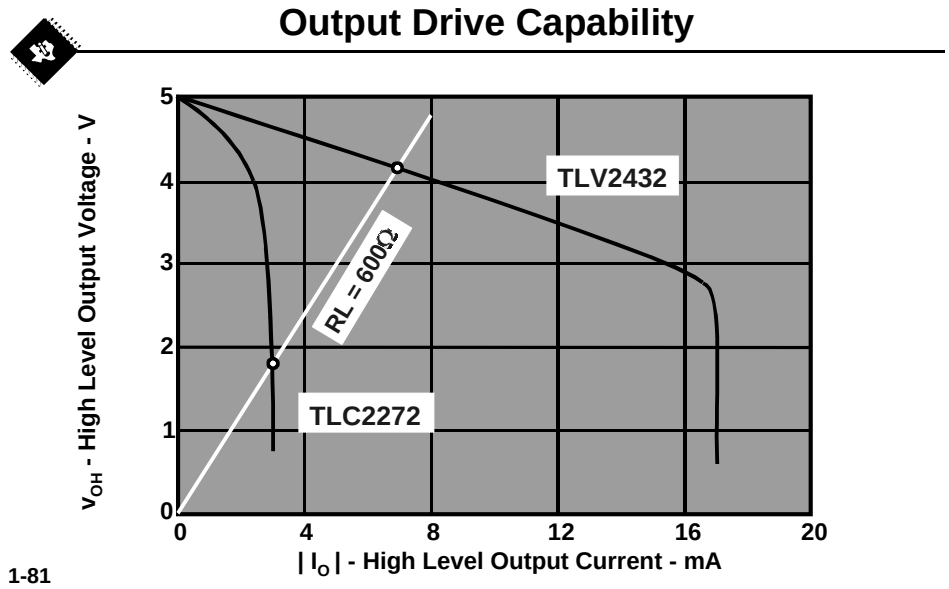
A solution to the problem of having headroom at the output between the signal and the supply rails, especially in a single supply low voltage system is an op amp which has a Rail-to-Rail output stage. This allows the output to swing close to the supply rails, which improves the dynamic range and signal to noise ratio. A bipolar Rail-to-Rail output stage can be designed by using a common-emitter output stage. In such a stage, the output swing is limited to the saturation voltage V_{CE} of the output transistors. The saturation voltage depends on the amount of load current, which might result into a saturation voltage of a few mV up to 500 mV.

The signal swing in a CMOS Rail-to-Rail op amp is limited only to the voltage drop caused by the resistance $R_{DS(on)}$ of the output stage transistor. Therefore it is possible to achieve a signal swing very close to the supply rails of the op amp. However, in this case also the maximum peak-to-peak value depends on the load which has to be driven by the output of the op amp.



Rail-to-Rail vs non Rail-to-Rail

The measurement shows the different behaviour of a Rail-to-Rail op amp versus a non Rail-to-Rail op amp. The TLC2272 which is Rail-to-Rail capable at the output is able to deliver an output signal which goes near to the 5-V supply voltage. The TLC272 clips the positive signal at around 4 V. This is equivalent to a reduction in the dynamic range of approximately 2 dB. It is therefore recommended for single supply application to choose Rail-to-Rail op amps, if the SNR and dynamic range is important.



Output Drive Capability

The maximum output drive capability of a CMOS op amps is less than that of a bipolar one. This might introduce a problem for Rail-to-Rail op amps which have to source a higher current at high output voltages. This might be the case when interfacing to A/D converters on 5V supplies. For CMOS op amps which cannot deliver that current, distortion is generated. Texas Instruments has now introduced CMOS op amps which are able to deliver a higher ouput current. This is also important for driving a flash A/D converter, where the input can be seen as a capacitance which switches between the analog input and the internal comparators of the converter. If the analog voltage is different to the charge of the capacitor at the time when the capacitor switches to the analog input, a high current from the op amp is required.

Advanced LinCMOS™

Rail-to-Rail Output Op Amps

DEVICE	SUPPLY (V) (Rated)	(Min)	V_{OH} (Min) I_{OUT} = 20 µA	V_{IO} (max) mV	GBW MHz	Feature
TLC2201/2	±5/+5	4.6	4.8	0.6	1.9	
TLC2252/4	±5/+5	4.4	4.98	1.5	0.2	
TLC2262/4	±5/+5	4.4	4.99	1.5	0.71	
TLC2272/4	±5/+5	4.4	4.99	1.5	2.18	
TLC4501	±5/+5	4	4.99	0.08	4.7	Self Calibrating
TLC4502	±5/+5	4	4.99	0.1	4.7	Self Calibrating
TLV2252/4	+3/+5	2.7	2.98/4.98	1.5	0.18	
TLV2262/4	+3/+5	2.7	2.99/4.98	1.5	0.67	
TLV2422	+3/+5	2.7	2.98/4.97	2	0.052	Wide Input
TLV2432	+3/+5	2.7	2.98/4.97	2	0.5	Wide Input
TLV2442	+3/+5	2.7	2.98/4.97	2	1.8	Wide Input
TLV2772	+2.7/+5	2.2	2.6(0.07 mA)/ 4.9(1.3 mA)	2.5	5.1	

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Advanced LinCMOS™ Rail-to-Rail Output Op Amps

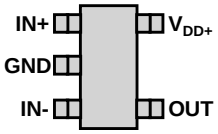
Texas Instruments manufactures a growing number of Rail-to-Rail output operational amplifiers. The TLC22xx devices are specified for a single 5-V supply and for a ±5-V supply. The TLV22xx and TLV24x2 are specified for a single 3-V supply and for a single 5-V supply.

Advanced LinCMOS™

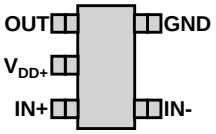
SOT-23 Rail-to-Rail Output Op Amps

DEVICE	SUPPLY (V) (Rated)	(Min)	V_{OH} (Min) I_{OUT} = 20 µA	V_{IO} (max) mV	GBW MHz	Feature
TLV2211	+3/+5	2.7	2.94/4.95	3	0.065	Micropower
TLV2221	+3/+5	2.7	2.97/4.88	3	0.48	Very Low Power
TLV2231	+3/+5	2.7	2.87/4.9	3	1.9	Low Power
TLV2711	+3/+5	2.7	2.94/4.95	3	0.065	Micropower
TLV2721	+3/+5	2.7	2.97/4.88	3	0.48	Very Low Power
TLV2731	+3/+5	2.7	2.87/4.9	3	1.9	Low Power

TLV22x1 pinout



TLV27x1 pinout



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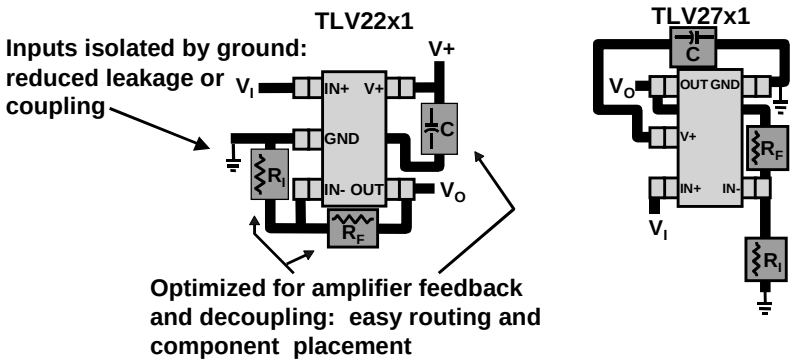
Advanced LinCMOS™ SOT-23 Rail-to-Rail Output Op Amps

Texas Instruments also introduced several Rail-to-Rail op amps in the SOT-23 package. These are basically 2 families, the TLV22x1 and the TLV27x1. Both families have op amps in a 'Micropower', 'Very Low Power' or 'Low Power' version. The two families are different in their pinning as shown in the picture.

SOT-23 Op Amps



☛ **Texas Instruments has the Footprint you need !**

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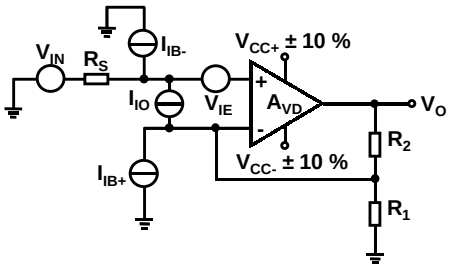
Layout Consideration of SOT-23 Packages

As already mentioned before, the Texas Instruments SOT-23 op amps are available in two different package options. The pinout of the op amp on the left side of the picture offers several advantages, because the inputs are isolated by the ground pin. This reduces leakage and coupling. The pinout is furthermore optimised for amplifier feedback offering easy routing and component placement.

DC Input Referred Errors



Input Offset Errors:

$V_{IE} = V_{IO} + V_{CMRR} + V_{kSVR} + V_N$

$I_{IB} = (I_{IB+} + I_{IB-})/2$

$I_O = |I_{IB+} - I_{IB-}|$

Gain Related Error:
(Non-inverting Amplifier)

$$A = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

$\beta = R_1 / (R_1 + R_2)$

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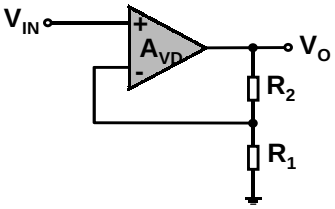
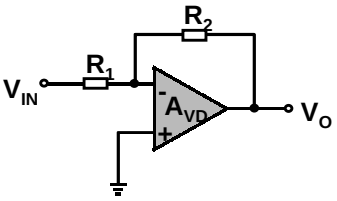
DC Input Referred Errors

The DC accuracy of an analog system is mainly limited by two parameters. These are the input offset errors and the gain-related error. The total input offset voltage is caused by the input offset voltage, the input bias current, the common-mode rejection ratio and the supply voltage rejection ratio of the op amp. The total input offset voltage raises a DC output error. A further important parameter is the open loop voltage Gain A_{VD} of the op amp. Ideally, this gain is infinite; however, in reality it will be typically in the range of 100 dB at DC and rolls off at frequencies above 100 Hz. The following pages give a detailed analysis of the influence of the input offset error and gain error on the output voltage of the op amp.

Signal Gain





Non-inverting Amplifier Gain

$$A = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

$$\beta = R_1 / (R_1 + R_2)$$

Inverting Amplifier Gain

$$A = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

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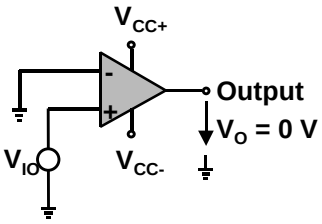
Gain Errors

Every op amp has a particular open loop gain which is called A_{VD}. Ideally, as already seen before, this gain would be infinite, but in reality it will for many op amps be 100 dB at DC and rolls off at frequencies above around 100 Hz. The frequency at which A_{VD} reaches 0 dB is known as the Unity Gain Bandwidth of the op amp. The gain limits the accuracy of an op amp and the bandwidth limits the maximum operating frequency. The closed loop gain results from the feedback which is used in the op amp circuitry.

Input Offset Voltage (V_{IO})

Input offset voltage is amplified by op amp gain



Parameter (best case)	Technology		
	BIPOLAR @ V_{CC} = ± 15 V	BiFET @ V_{CC} = ± 15 V	CMOS @ V_{CC} = 5 V
V_{IO}(typ)	10 µV	0.3 mV	80 µV
V_{IO}(max)	25 µV	1.5 mV	200 µV
$\frac{\Delta V_{IO}}{\Delta T}$	0.1 µV/°C	5 µV/°C	0.5 µV/°C

For a 5 V ADC:
10 bit: 1 LSB = 4.88 mV
12 bit: 1 LSB = 1.22 mV

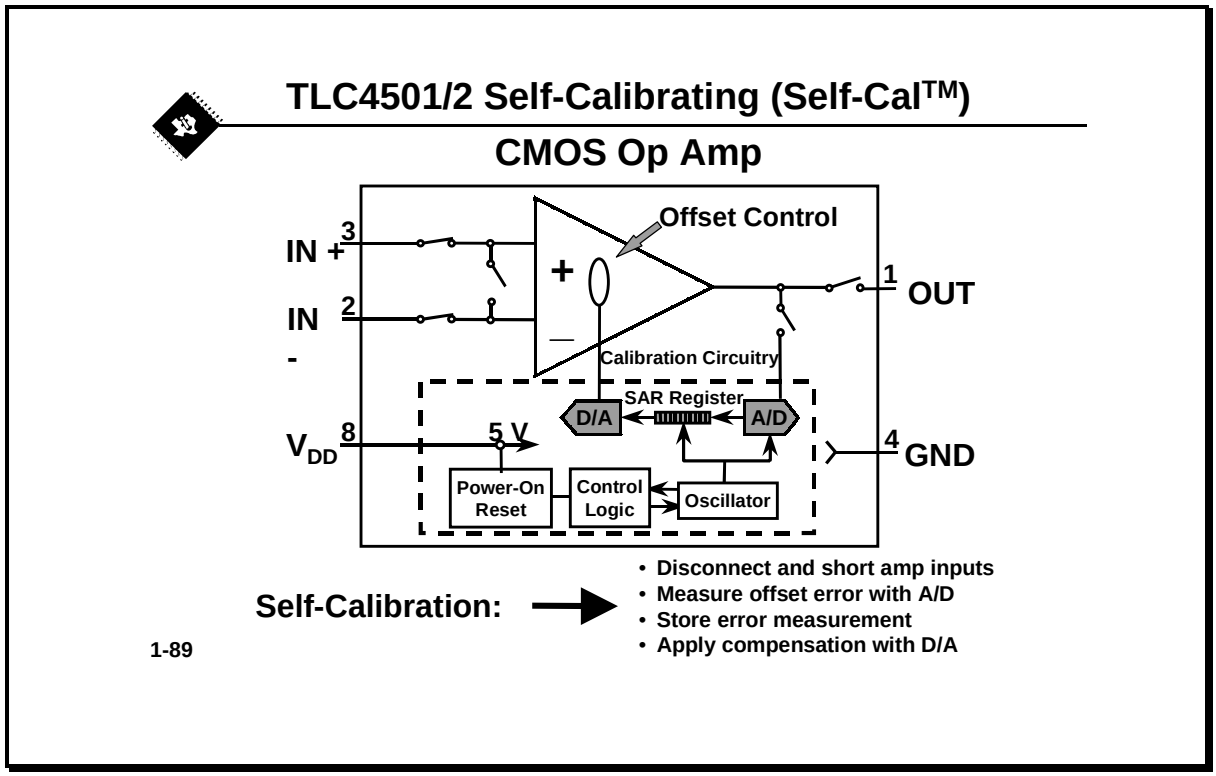
1-88

Input Offset Voltage (V_{IO})

An ideal op amp, where the inputs are both connected to ground, would provide theoretically an output voltage of 0 V, because the differential and common-mode voltage in that case is zero. However, the real op amp shows an output voltage which is not equal to zero. A small input offset voltage V_{IO} between the differential inputs is imaginable, and causes the output voltage.

The input offset voltage V_{IO} of an operational amplifier is the voltage that must be applied between the two input terminals to get an output voltage of 0 Volt, as shown in the picture. The voltage V_{IO} may be positive or negative and this is caused mainly by the mismatch of the input transistors of the op amp's differential input stage. The voltage V_{IO} is amplified with the gain of the amplifier. This may be the open loop gain, or the gain at which the op amp is adjusted. In addition, the input offset voltage is also dependent on the ambient temperature. The best devices vary around 0.1 µV/°C and this may go up to several tenths of µV/°C.

Bipolar op amps have typically the lowest V_{IO} and temperature drift. CMOS devices can achieve offset voltages of around 100 µV, which is better than BiFET, but cannot compete with the best bipolar devices. However, chopper stabilised CMOS op amps achieve a very low input offset voltage down to 1 µV (max). One of the latest CMOS op amps introduced by Texas Instruments integrates a self calibration to allow a maximum V_{IO} of 40 µV. This technology is described on the following page.

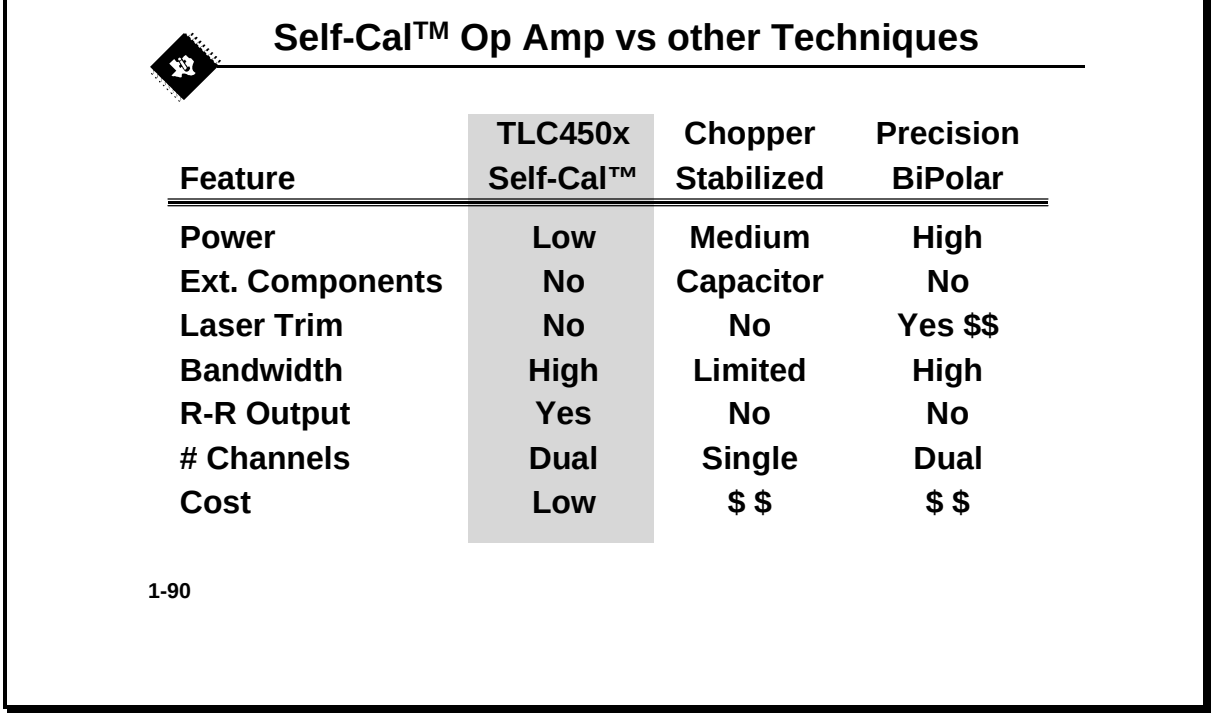


TLC4501/2 Self-Calibrating (Self-Cal™) CMOS Op Amp

Texas Instruments has introduced the CMOS operational amplifier TLC4501 and TLC4502 which integrate a new self-calibrating (Self-Cal™) technology. This technology allows a compensation of the input offset voltage down to a value of 40 μV maximum for the TLC4501A. This gives a big improvement in comparison with the standard CMOS op amps, which have typically an input offset voltage of around 1 mV. The picture shows the block diagram of this self-calibrating op amp. After power-up, the differential inputs of the TLC4501/2 are connected to each other, so that the inputs are disconnected from the real input and the differential voltage is forced to zero. This self-calibrating feature requires typically 300 ms. The voltage at the output of the op amp is, during this time, connected to an A/D converter, which converts the input offset voltage of the op amp into a digital format. The input offset cancellation uses a current-mode D/A converter, whose full-scale output allows for an adjustment of approximately ± 5 mV to the input offset voltage.

The performance of the TLC4501 and TLC4502 in terms of input offset voltage is:

Op Amp	TLC4501	TLC4501A	TLC4502	TLC4502A
V_{IO}	± 80 μV	± 40 μV	± 100 μV	± 50 μV



Self-Cal™ Op Amp vs other Techniques

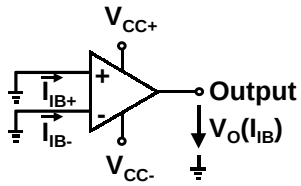
While chopper op amps and some precision bipolar op amps can achieve lower input offset voltages than the Self-Cal amplifier, the TLC4501/2 offers significant advantages over both:

Chopper amplifiers suffer from bandwidths limited by the chopping frequency. They also introduce switching noise onto the signal and the ground plane. The TLC4501 and the TLC4502 have no chopping circuitry. Furthermore, choppers typically require external storage capacitors and are generally expensive.

High precision bipolar op amps lack the high impedance inputs preferred for sensing very small signals from high impedance sensors. High input currents lead to dc errors when large resistance's are used. Furthermore, bipolar op amps tend to consume more power.

The TLC4501/2 CMOS architecture doesn‘t show these disadvantages. Moreover, the TLC4501/2 require no laser trimming and are therefore less expensive than high precision bipolar amplifiers.

Input Bias Current (I_{IB})



Parameter	Technology		
	TLE2037I (BIPOLAR)	TLE2071 (BiFET)	TLC2201 (CMOS)
I_{IB}(typ, 25°C)	15 nA	20 pA	1 pA
I_{IB}(max, 25°C)	90 nA	175 pA	
I_{IB}(max)	150 nA	5 nA	150 pA
$\frac{\Delta I_{IB}}{\Delta T}$	Fairly Stable over tempe-rature	Double for every 10°C increase	Double for every 10°C increase

$$I_{IB} = \frac{I_{IB+} + I_{IB-}}{2}$$

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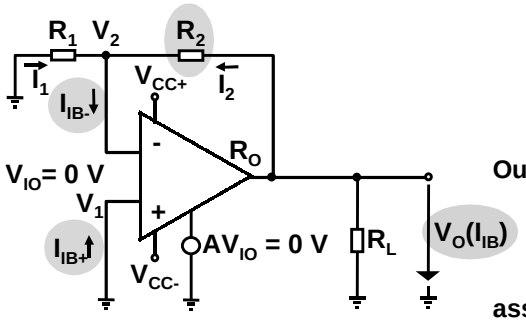
Input Bias Current

The input bias current I_{IB} is defined as the average of the currents I_{IB+} and I_{IB-} into the two input terminals, as shown in the picture. I_{IB+} is here the current into the noninverting input and I_{IB-} is the current into the inverting input. These currents are the bias currents of the input transistors of the differential amplifier.

Bipolar op amps have typically a very high input bias current of several hundred nano-amperes compared to BiFET and CMOS op amps. This is the reason why bipolar op amps are not well suited for high impedance applications. BiFET and CMOS op amps have a very high input impedance and therefore a very low input bias current of typically around 1 pA or even less at a temperature of 25°C. This makes the BiFET and CMOS op amps ideal for high impedance applications. However, the input bias current doubles for every 10°C increase in temperature, which may cause a significant output offset voltage, if the op amp is used in a high temperature environment with a large feedback resistor.

The following page shows the impact of the input bias current on the output offset voltage.

Output Offset Voltage



$$V_2 = I_{IB} \times \frac{R_1 \times R_2}{R_1 + R_2}$$

Output offset voltage $V_O(I_{IB})$:

$$V_O(I_{IB}) = R_2 \times I_{IB}$$

assuming that $I_{IB-} = I_{IB+} = I_{IB}$

☛ Input bias current can cause an output offset voltage.

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Output Offset Voltage caused by the Input Bias Current

The input bias current of an op amp may cause an output offset voltage at the output, if the input bias current is not compensated. The circuit shows an op amp in the inverting or noninverting configuration. The equation for the output offset voltage V_{IOB}, which is caused by the input bias current of an op amp in the inverting or noninverting configuration, will be derived. For the calculation of the voltage V_{IOB}, the input offset voltage V_{IO} is assumed to be zero. The currents I_{IB-} and I_{IB+} are flowing into the inverting and noninverting inputs of the op amp. Since the noninverting input is connected to ground, the voltage $V_1 = 0$. The output resistance R_O of the op amp is very small and can therefore be neglected. Because of that the resistors R_1 and R_2 can be seen in parallel. The voltage V_2 can now be calculated as follows: $V_2 = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$

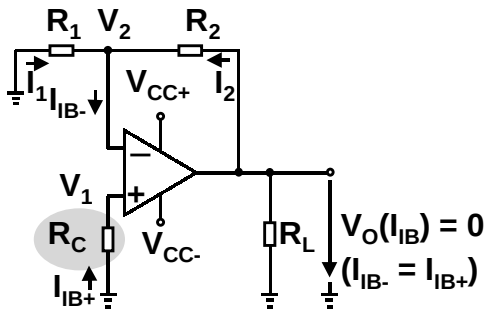
Considering the node at V_2, it can be written: $I_1 + I_2 = I_{IB-}$, or

$$\frac{0 - V_2}{R_1} + \frac{V_O(I_{IB}) - V_2}{R_2} = I_{IB-}$$

This results in: $$V_O(I_{IB}) = V_2 \times (1 + \frac{R_1}{R_2}) + R_2 \times I_{IB-}$$

The differential voltage between the two input terminals is ideally 0. V2 is therefore 0, since V1 = 0. The equation results into the output offset voltage caused by the input bias current by assuming that $I_{IB} = I_{IB-} = I_{IB+}$: $\boxed{V_O(I_{IB}) = R_2 \times I_{IB}}$

Input Bias Current Compensation



Compensation Resistor R_C

$$R_C = \frac{R_1 \times R_2}{R_1 + R_2}$$

The input bias current is compensated if $V_1 = V_2$

1-93

Compensation of the Input Bias Current

The effect of the input bias current can be compensated, if the voltage drop V_2 at the inverting and the voltage drop V_1 at the noninverting input of the op amp are equal. As already described before, the voltage V_2 can be calculated as follows:

$$V_2 = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$$

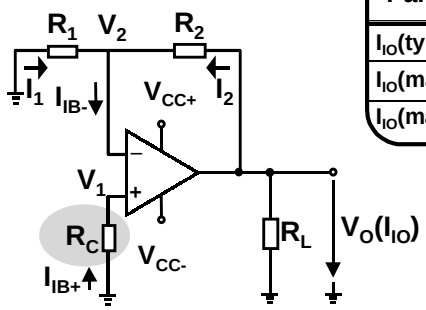
Under the assumption that the input bias current I_B is equal as well to the bias current flowing into the noninverting input (I_{IB+}) as to the bias current flowing into the inverting input (I_{IB-}), the compensation resistor R_C can be calculated as follows:

$$R_C = \frac{R_1 \times R_2}{R_1 + R_2}$$

The resulting voltage V_1 is under these conditions equal to the voltage V_2.

$$V_1 = R_C \times I_{IB+} = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$$

Input Offset Current (I_{IO})



Parameter	Technology		
	TLE2037 (BIPOLAR)	TLE2071 (BiFET)	TLC2201 (CMOS)
I_{IO}(typ, 25°C)	6 nA	15 pA	0.5 pA
I_{IO}(max, 25°C)	90 nA	100 pA	
I_{IO}(max)	150 nA	1.4 nA	150 pA

Input Offset Current I_{IO}:

$$I_{IO} = | I_{IB+} - I_{IB-} |$$

Output Offset Voltage caused by I_{IO}:

$$V_O(I_{IO}) = R_2 \times I_{IO}$$

1-94

Input Offset Current

We have seen before, that the resistor R_C is used for compensating the input bias current of the op amp. A complete compensation is only possible, if the individual input bias currents into the terminals of the op amp are equal. In practice, this won‘t be the case. The maximum difference between the input bias currents I_{IB+} and I_{IB-} is called the Input Offset Current, which is defined as follows:

$$I_{IO} = |I_{IB+} - I_{IB-}|$$

The output offset voltage V_{OIIO} caused by the input offset current can be calculated by applying the superposition theorem. The output offset voltage caused by the voltage V_2 is: $V_O(I_{IB-}) = -R_2 \times (I_{IB-})$

The output offset voltage caused by the voltage V_1 is:

$$V_O(I_{IB+}) = V_1 \times (1 + \frac{R_2}{R_1})$$

With:

$$V_1 = R_C \times (I_{IB+}) = \frac{R_1 \times R_2}{R_1 + R_2} \times (I_{IB+})$$

The equation for V_{OIB1} results in:

$$V_O(I_{IB+}) = R_2 \times (I_{IB+})$$

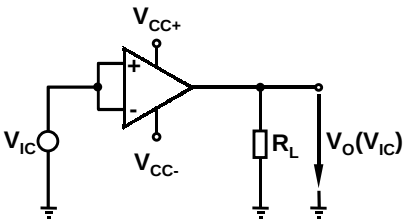
The maximum output offset voltage caused by the input offset current can then be calculated by addition of $V_O(I_{IB+})$ and $V_O(I_{IB-})$:

$$V_O(I_{IB+}) + V_O(I_{IB-}) = R_2 \times (I_{IB+}) - R_2 \times (I_{IB-}) = R_2((I_{IB+}) - (I_{IB-}))$$

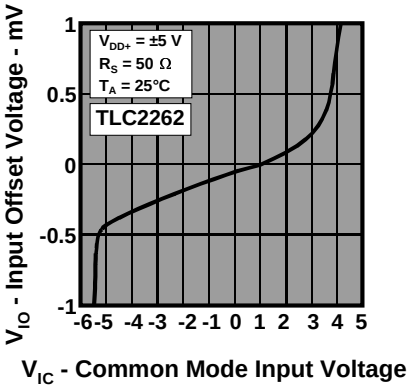
$$V_O(I_{IO}) = R_2 \times I_{IO}$$

Here again as for the input bias current, the amount of output offset voltage caused by the input offset current is determined by the feedback resistor R_2. The input offset current is typically smaller than the input bias current. Therefore the output offset which is caused by the input offset current should be smaller then the output offset voltage caused by the input bias current.

Common-Mode Rejection Ratio (CMRR)



$$CMRR(dB) = 20 \times \log \frac{\Delta V_{IC}}{\Delta V_{IO}}$$



☛ **Remember: If CMRR = 80 dB and ΔV_{IC} = 1 V, then ΔV_{IO} = 100 µV**

1-95

Common-Mode Rejection Ratio

The common-mode rejection ratio of an ideal op amp is infinite. However in practice, a real op amp produces a small voltage at the output, if a common-mode voltage is applied to the inputs as shown in the picture. The capability to reject the common-mode voltage is called the common-mode rejection ratio, which is defined as follows:

$$CMRR = 20 \times \log \frac{\Delta V_{IC}}{\Delta V_{IO}}$$

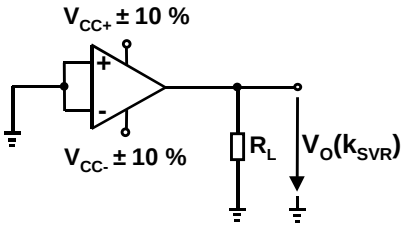
For an op amp with a common-mode rejection ratio of 80 dB, we get:

$$\frac{\Delta V_{IC}}{\Delta V_{IO}} = 10^4 .$$

This means that a change of the common-mode input voltage of 1V causes a change in the input offset voltage of 100 µV.

Important to mention is that inverting amplifier do not suffer from common-mode rejection ration effects. This is because the amplifier inputs are permanently at ground for dual supply applications or half the supply voltage in single supply applications. The non-inverting amplifier configuration has a common-mode voltage equal to the input signal.

Supply Voltage Rejection Ratio (k_{SVR})



$$k_{SVR} = 20 \times \log \frac{\Delta V_{CC\pm}}{\Delta V_{IO}}$$

$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{\frac{k_{SVR}}{10^{20}}}$$

Example: TLC4501 with a typical k_{SVR} of 100 dB

$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{\frac{100}{10^{20}}} = 10\ \mu V/V$$

1-96

Supply Voltage Rejection Ratio

The supply voltage rejection ratio k_{SVR} of an op amp indicates how a change in the supply voltage influences the input offset voltage V_{IO}. The change in the supply voltage may be caused by a poor supply voltage regulation or a bad supply voltage filtering. The value k_{SVR} is usually given in dB and we can say:

$$k_{SVR} = 20 \times \log \frac{\Delta V_{CC\pm}}{\Delta V_{IO}}$$

Rearranging this equation, we get:

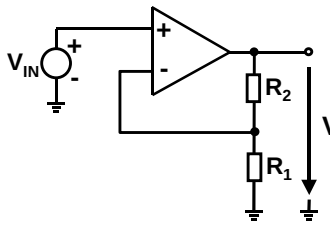
$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{10^{\frac{k_{SVR}}{20}}}$$

This results as an example for the TLV2262A with a k_{SVR} of typically 100 dB in:

$$\frac{\Delta V_{IO}}{\Delta V_{DD\pm}} = \frac{1}{10^{\frac{100}{20}}} = 10\,\frac{\mu V}{V}$$

In a battery powered system with a supply voltage of V_{DD} = 3 V, it is possible that the supply voltage may vary up to ± 10 %. This results into a supply voltage range from 2.7 V up to 3.3 V. With a supply voltage rejection ratio of 100 dB, the change in the input offset voltage is 3 μV. Considering the minimum supply voltage rejection ratio of 80 dB, we get the maximum change in the input offset voltage of 30 μV.

Total DC Error Non-inverting Amplifier



- Input Bias Current
- Input Offset Current
- Common Mode Rejection Ratio
- Supply Voltage Rejection Ratio

$$V_O = \left(1 + \frac{R_2}{R_1}\right)\left[V_{IN} + V_{IO} + \alpha_{VIO} \times \Delta T + I_{IB} \times \left(\frac{R_2}{1 + \frac{R_2}{R_1}}\right) + \frac{V_{IC}}{CMRR} + \frac{\Delta V_{CC}}{k_{SVR}}\right] \times \frac{1}{1 + \frac{1}{A_{VD}}\left(1 + \frac{R_2}{R_1}\right)}$$

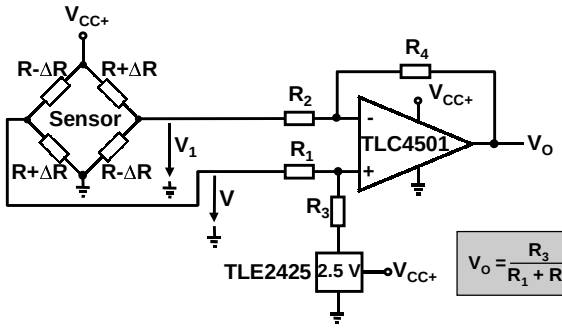
Noise and input offset voltage long-term drift neglected

1-97

Total DC Error Noninverting Amplifier

The picture shows an example of a DC error consideration for an op amp which operates as a noninverting amplifier. All the error terms in a DC application which were covered before, are summarised in an equation.

Precision Single Supply Differential Amplifier



$$V_O = \frac{R_3}{R_1 + R_3} \times \left(1 + \frac{R_4}{R_2}\right) \times V_1 - \frac{R_4}{R_2} \times V_2 + 2.5\ V$$

- **Single supply operation**
- **TLC4501 Self-Cal™ amplifier**
- **TLE2425 virtual ground reference**

for $\frac{R_4}{R_2} = \frac{R_3}{R_1}$: $V_O = \frac{R_3}{R_1} \times (V_1 - V_2) + 2.5\ V$

1-98

Precision Single Supply Differential Amplifier

This is the classic differential amplifier (subtractor) in a single supply environment and its the simplest way to measure and amplify the potential difference across the bridge diagonal of a Wheatstone Bridge.

This amplifier is a combination of a non-inverting and an inverting amplifier. The op amp is dc-biased with half the supply voltage at the non-inverting input because of the single supply operation, and therefore allows a maximum symmetrical voltage swing at the output. The "TLE2425 Virtual Ground Generator" is the ideal device since it generates exactly the reference voltage VREF = 2.5 V from a voltage in the range of 4 - 40 V. The voltage at the output of the op amp can be calculated as follows:

$$V_O = \frac{R_3}{R_1 + R_3} \times \left(1 + \frac{R_4}{R_2}\right) \times V_1 - \frac{R_4}{R_2} \times V_2 + V_{REF}\,.$$

If the resistors are chosen so

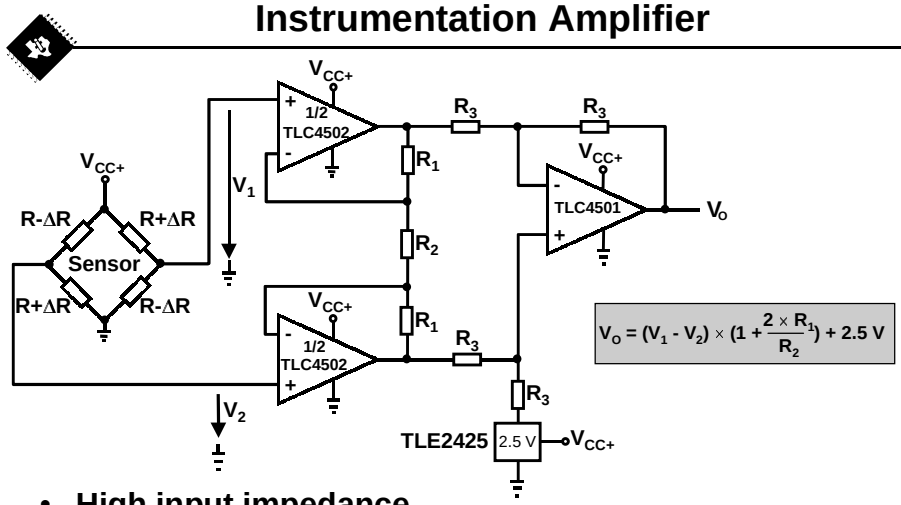
$$\frac{R_4}{R_2} = \frac{R_3}{R_1}\,,$$

an easy practical result is obtained

$$V_O = \frac{R_3}{R_1} \times (V_1 - V_2) + V_{REF}\,,$$

since for an input voltage of V_1=V_2, the output of the op amp delivers theoretically exactly the middle voltage V_O = 2.5 V.

The disadvantages of this circuit are that its input impedance is unbalanced and the common mode rejection is modified by the source impedances. This circuit is therefore not recommended for high impedance sources. The common mode rejection of the TLC4501 is typically 100 dB. This means that an increase of 1 V in the common mode voltage is similar to a differential voltage between the inputs of 10 μV. More important is that the Common Mode Rejection is also driven by resistor tolerances. A high accuracy in the resistor values is therefore absolutely required.

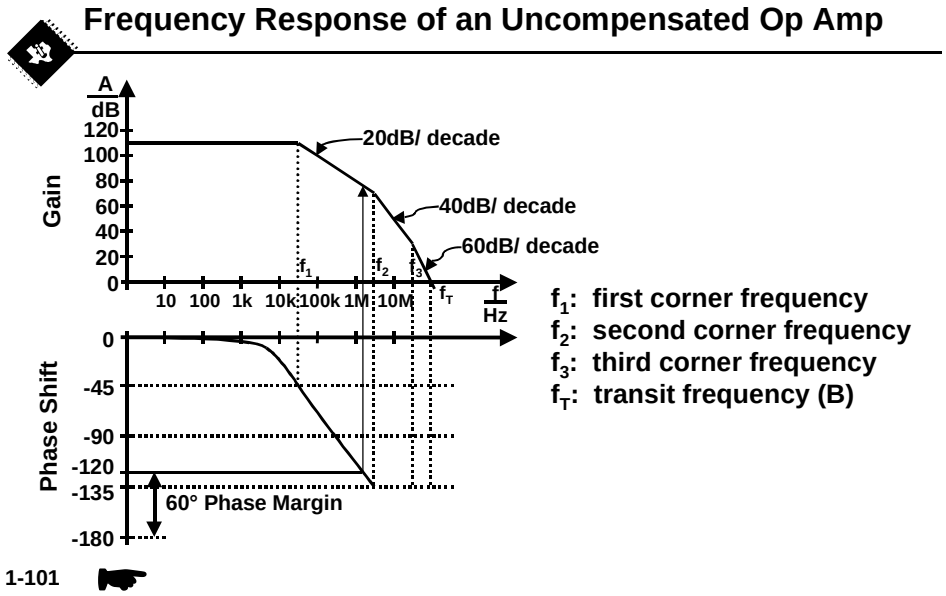


Instrumentation Amplifier

A very high input impedance can be achieved by using an instrumentation amplifier. Such an amplifier consists of three op amps. The differential amplifier discussed before can be found again with a gain of 1, because all resistors are the same. Two further op amps are connected in the front of this differential amplifier to provide now the very high input impedance which is only determined by the op amp input impedance. The source which is connected to the instrumentation amplifier is in this case only loaded by the high input impedance of the CMOS op amp TLC4501 which is typical 10^{12}. The gain is adjusted by the resistor R_2. The output voltage can be calculated as follows

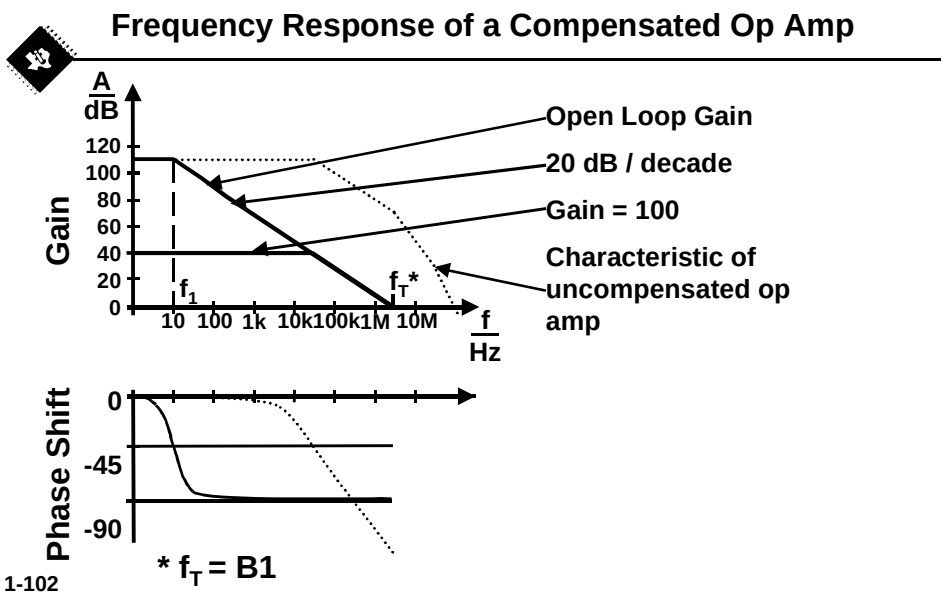
$$V_O = (V_2 - V_1) \times (1 + \frac{2 \times R_1}{R_2}) + V_{REF}.$$

Again, also in this circuit it is very important to select the resistors R_3 with a high accuracy relative to each other to achieve high common mode rejection. This can be achieved with a resistor array network for R_3, where the relative accuracy is very good (value in the region of 10 kΩ). The absolute accuracy of the resistors R_3 is not as important.



Frequency Response of an Uncompensated Op Amp

An operational amplifier behaves, because of internal stages and parasitic capacitances, as a low-pass filter of a higher order. The figure shows the typical frequency response. The differential gain and the phase shift between input and output are a function of the frequency. The gain is constant up to the first break frequency f_1. At this point the gain has decreased by 3 dB and the phase shift between input and output of the op amp has increased to -45°. For frequencies above f_1 the amplitude decreases with 20 dB per decade until the second break frequency f_2. If the frequencies f_1 and f_2 are far enough apart, the phase shift caused by the first low-pass filter is -90°, the phase shift caused by the second low-pass filter is -45°, which results into a phase shift of -135° at frequency f_2. Beginning from f_2, the amplitude decreases with 40 dB per decade, till the edge frequency of the third low-pass filter is reached. The phase shift at f_3 between input and output is now -180°, under the assumption that the frequencies f_2 and f_3 are far enough apart. This is the point where the inverting and the noninverting input of the op amp swap their roles. The feedback which is fed to the inverting input, expected as a negative feedback, has now become positive and may influence the circuitry to oscillate. To avoid oscillation, a phase margin is required. If the gain $|A_{VD}| > 1$, the phase margin should be at least -60°, which means that the phase shift between input and output is not higher than around -120°. This results for the depicted frequency response into a minimum gain of 75 to 80 dB and a restricted bandwidth.



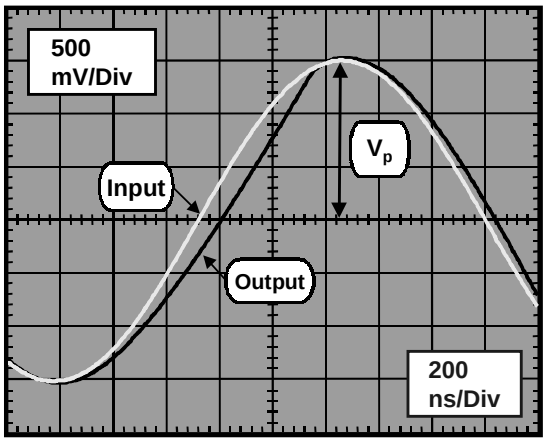
Frequency Response of a Compensated Op Amp

An operational amplifier which has to be used universally must have a phase shift between input and output which is less than around 120° while having a closed loop gain greater or equal to 1. This can be achieved if the frequency response of the op amp over the usable frequency range is compensated so that the frequency response is similar to a first order low-pass filter. The undesired low-pass filter, which was discussed before, cannot be avoided and remains at the same frequency. However, the break frequency f_1 can be decreased by adding a compensation capacitor inside the op amp that the gain A reaches the value 1 before the second low-pass filter causes a phase shift of -180° between input and output. Since the break frequency f1 has decreased, the available bandwidth is lower compared to a decompensated op amp. This is the reason that some high bandwidth op amps (e.g. the TLE2037) are not compensated. The picture shows an op amp which can be used universally since the phase shift between input and output is 90° at a closed loop gain of 1. It shows also the available bandwidth at a gain of 100 and at open loop gain. It is clear that the available bandwidth decreases with an increasing gain.

Limited Slew Rate Distortion

$SR_{min} = 2 \times \pi \times f \times V_p$

Example:
SR of 3.45 V/µs
output swing V_p of 1.5 V
f_{max} = 366 kHz



Result with f_{in} = 460 kHz

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Distortion caused by limited Slew Rate

The basic bandwidth of an operational amplifier is specified as the unity-gain bandwidth. This unity-gain bandwidth is the range of frequencies within which the maximum output voltage swing is above a specified value. However, this bandwidth can only be used for **small signals** which are in the range of **mV** or **µV**. If large-signals in the range of **several volts** up to the supply voltage are considered, the slew rate is the determining factor of the maximum signal frequency. The measurement shows the input and output voltages of an op amp which operates as a voltage follower. The input voltage is a sine wave. The equation for the output voltage without distortion is:

$$v(t) = V_P \times \sin \omega t$$

The slope of this sine signal is: $\frac{dv}{dt} = V_P \times \omega \cos \omega t$

The maximum slope occurs when $\cos \omega t = 1$, or at the zero-axis crossing of the sine signal. If the slew rate of the op amp is set to the maximum slope of the signal, the following equation is obtained:

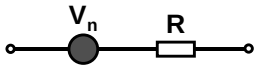
$$SR = \frac{dv}{dt}\Big|_{max} = V_P \times \omega$$

This equation gives the minimum required slew rate of the op amp for a desired output magnitude and signal frequency to get an output signal without distortion in terms of Transient Intermodulation (TIM). The example shows the effect of

slew rate, which is too slow. The maximum signal frequency in that example is 366 kHz with a given slew rate of 3.45 V/μs and a signal magnitude of 1.5 V. The measurement shows the result with a signal frequency of 460 kHz. It can be seen that the output of the op amp is not able to follow the input signal, especially at the zero-axis crossing. At the minimum and at the maximum amplitude where the sine wave has the lowest slope, the output is able to follow the input signal.

Thermal Noise (Johnson Noise)

Thermal noise is caused by free electrons which move randomly in a resistive material.



$$V_n = \sqrt{4 \times k \times T \times \Delta f \times R}$$

where:
k is Boltzmann's Constant (1.374×10^{-3} J/°K)
T is the absolute temperature in degrees Kelvin
Δf is the bandwidth in Hz
R is the resistance in Ω

Rule of thumb:
The noise contribution of a 1 kΩ resistor at 25°C in a 1 Hz bandwidth will generate 4 nV rms noise.

1-104

Thermal Noise (Johnson Noise)

Thermal Noise is generated when thermal energy causes free electrons to move randomly in a resistive material. Capacitances and inductances don‘t show this thermal noise except in the thermal noise of the parasitic resistances. The phenomenon of thermal noise was discovered by Schottky in 1928 and measured and evaluated by Johnson in the same year and it is therefore also referred to as Johnson noise. The rms thermal noise across an open-circuit resistor is given by: $V_n = \sqrt{4kT\Delta fR}$,

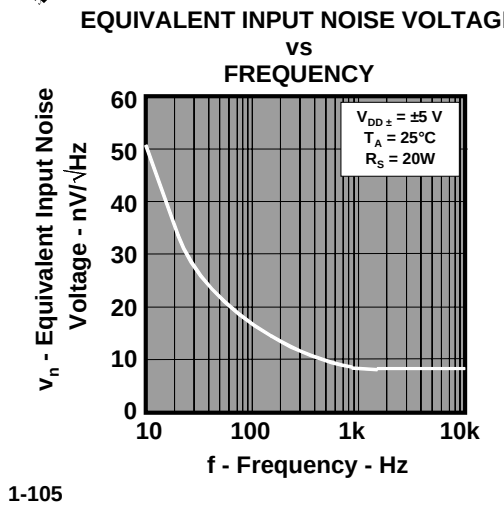
where k is the Boltzmann‘s constant, R the resistance, Δ f the bandwidth over which the noise is measured and T is the absolute temperature in degree Kelvin.

The generated noise voltage up to high frequencies is independent of the frequency. Therefore the thermal noise is also referred to as white noise in analogy with the spectrum of white light which has also a flat power distribution in the optical frequency range.

Therefore, the power in thermal noise is proportional to the square of V_n, which is independent of the frequency for a fixed bandwidth. The power between 20 Hz and 20 kHz is the same as the power between 10.020 kHz and 30 kHz.

The noise contribution of a 1 kΩ resistor at 25°C in a 1 Hz bandwidth will generate 4 nV rms noise. With a bandwidth of 1 kHz, the thermal noise increases to: $4\ \text{nV} \times \frac{\sqrt{1000\text{Hz}}}{\sqrt{\text{Hz}}} = 126\ \text{nV}$.

Op Amp Noise (TLC2272)



Typ. Noise Parameter @ 25°C (TLC2272):

V_n (f = 10 Hz): 50 nV/√Hz

V_n (f = 1 kHz): 9 nV/√ Hz

V_{NPP} (f = 0.1 Hz to 1 Hz): 1 µV

V_{NPP} (f = 0.1 Hz to 10 Hz): 1.4 µV

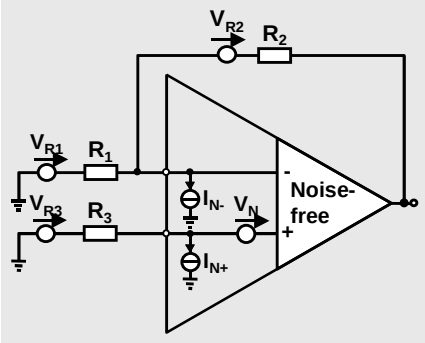
I_N: 0.6 fA/√ Hz

Op Amp Noise (TLC2272)

An op amp shows different kinds of noise phenomena. These are the Schottky noise (current noise), thermal noise (voltage noise) and flicker noise. The Schottky noise is associated with the current flowing through a pn junction. Voltage noise is generated both by ohmic resistances in the op amp, and also by the effect of the current noise on the resistors in the op amp circuitry. An example of this is shown on the next page. This noise is for most of the frequency operating area white noise. This means that the noise level up to high frequencies is independent of the frequency and remains at the same amplitude (also referred to as “white noise“. For the TLC2272 it can be seen that above 1 kHz the voltage noise stays at around 9 nV/√Hz. However, at lower frequencies in the region of 10 Hz up to some hundred Hz, the noise level is higher. This increase is caused by the flicker noise, which is only dominant in the low-frequency area and is inversely proportional to the frequency. The flicker noise is

therefore referred to as 1/f noise and is also called „pink“ noise. This phenomena is visible in the shown noise diagram for the TLC2272.

Calculating the Noise at the Output of an Op Amp



Noise of each source individually:

V_{N1}: Op amp voltage noise: $V_N \times (1 + \frac{R_2}{R_1})$

V_{N2}: Op amp current noise (I_N): (I_{N-}) × R_2

V_{N3}: Op amp current noise (I_{N+}): (I_{N+}) × R_3 × $(1 + \frac{R_2}{R_1})$

V_{N4}: Johnson noise R_1: $\sqrt{4kT\Delta fR_1} \times (-\frac{R_2}{R_1})$

V_{N5}: Johnson noise R_2: $\sqrt{4kT\Delta fR_2}$

V_{N6}: Johnson noise R_3: $\sqrt{4kT\Delta fR_3} \times (1 + \frac{R_2}{R_1})$

$$V_{NT} = \sqrt{(V_{N1})^2 + (V_{N2})^2 + (V_{N3})^2 + (V_{N4})^2 + (V_{N5})^2 + (V_{N6})^2}$$

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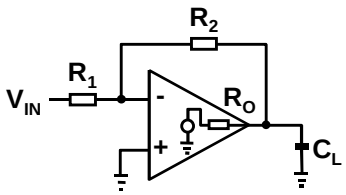
Calculating the Noise at the Output of an Op Amp

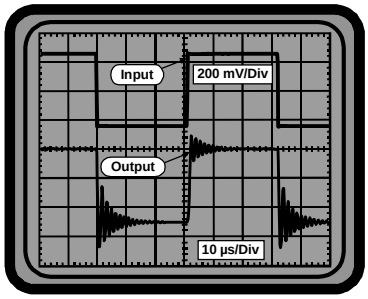
The picture shows an example where the noise at the output of an op amp is calculated. The op amp circuit which is investigated can be considered as an inverting or non-inverting amplifier, but without having a signal source. Six different noise sources have to be taken into account in this example, which generate a noise voltage at the output of the op amp. These are the three op amp noise sources (voltage noise, current noise I_{N+}, I_{N-}) and the thermal noise of each resistor used. Each noise source has a specific transmission factor to the output of the op amp.

The op amp voltage noise is amplified with the factor $(1 + R_2/R_1)$, because this voltage is applied at the non-inverting input of the amplifier. The noise current I_{N+} flows through the resistor R_3 and generates a voltage ($I_{N+} \times R_3$) at the non-inverting input. This voltage is also amplified with the factor $(1 + R_2/R_1)$. Therefore the output voltage caused by I_{N+} is: $(I_{N+} \times R_3) \times (1 + R_2/R_1)$. The noise current I_{N-} generates the voltage $I_{N-} \times R_2$ which is transmitted with factor 1 to the output of the op amp. The thermal noise caused by R_1 ($\sqrt{4kT\Delta fR_1}$) is amplified with the factor $-R_2/R_1$ (inverting amplifier). The thermal noise caused by R_3 ($\sqrt{4kT\Delta fR_3}$) is amplified with the factor $(1 + R_2/R_1)$ (non-inverting amplifier). The thermal noise caused by R_2 ($\sqrt{4kT\Delta fR_2}$) is applied directly at the output of the op amp. It is important to mention here that the resulting noise is not the arithmetic

sum of all noise sources. The resulting noise at the output of the op amp is the root of the sum of their squares as shown in the picture above.

Driving a Capacitive Load





* **Measurement with a TLC272 operating as a voltage-follower with a 220 pF capacitive load.**

A capacitive load creates in combination with the output impedance R_O of the op amp a low-pass filter. A further phase shift in addition to the op amp's phase shift is caused and the phase margin is reduced.

1-107

Driving a Capacitive Load

Problems in terms of stability are often caused either by bad bypassing or by a capacitive load which the op amp has to drive, whether or not this is desired. Even the trace capacitance of a printed circuit board, which may be in the range of 0.5 to 1 pF/cm may increase the settling times for amplifiers which are designed to handle capacitive loads of around 100 pF. The capacitive load at the output of the op amp creates a low pass filter with the output resistance R_O. The break frequency depends on R_O and C_L and can be calculated as follows:

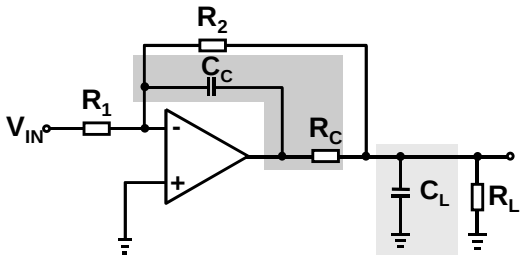
$$f_c = \frac{1}{2\pi R_o C_L}$$

This low-pass filter causes a phase shift in addition to the op amp‘s phase shift. The phase shift is given by:

$$\varphi = -\arctan \varpi R_O C_L$$

The phase margin is therefore reduced and at frequencies where the phase shift of the op amp and the low-pass filter is each 90°, the negative feedback becomes a positive feedback. This results into oscillation at the output of the op amp which can also be seen in the measurement.

Lead Compensation of Capacitive Load



☛ **The capacitor C_C in parallel to the feedback resistor causes a phase lead and can therefore compensate for the phase lag caused by the capacitive load C_L.**

1-108

Lead Compensation of Capacitive Load

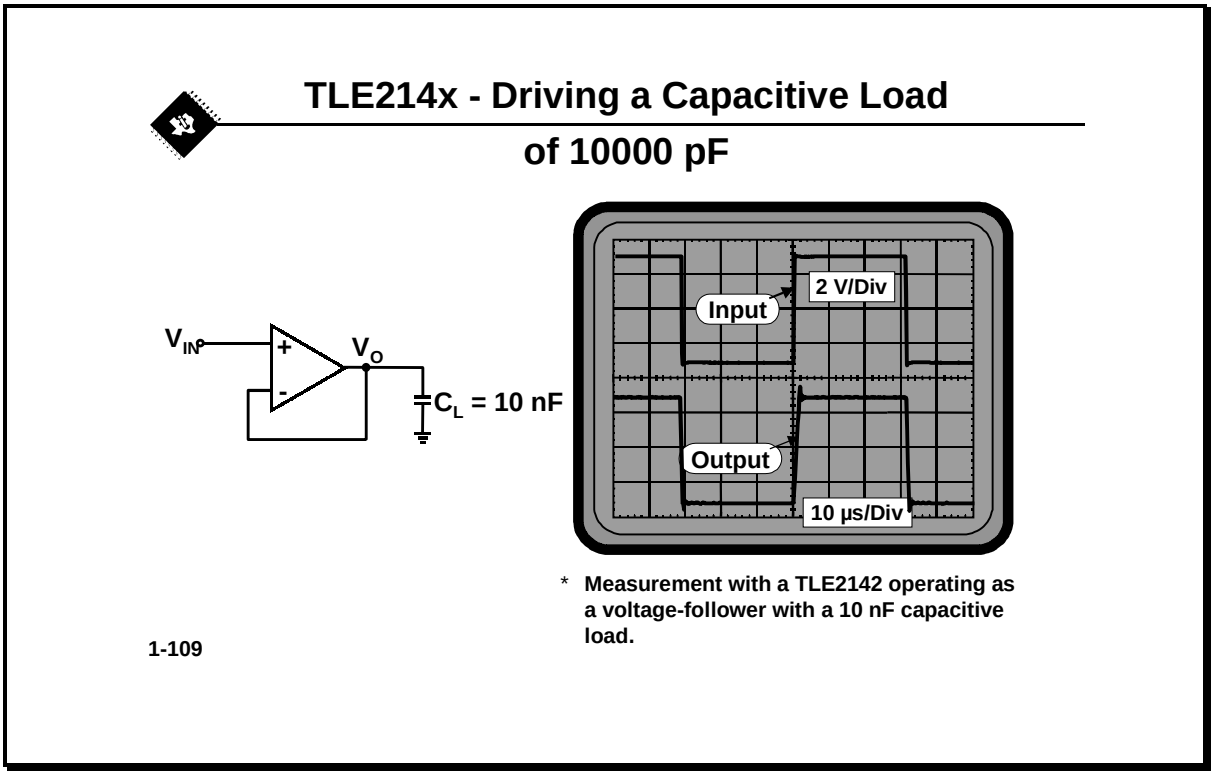
A popular technique to reduce the oscillation caused by a capacitive load is the lead compensation of the capacitive load. The phase lag caused by the capacitive load C_L can be compensated for by a small capacitor C_C in parallel with the feedback resistor in order to provide a phase lead at the input of the op amp. It is possible to neutralise the phase lag which is caused by C_L. The required phase lead can be generated with C_C. The equation for a neutral compensation are:

$$R_C = \frac{R_1 \times R_2}{R_1 + R_2} \times R_O$$

and

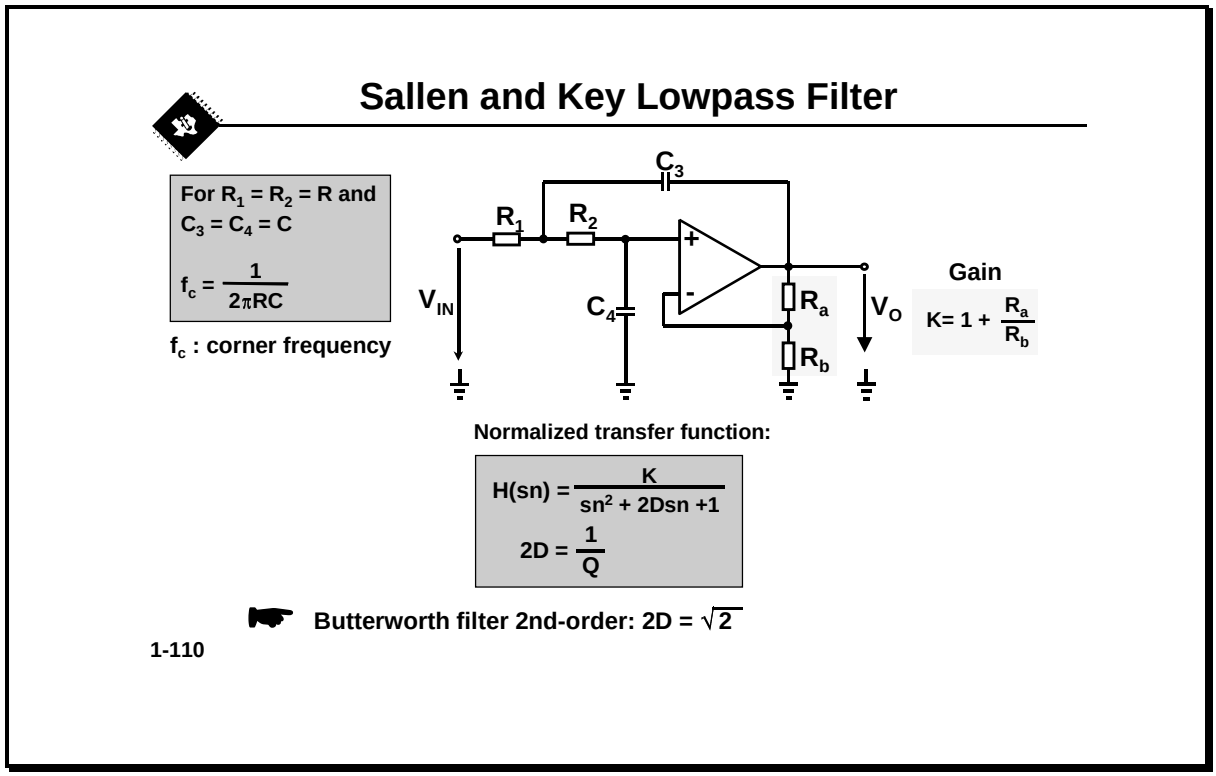
$$C_C = (1 + \frac{R_1 \times R_2}{R_1 + R_2})^2 \times \frac{R_O \times R_2}{R_O + R_2} C_L$$

In most cases a small isolating resistor (30 – 100 Ω) between the amplifier feedback and the capacitive load is sufficient in order to reduce the oscillation at the output of the op amp.



TLE214x – Driving a Capacitive Load of 10000 pF

The TLE214x op amp family is especially designed to be able to drive a higher capacitive load. The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. Therefore, this family is suitable for direct buffering of longer cables.



Sallen and Key Lowpass filter

Active filters are built up from op amps with resistive and capacitive components. Sallen and Key circuit technology, as shown in the picture, can be used to implement all types of filters. Active filters have many advantages over R-L-C filters especially at low frequencies where the elimination of large inductors improves filter performance while reducing costs. Other advantages are greater response accuracy and the ability to provide circuit gain. Designing active filters means choosing a filter shape that satisfies the requirements in terms of amplitude, phase and transient response. It is basically only possible to optimise one of these parameters while for the other a compromise has to be found. A Butterworth filter is often the best overall choice because it has the flattest passband and proceeds smoothly from the passband, without ripple, through the cut-off frequency fc at –3 dB into the stop band with a decrease in the amplitude of 40 dB/decade. The normalised equation for a 2nd order lowpass filter is:

$$H(sn) = \frac{K}{sn^2 + 2Dsn + 1} = \frac{K}{\left(\frac{s}{\omega_B}\right)^2 + 2D\frac{s}{\omega_B} + 1}$$, where 2D = 1/Q.

It is possible to select the center frequency, the damping D and its inverse Q. Damping, or Q, sets the peaking or drop of the response near the cutoff frequency. The normalised equation for a Butterworth 2nd order filter is:

$$H(sn) = \frac{K}{\left(\frac{s}{\omega_B}\right)^2 + \sqrt{2}\frac{s}{\omega_B} + 1} \qquad (1)$$

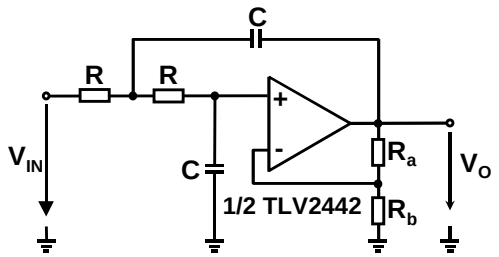
The transfer function of the Sallen and Key circuit results in:

$$H(s) = \frac{K}{s^2 R_1 R_2 C_3 C_4 + s\left[C_4(R_1 + R_2) + R_1 C_3(1 - K)\right] + 1} \qquad (2)$$

From (1) and (2) we get: $\frac{1}{\omega_B} = R_1 R_2 C_3 C_4$ and $\frac{\sqrt{2}}{\omega_B} = C_3 C_4 (R_1 + R_2) + R_1 C_3 (1 - K)$.

Filter for Telecom Application

- Butterworth 2nd Order -



f_c = 4 kHz
K = 1.586
R = 5 kΩ
C = 7.96 nF

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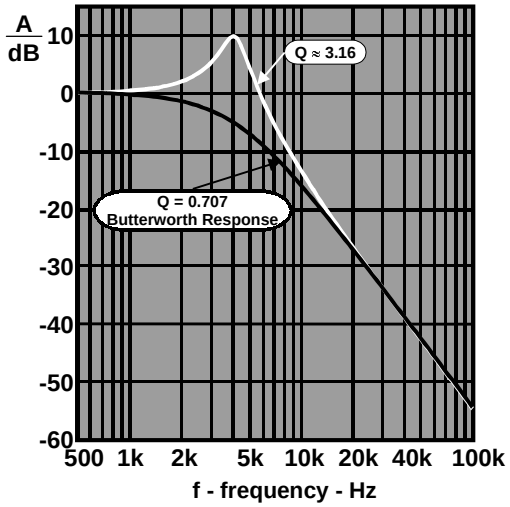
Filter for Telecom Application - Butterworth 2nd Order -

An example for a lowpass filter with a cutoff frequency of 4 kHz (telecom application) is considered with the condition: R1=R2=R, C3=C4=C, ωB=ωC and R=5kΩ. The cutoff frequency is simply: $f_C = \frac{1}{2\pi RC}$. The gain K results into: $\sqrt{2}RC = 3RC - KRC$, therefore K=1.586. With R=5kΩ, C can now be calculated: $C = \frac{1}{R\omega_C} = 7.96\,\text{nF}$.

The op amp used in active filters has to be chosen carefully, because the gain-bandwidth and the slew rate will limit the accuracy and highest frequency of operation for a given filter realisation. As the filter gain-cut-off frequency product approaches the op amp gain bandwidth product the accuracy of the cut-off frequency will be reduced. To limit these effects the closed loop gain of the op amp gain should be at least 10 times higher than the cut-off frequency of the filter. The slew rate limits the large signal bandwidth and can affect stability with increasing amplitude because of the additional phase shift introduced when the signal is close to the slew limit. The TLV2442 fits this application ideally

Responses of 2nd-order filter



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Responses of 2nd order Filter

The graph shows the frequency response of the circuit which was shown on the page before. Two characteristics, the Butterworth frequency response (Q = 0.707) and the a Q of 3.16, were measured. The Butterworth characteristic shows it has the flattest passband and proceeds smoothly from the passband, without ripple, through the cut-off frequency fc at –3 dB into the stop band with a decrease in the amplitude of 40 dB/decade.

Absolute Maximum Ratings (TLC227x)

Supply voltage V_{DD+} (see Note 1)		8 V
Supply voltage V_{DD-} (see Note 1)		-8 V
Differential input voltage, V_{ID} (see Note 2)		±16 V
Input voltage, V_I (any input, see Note 1)		V_{DD-} -0.3 V to V_{DD+}
Input current, I_I (any input)		±5 mA
Output current, I_O		±50 mA
Total current into V_{DD+}		±50 mA
Total current out of V_{DD-}		±50 mA
Duration of short-circuit current at (or below) 25° C (see Note 3)		unlimited
Continuous total dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A:	C suffix	0° C to 70° C
	I suffix	-40° C to 85° C
	M suffix	-55° C to 125° C
Storage temperature range		-65° C to 150° C
Lead temperature 1.6 mm from case for 10 seconds		260° C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operation conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

Notes: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN-. Excessive current will flow if input is brought below V_{DD-} - 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltage must be limited to ensure that the maximum dissipation rating is not exceeded.

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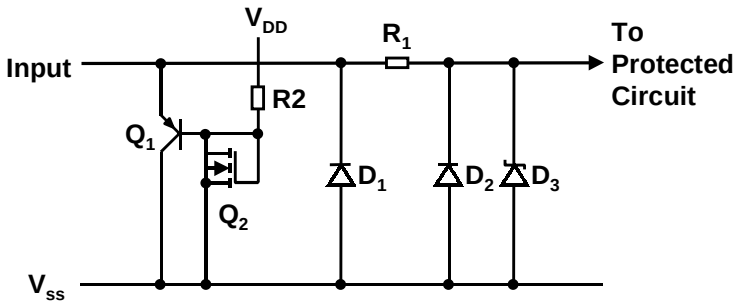
Absolute Maximum Ratings (TLC227x)

The absolute maximum ratings are the limit values for a specific device; if these are exceeded, permanent damage to the device may be caused. The picture above shows the Absolute Maximum Ratings as an example for the Advanced LinCMOS™ operational amplifier TLC2272.

CMOS devices are limited in their supply voltage and will not operate with supply voltages greater than 16 V. This can be seen in the example with the TLC2272 which has a maximum supply voltage V_{DD+} of 8 V and V_{DD-} of -8 V with respect to the midpoint between V_{DD+} and V_{DD-}.

An important value which often causes problems, is the input voltage of an op amp. For most of the devices, the input voltage shall not exceed the supply voltages. With the TLC2272 the input voltage must not be more than 0.3V more negative than V_{DD-} and not higher than V_{DD+}. This has to be considered especially when the supply voltage of the op amp is turned off and an input voltage is still applied. If this hasn‘t been taken into account, an excessive current will flow! Such excessive current can be avoided if the input current is limited by using an external current limiting resistor.

LinCMOS™ ESD Protection Schematic



All input and output pins on LinCMOS™ and Advance LinCMOS™ have an ESD protection to withstand:

- 2000 V discharged from a 100 pF capacitor through a 1500 Ω resistor **(Human Body Model)**
- 200 V discharged from a 100 pF capacitor with no current limiting resistor **(Charged Device Model)**

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Input Protection Circuit Operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterised by extremely fast rise times and usually low energies, and can occur both if the device has all pins open and if it is installed in a circuit.

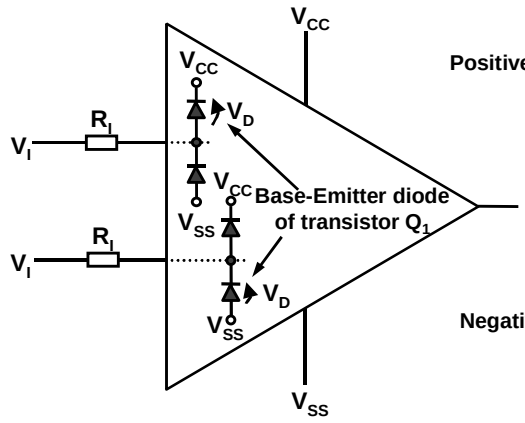
Positive ESD transients

Initial positively charged energy is shunted through Q_1 to V_{SS}. Q_1 will turn on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q_1. Additional energy is dissipated in R_2 when Q_1 h_{FE} limits and saturates. The base current now increases with input current. This current through R_2 will force the voltage at the gate of Q_2, which is a n-channel enhancement MOS transistor, to exceed its threshold voltage (V_T ~ 22 to 26 V) and turn on. The input current through Q_1 is now shunted through Q_2 to V_{SS}. If the voltage on the input pin continues to rise, the breakdown voltage of the Zener diode D_3 is exceeded and all remaining energy is dissipated in R_1 and D_3. The breakdown voltage of D_3 is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

Negative ESD transients

The negatively charged ESD transients will be shunted directly through D_1. Additional energy will be dissipated in R_1 and D_2 as D_2 becomes forward biased. The voltage seen by the protected circuit is -0.3 V to -1.0 V (the forward voltage of D_1 and D_2).

Input Current Limiting Configuration



Positive Voltage Input Current Limit:

$$R_I = \frac{+V_I - V_{DD} - V_D}{5\ mA}$$

Negative Voltage Input Current Limit:

$$R_I = \frac{-V_I - V_{SS} - (V_D)}{5\ mA}$$

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Input Current Limiting Configuration

LinCMOS™ operational amplifiers are being used in circuit environments that have input voltages which may exceed the recommended common-mode input voltage range. This, as an example, may be caused by using Rail-to-Rail operational amplifiers where output swing reaches the positive or negative supply voltage. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The picture above shows the equivalent protection by using a clamping diode to V_{CC} and to V_{SS}. The clamping diode in this case to V_{CC} is provided by the base-emitter-diode of transistor Q1 of the protection circuit as discussed before. The recommended current limit shown on most product data sheets is $\pm$ 5 mA.