Data Converters

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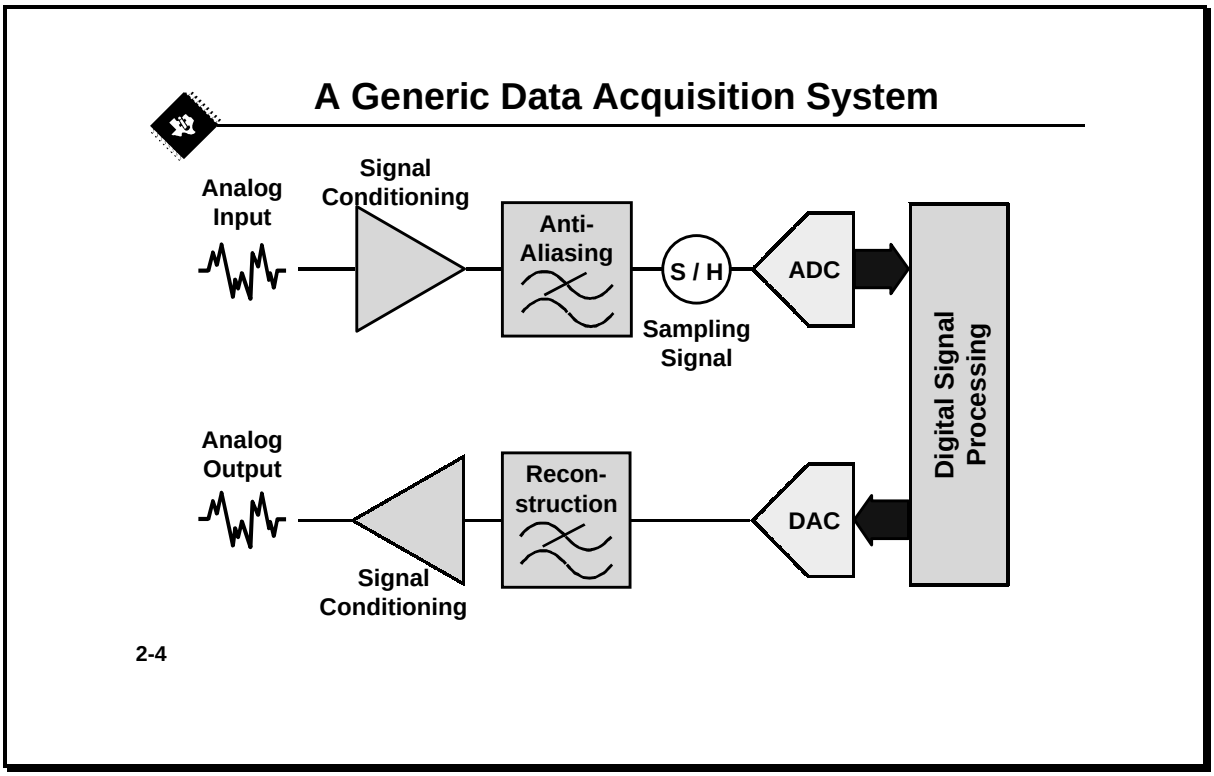
Data Converter Overview



What Is A Data Acquisition System?

For a computer or other digital equipment to process analog signals, these signals must first be converted from the analog domain to the digital domain. This process is called quantization. Quantization may be defined as the conversion of an input function, which may have values in a continuous range to an output that has only discrete values.

Data conversion uses the quantization process for transforming analog electrical signals into digital information for storage, display, processing, data transmission, or control. A data conversion system performs this task and comprises sensors, transducers, signal conditioning, anti-aliasing filters, sample-and-hold circuits, analog multiplexers and analog-to-digital converters (ADCs). Recovery of a digital signal into analog form is sometimes required. Digital-to-analog converters (DACs) and filters perform this function. The output amplifier provides the necessary drive the application requires.

How do you Choose a Data Converter?

Use the same converter you used last time.

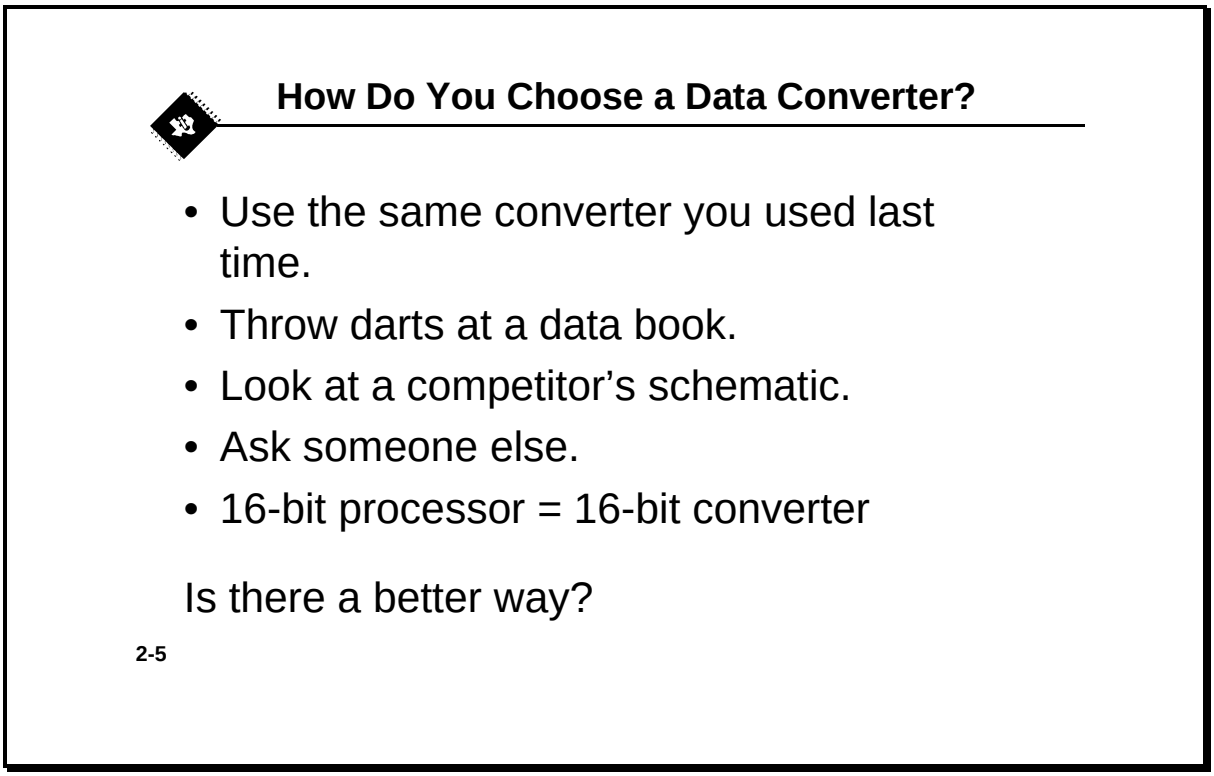
Throw darts at a data book.

Look at a competitor's schematic.

Ask someone else.

16-bit processor = 16-bit converter.

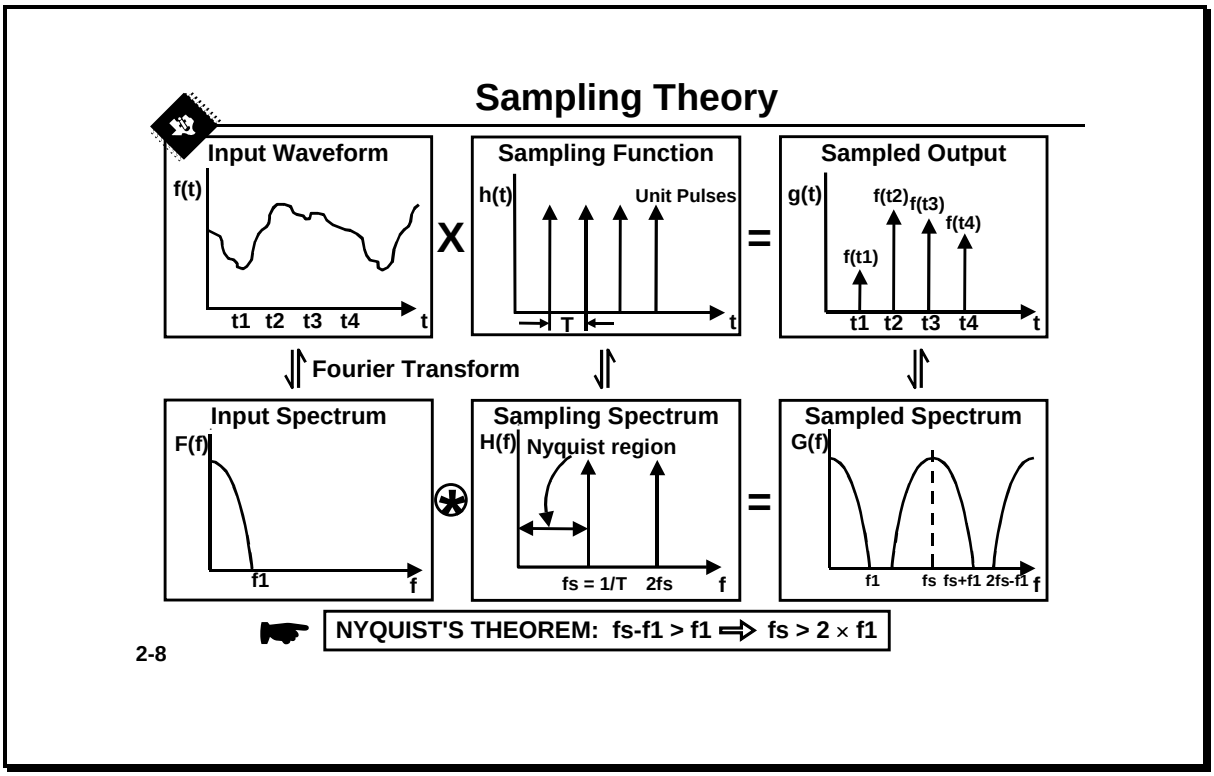
Is there a better way?



Many methods seem to be used in selecting data converters. Some of the methods described above would seem less than optimum. The objective should be to select the right converter for the application. Selecting the right converter be cost effective and provide the performance needed to implement the system solution.

Selecting the right converter begins with the system definition. A description overall system performance and a description of the signal to be converted are the first steps. The signal bandwidth will determine the converter speed. Signal information content will help to determine converter resolution. The system processor interface will determine the converter data interface. This results in an initial specification for a data converter. The converter requirements can be further defined by a more detailed evaluation of system requirements.

The next part of this section describes the basics of sampling theory and sources of error. The next parts describe DC and AC performance of converters. An understanding of the sources of error, AC and DC performance are necessary in order to refine the initial data converter requirements of speed and resolution. Often converters are selected on speed and resolution alone, however without an understanding of the other parameters it is difficult to achieve optimum system performance.



Sampling Theory Overview

In order to produce a discrete digital representation of a continuously varying analog signal, it is necessary to take samples of the signal at regular intervals and convert them from analog into digital form. In an ideal situation the sampling function is a train of impulses, each of which is infinitesimally narrow and has unit area. The frequency of these pulses is the sampling rate (fs). The input signal can also be idealized by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

The ideal sampling condition, represented in both the frequency and time domains, is shown in the figure above. The effect of sampling in the time domain is to produce amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown, with sidebands around each discrete frequency produced by the amplitude modulation. In effect some of the higher frequencies are “folded back” so that they produce interference at lower ones. This interference causes distortion, which is called aliasing. Aliases cannot be removed by subsequent processing.

If we assume that the input signal is band limited to a frequency f_1 and is sampled at frequency f_s it is clear from the figure that the overlap (and hence aliasing) will not occur if

$$f_1 < f_s - f_1$$

This could also be expressed by: $2f_1 < f_s$

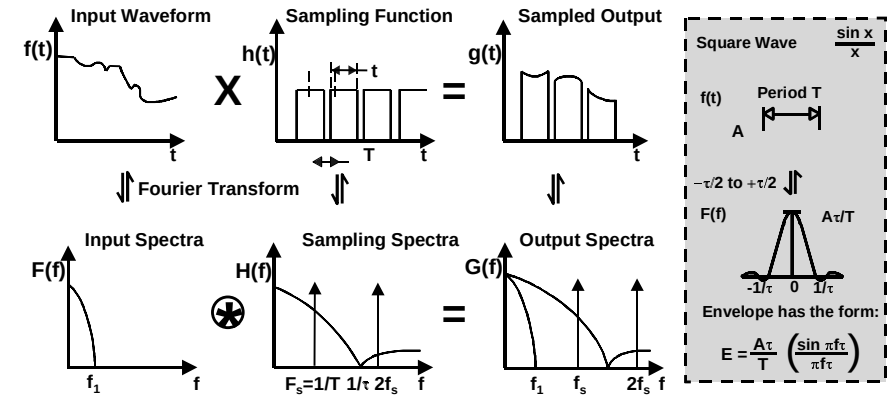
Therefore, if sampling is done at a frequency at least twice as great as the maximum frequency of the input signal, no aliasing will occur and all the signal information can be extracted. This is Nyquist's Sampling Theorem, which provides a basic criterion for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

In real sampling, however, the width of each sample is finite and this gives rise to a modulation error of (sin x) / x. This is explained later.

Real world signals are generally not band limited. To avoid errors due to aliasing an anti-aliasing filter is normally used. This filter band limits the signal and minimizes any errors due to aliasing. Anti-aliasing filters can be either external or internal to the data converter.

When designing a system it is necessary to know the input signal characteristics in order to select a sampling rate and filters, if necessary, for minimum conversion errors.

Real Sampling - Analog to Digital Conversion



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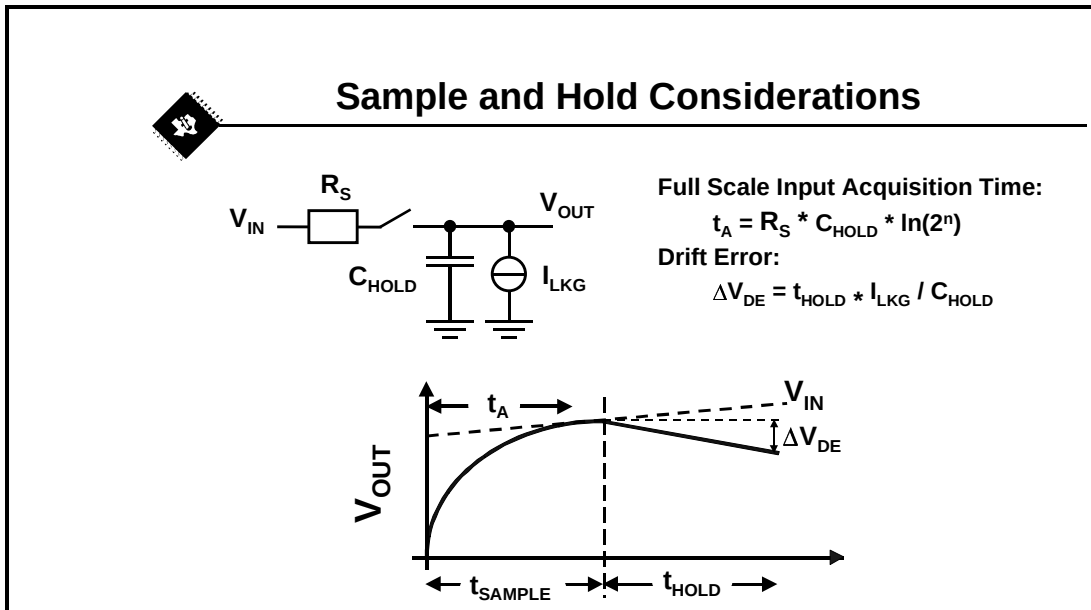
Real Sampling Analog to Digital Conversion

Sampling analog input signals with a unit impulse is an ideal case, which can only be approximated in practice. As shown in the above figure, a real sampling pulse will have a finite width τ, but this should still be much shorter than the sampling interval T. The effect of a sampling pulse τ of finite width is to multiply the input signal by a (sinx)/x function in the frequency domain, as shown above, and attenuate the higher frequencies. The narrower the sampling pulse τ the lower this attenuation will be.

For practical sample and hold (S/H) devices and analog to digital converters that contain an S/H function the aperture over which the incoming signal is sampled gives the effective sampling pulse width. This aperture is the transition time from sample to hold and the value held is the average input over this transition. In this situation the sampling pulse width is the uncertainty or jitter in the sampling instant caused by noise on the digital hold signal within the device. For analog to digital converters, usually of older design, that does not include a S/H function the aperture or sampling pulse width is equal to the conversion time.



Sample and Hold Considerations

Acquisition Time

During the sampling phase, period t_{SAMPLE}, of a sample and hold circuit's operation it acquires and tracks the input signal to within a specified error band.

The Acquisition time, t_A, required depends on the impedance driving the sample and hold and the capacitor value within the sample and hold. The worst case value for the acquisition time when the input voltage goes from a minimum input to a maximum input, that is the input range of the ADC that the sample and hold is driving.

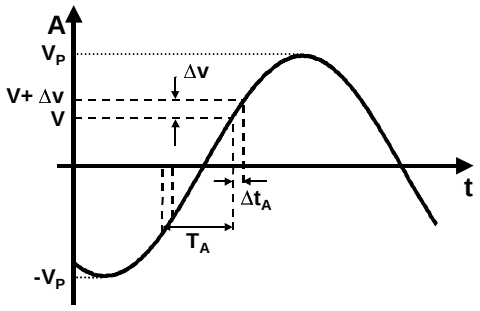
Voltage Drift

Once the signal has been held, its output will start to droop due to the leakage of the capacitor, open circuit leakage of the analogue switch and impedance of the following stage.

Assuming a constant leakage current of I_{LKG} over the hold period the held signal will have dropped by:

$$V_{Droop} = t_{HOLD} * I_{LKG} / C_{HOLD}$$

Aperture-Jitter (Sampling Uncertainty)



The Aperture Error is less than 1 LSB, if:

$$\Delta t_A < \frac{1}{2^n \times \pi \times f_{max}}$$

In a 12-bit system with a maximum signal frequency of 20 MHz, the Aperture-Jitter has to be less than 3.8 ps !

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Aperture Jitter (Sampling Uncertainty)

A parameter, which may decrease the SNR of the system, is caused by the sampling uncertainty, or the Aperture-Jitter. If the aperture time varies by the time Δt_A, an error is caused which is equal to the change Δv in the voltage. This results into a degradation of the SNR of an ADC. To calculate the maximum time Δt_A which results into an error less than 1 LSB, a sine wave with the maximum frequency f_{max} as an input signal is considered. This can be expressed as:

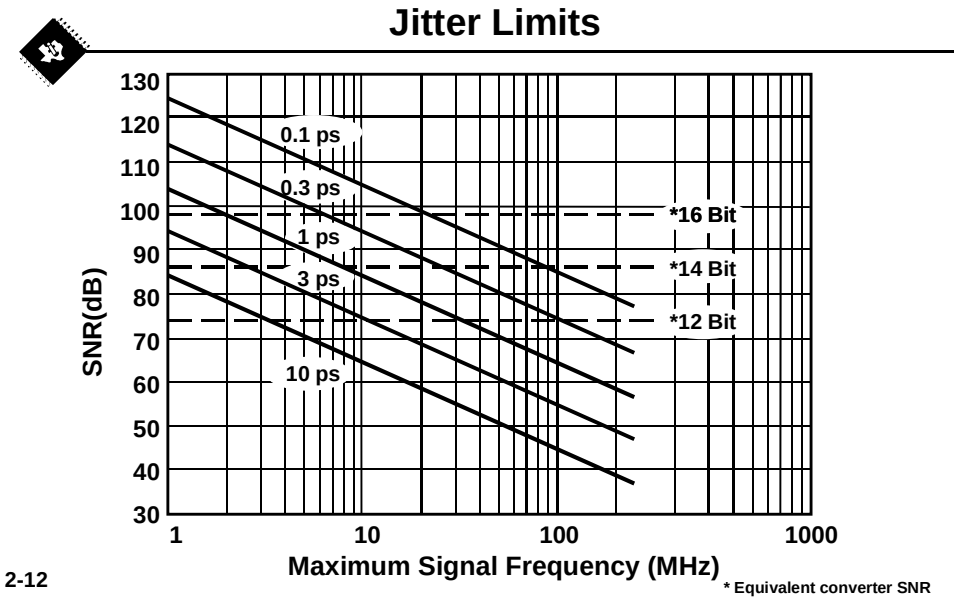
$$v(t) = V_P \times \sin \omega t .$$

The slope of the sine signal is:

$$\frac{dv}{dt} = V_P \times \varpi \times \cos \varpi t .$$

The maximum slope occurs when $\cos \varpi t = 1$, or at the zero-crossing point. This results in: $\Delta t_A = \frac{\Delta v}{V_P \times \varpi}$. In order to limit the error in the change of the voltage to less than 1 LSB (1 LSB can be expressed as $\frac{2V_P}{2^n}$), Δt_A results in:

$$\Delta t_A < \frac{1}{(2^n) \times \pi \times f_{max}} .$$



Jitter Limits

The degradation of the SNR, caused by the phase jitter, is a function of the frequency and the maximum phase jitter t_j. As described before, the slew rate of a sine wave can be expressed by:

$$\frac{dv}{dt} = V_P \times \omega \times \cos \omega t ,$$

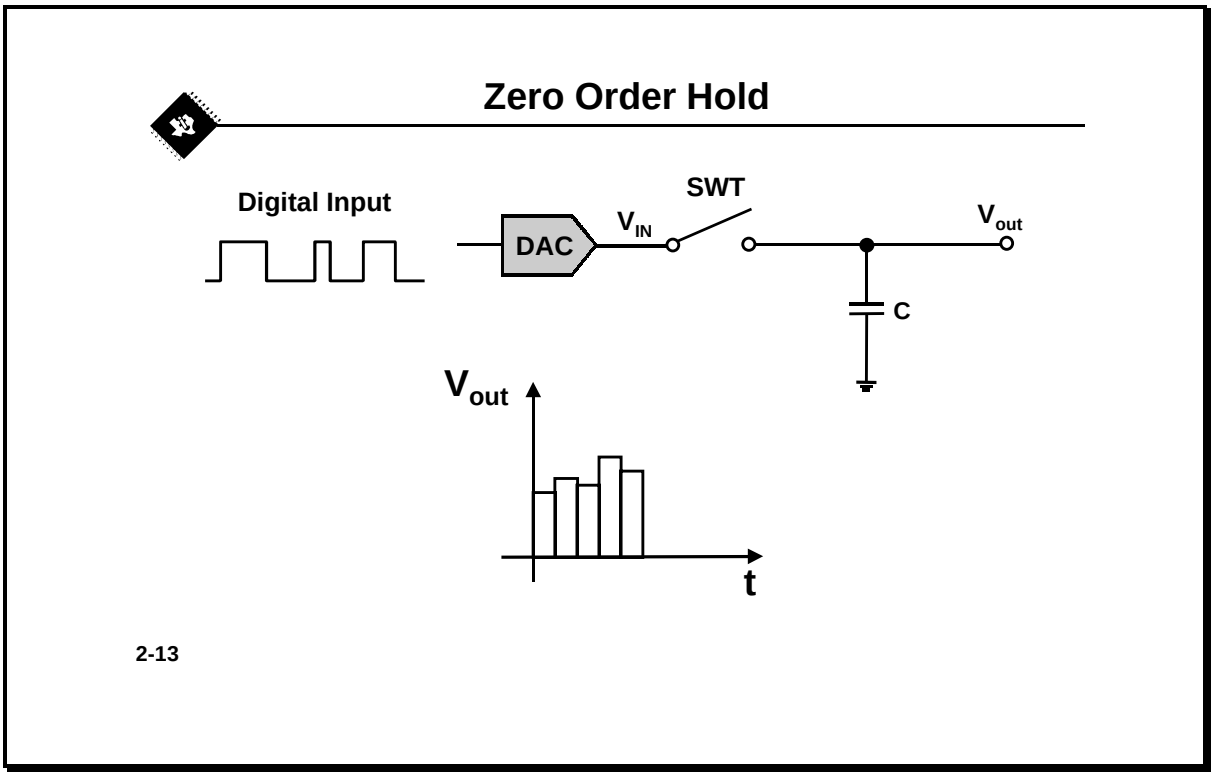
and the maximum slew rate of a sine wave is at the zero-crossing point.

$$\frac{dv}{dt}\Big|_{max} = V_P \times \omega .$$

The rms value is then $\frac{dv}{dt}RMS = \frac{V_P \times \omega}{\sqrt{2}}$, therefore $\Delta Vrms = dvrms \times dt$ (with $dt = t_j$). The SNR is given by: $SNR = \frac{V_P}{\sqrt{2}\Delta Vrms}$, expressed in dB:

$$\boxed{SNR_{(dB)} = 20 \times \log \frac{1}{2 \times \pi \times f \times t_j}}$$

For instance, with a jitter of 3 ps and with a maximum signal frequency of 10 MHz, the SNR is about 74 dB.

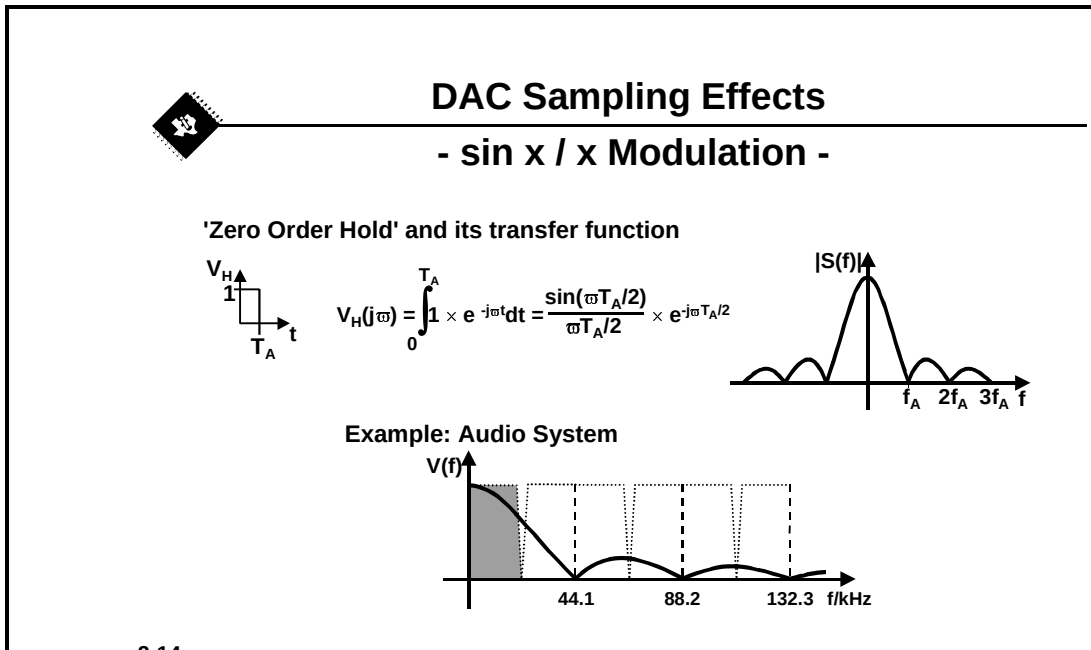


Zero Order Hold

A switch and a capacitor can represent the simplest form of a zero order hold. The switch is closed for a short time and places a coded voltage on the hold capacitor and repeats the process for every switch closure.

The sample and hold function produces the output voltage envelope shown in the insert as more samples are taken.

Most DAC architectures replicate this sample and hold function to produce the envelope waveform and reduce transients associated with code changes (glitches). The output voltage of the DAC is sin x/x weighted, which is shown on the next page.



DAC Sampling Effects - sinx/x Modulation

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical idea, which can be approached but never fully reached in practice. Instead of the ideal very short output pulse, the sample and hold stage produces at the output a pulse with a length which in some cases is up to about the sampling frequency. D/A converters are a good example for this, where the analog output is maintained over the period where the next analog voltage is reproduced. The result of sampling with a finite pulse shows that the original signal is weighted with a (sin(x))/x function, where x in this case is $\pi f/f_S$.

$$x = \omega \times \frac{T_A}{2} = 2 \times \pi \times f \times \frac{T_A}{2} = \pi \times f \times \frac{1}{f_s} = \pi \times \frac{f}{f_s}$$

This effect is also known as (sin(x))/x distortion. The error resulting from this can be controlled with a filter which compensates for the (sin(x))/x distortion. This can be implemented as a digital filter, in a DSP, or using conventional analog techniques. The (sin(x)/x) is much worse on DACs than on ADCs. Therefore, a correction is performed many times in D/A converters.

DC Specifications

How Large is an LSB ?

$$1\ LSB = \frac{V_{FULLSCALE(nom.)}}{2^N} \qquad N = \text{Resolution of ADC}$$

N =	8	10	12	14	16	20
1 LSB ± 5 V input range	39.06 mV	9.77 mV	2.44 mV	610 µV	153 µV	9.53 µV
1 LSB + 5 V input range	19.53 mV	4.88 mV	1.22 mV	305 µV	76.3 µV	4.77 µV
1 LSB + 3 V input range	11.72 mV	2.93 mV	732 µV	183 µV	45.8 µV	2.86 µV

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How Large is a LSB ?

A code of an ADC represents a specific voltage magnitude, which is given by:

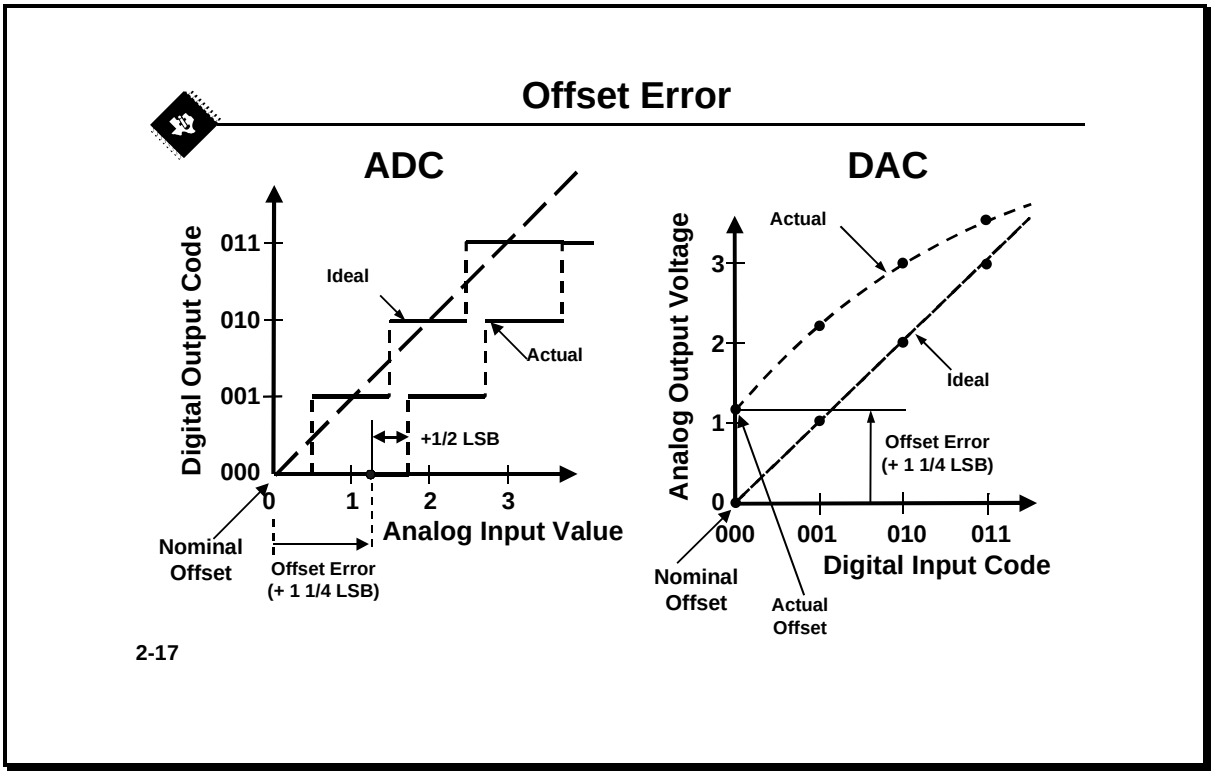
$$1LSB = \frac{V_{FS(nom.)}}{2^N},$$

Where N is the resolution of the ADC. The figure shows the magnitude of a LSB for different resolutions and different analog input voltage ranges. It‘s obvious that the LSB is getting very small if the ADC provides a high resolution or the analog input voltage range is small. The figure shows LSB values smaller than 1 mV. Therefore, it is a challenge to keep the error (offset, drift, noise), which is caused by the signal conditioning stage below an LSB of the ADC.

Practical Full-Scale Range (VFS) is the total range of analog values that correspond to the ideal transfer line.

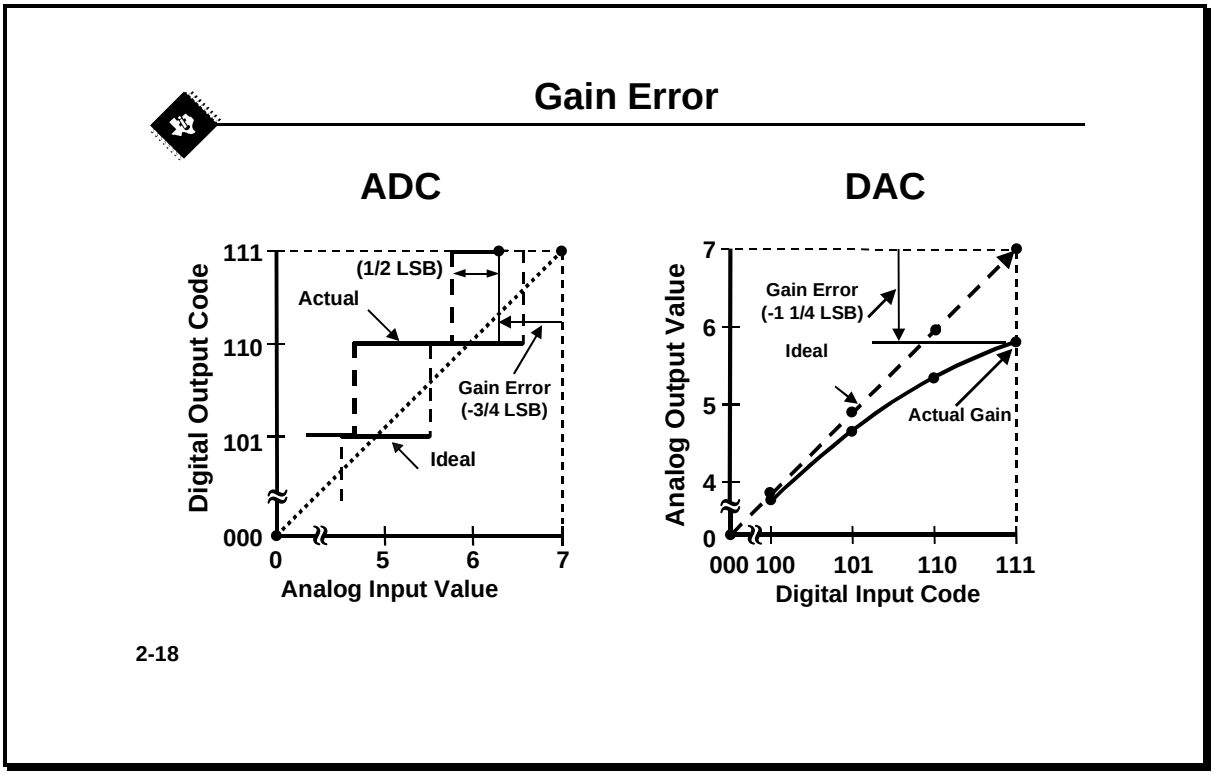
$$1LSB = \frac{V_{FS}}{2^N - 1},$$

Nominal Full-Scale Range (VFS(nom)) is the total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.



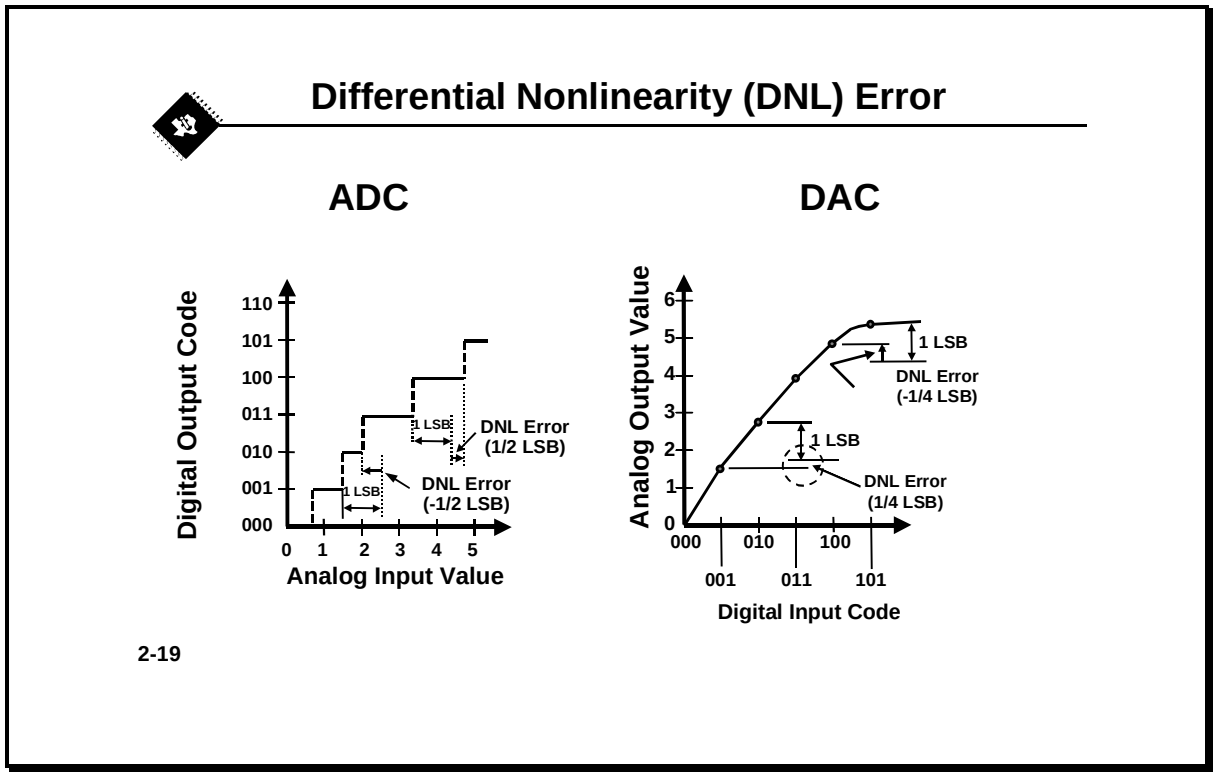
Offset Error

The offset error is defined as the difference between the nominal and actual offset points. For an A/D converter, the offset point is the mid step value when the digital output is zero and for a DAC it is the output value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error.



Gain Error

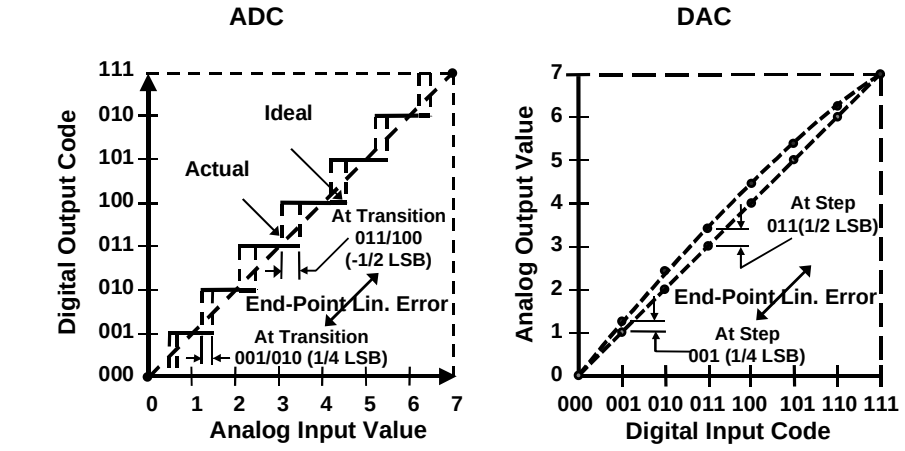
The gain error as shown in the picture is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.



Differential Nonlinearity (DNL) Error

The differential nonlinearity error shown in the figure above (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become nonmonotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible 2^n binary codes are never output.

Integral Nonlinearity (INL) Error



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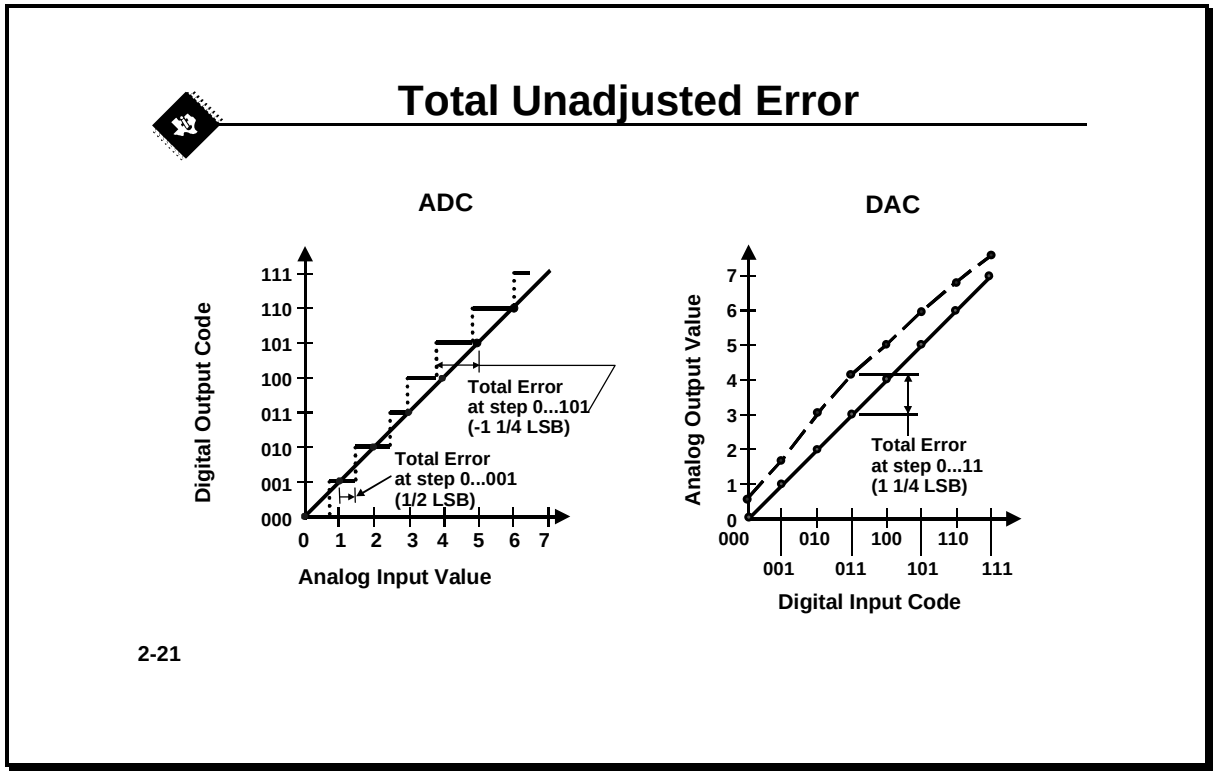
Integral Nonlinearity (INL) Error

The integral nonlinearity error is shown in the figure above. It is sometimes seen as simply deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

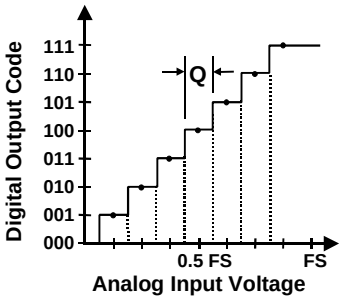


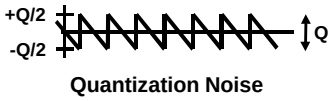
Absolute Accuracy (Total) Error

The absolute accuracy or total error of an ADC as shown in the picture is the maximum value of the difference between analog value and the ideal midstep value. It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC.

Dynamic (AC) Specifications

Signal to Noise Ratio of Data Converter





$$SNR = \frac{V_{SIN}}{V_N}$$

$$SNR(dB) = 6.02 \times N + 1.76$$

N is number of bits of resolution

Each extra bit provides approximately 6 dB improvement in the SNR !

Effective Number Of Bits (ENOB):

$$ENOB = \frac{(SNR + D)(dB) - 1.76}{6.02}$$

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Signal to Noise Ratio of Data Converter

The Signal to Noise Ratio (SNR also often referred to as S/R) is a very important parameter for an A/D converter. The SNR is the ratio of the rms (root mean square) value of the input signal to the rms value of the quantization noise. The input signal is typically a sine wave with a maximum amplitude V_{peak}. The rms value can be calculated as follows:

$$V_{SIN(RMS)} = \frac{V_{PEAK}}{\sqrt{2}} = \frac{V_{FSR}}{2 \times \sqrt{2}}$$

The quantization noise voltage, which is also shown in the picture, is similar to a sawtooth voltage waveform. The rms value of a sawtooth waveform is: $V_N = \frac{V_P}{\sqrt{3}}$, where V_P is Q/2. This results into $V_N = \frac{Q}{2 \times \sqrt{3}} = \frac{Q}{\sqrt{12}} = \frac{V_{FSR}}{2^n \sqrt{12}}$. Therefore, the SNR can be derived.

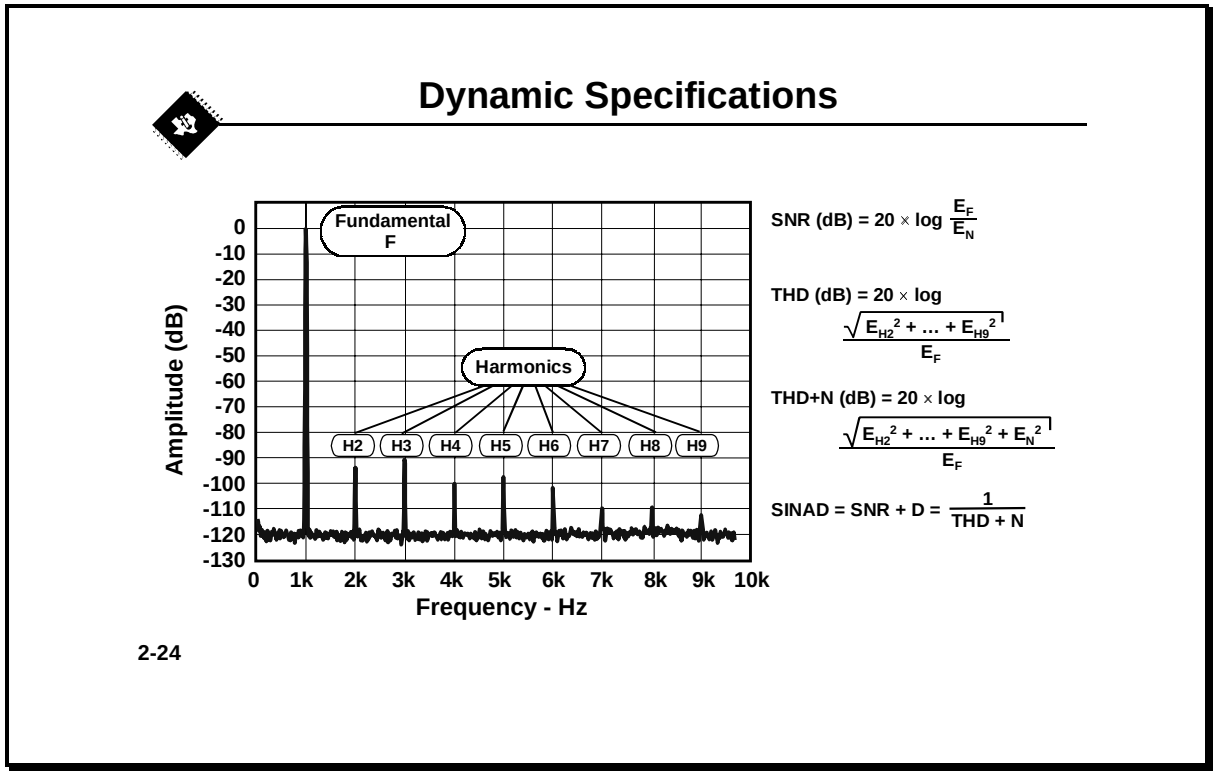
$$SNR = \frac{V_{FSR}}{2\sqrt{2}} \times \frac{2^n \sqrt{12}}{V_{FSR}} = 2^n \sqrt{1.5}$$

$$SNR(dB) = 20 \times \log 2^n + 20 \times \log \sqrt{1.5} = n \times 20 \times \log 2 + 20 \times \log \sqrt{1.5}$$

This can be written as:

$$\boxed{SNR(dB) = 6.02 \times n + 1.76} \quad (1)$$

The theoretical SNR of a 12-Bit ADC is approximately 74 dB.



Dynamic Specifications

SNR

For a full-scale sinewave input, the theoretical SNR for an N bit converter is given by: SNR = 6.02N + 1.76 dB as already derived before. The normal way of measuring the SNR for a converter is to digitize a full-scale sinewave and then perform an FFT on the output. The rms power of the fundamental is then compared to the noise floor by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of noise. The ratio of the two is taken to give a direct measurement of the SNR.

THD

As in SNR testing, the normal way of measuring the distortion for a converter is to digitize a full-scale sinewave input and then perform an FFT on the output. The rms power of the fundamental is then compared to the sum of the harmonics by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of harmonics. The ratio of the sum of the harmonic amplitudes to the fundamental gives a direct measurement of distortion. The number of harmonics, which are used for the THD calculation, may vary depending on the particular application.

THD + N

The distortion plus noise (THD + N) is the ratio of the sum of the harmonic distortion and noise to the rms power of the input signal. The distortion and noise

are measured separately and than added together to form the ratio. The noise voltage relates to the measured bandwidth.

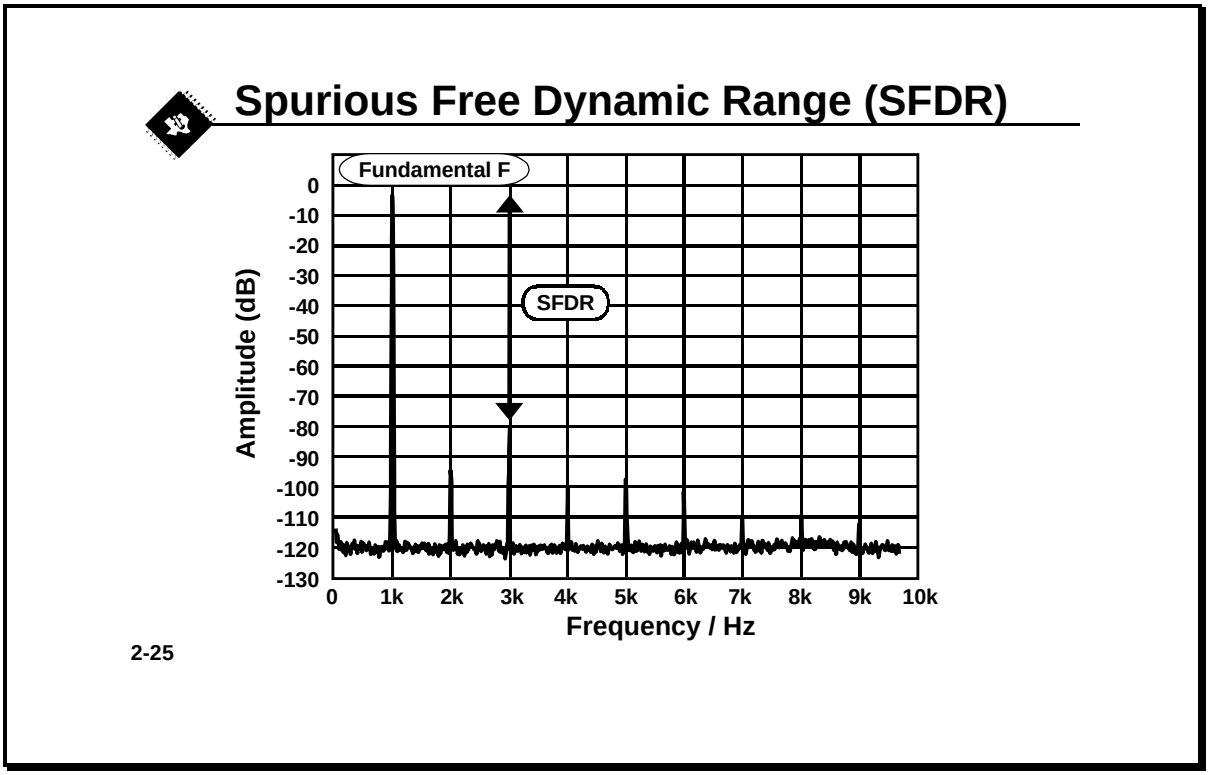
SINAD

The signal to distortion plus noise (SINAD) is the ratio of the input signal to the sum of the harmonic distortion and noise. The distortion and noise are measured separately and than added together to form the ratio. The SINAD is the reciprocal to the THD + N. The SINAD and THD+N are a good indication of the overall dynamic performance of the ADC, because all components of noise and distortion are included.

This measurement is used to determine the **E**ffective **N**umber **of B**its (ENOB) of accuracy the converter displays at that frequency. For example, a nominal 8 bit resolution ADC may be specified as having 45dB SNR at a particular input frequency. The number of effective bits is defined as

$$ENOB = \frac{SNR_{REAL} - 1.76}{6.02} = 7.2\ bits$$

The actual performance of the device is therefore less than its nominal resolution at this frequency.

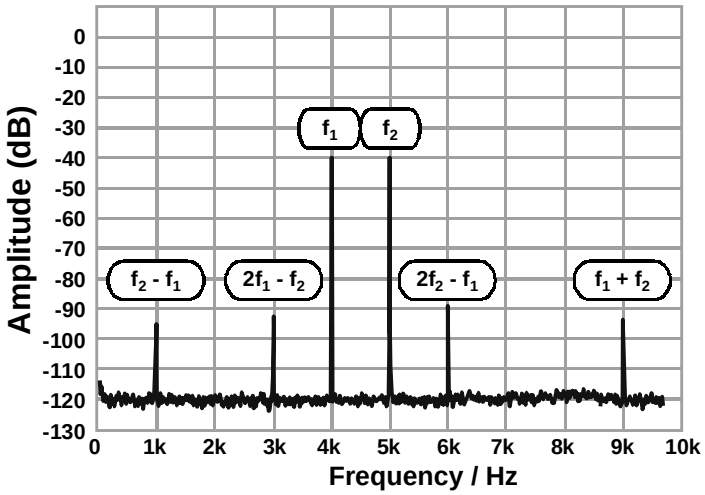


Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is also a very important dynamic specification for wide dynamic range and high frequency applications. The SFDR is the difference in dB between the maximum signal component and the largest distortion component as shown in the picture. The SFDR becomes an issue when the spectral purity of a converter is important. This is the case for A/D converters in noisy receiver environments where the converter must digitize a small-amplitude signal.

The SFDR of the 10-bit 20 Msps A/D converter TLC876 is typically 64 dB at 20 Msps with a 3.58 MHz input signal. The SFDR of the 8-bit 40 Msps A/D converter TLC5540 is typically 46 dB at 40 Msps with a 3 MHz input signal.

Intermodulation Distortion, IMD



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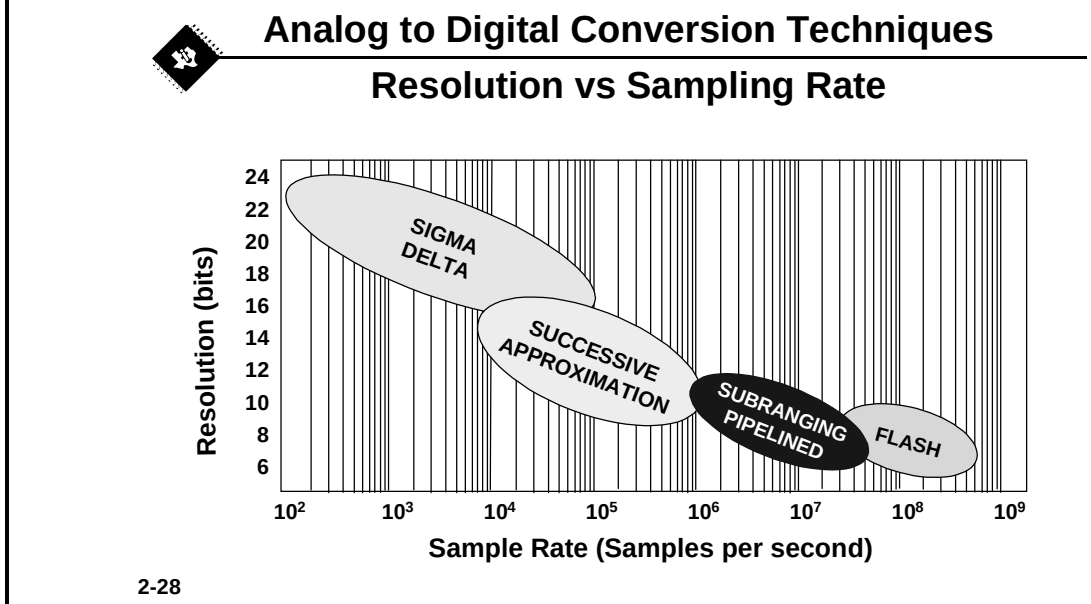
Intermodulation Distortion IMD

Intermodulation distortion is a measurement of how much one frequency modulates another frequency within a system. Two frequencies are added together and applied to the system. The output harmonic products are measured and the value is also a measure of linearity. The more linear the system is, the lower the intermodulation products become. The second order terms are: $f_1 + f_2$ and $f_2 - f_1$. Third order terms are: $2f_1 + f_2$, $2f_1 - f_2$, $f_1 + 2f_2$ and $f_1 - 2f_2$. Especially when the distortion frequencies are close to the original frequencies, it will be very difficult to filter these out. Also in RF applications, the IMD products can mask out the information of very small-amplitude signals.

A/D Converter Architectures



Analog to Digital Conversion Techniques

The analog to digital converter (ADC) is a vital component in many of today's digital signal processing systems. The architecture used to implement the ADC is determined by the combination of sample rate and resolution for which the converter is specified. The picture shows four of the most popular conversion methods.

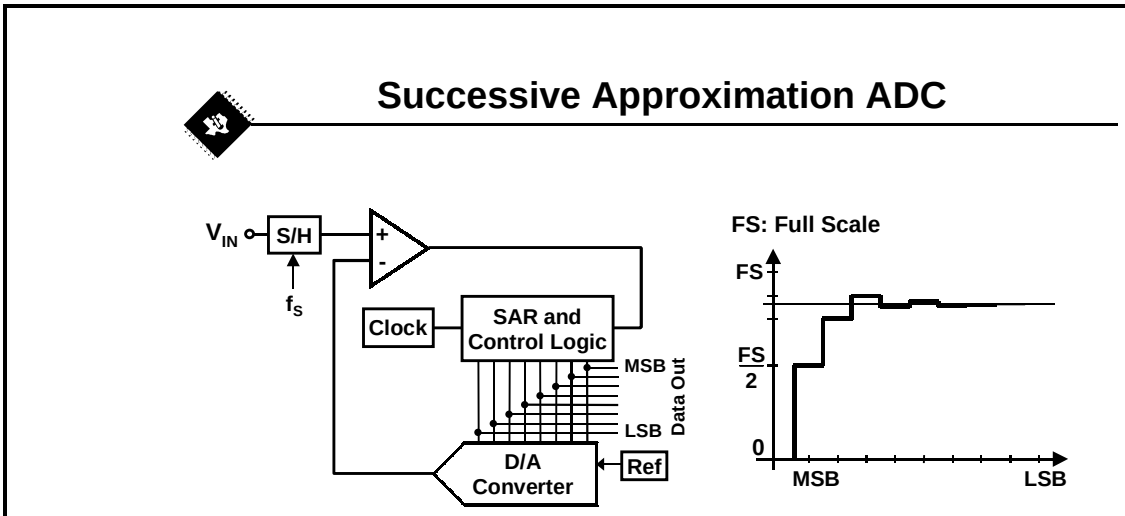
The successive approximation register (SAR) method has been used extensively throughout the last two decades to produce a wide range of ADCs with individual resolutions ranging from 8 to 16 bits. For a particular IC process, sample rates of these converters are inversely proportional to the resolution. This is because the conversion method requires one clock cycle to produce each bit of the output result. This limits the maximum practical sample rate which SAR type ADCs can achieve. However, successive approximation architectures do offer parallel data output.

The sigma delta method has grown in popularity in recent years, particularly for sample rates below 100 ksps. They are used extensively for the conversion of audio signals. This technique lends itself well to oversampling followed by decimation and digital low pass filtering. It also produces the highest resolution ADC's currently available.

The flash conversion method has previously been favored for achieving sample rates in excess of 15 MSPS. However, the flash method requires 2^n-1 comparators to implement an n-bit converter. This means that 255 comparators

are needed for an 8-bit ADC. Flash converters therefore occupy a relatively large area of silicon, require a lot of power, have a high input capacitance and are expensive.

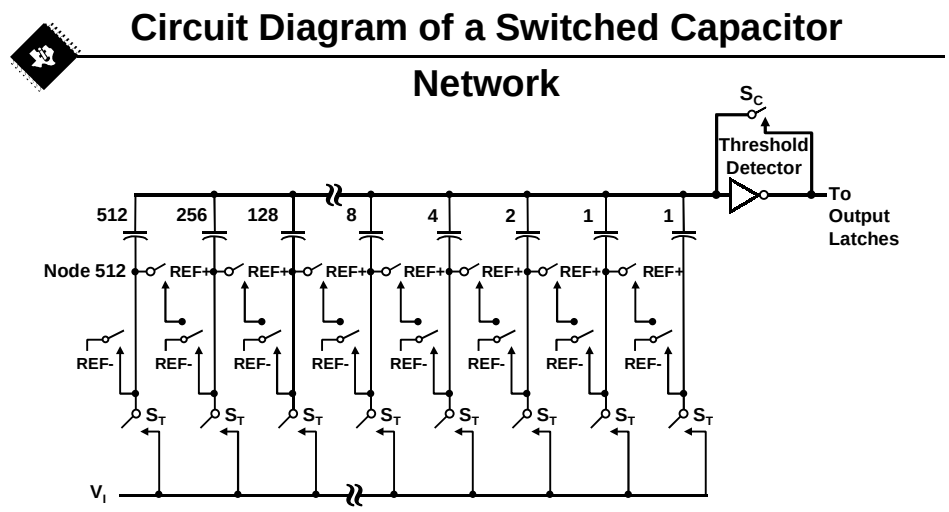
Semi-flash and, more generally, subranging architectures offer a good compromise between lower power/cost and the high speed of the flash approach. Recently pipelined architectures have been gaining in popularity because they offer an excellent combination of high sample rates, relatively small IC area and moderate cost. They are particularly suitable for continuous sampling applications where their inherent pipeline delay will not affect system performance.



Successive Approximation ADC

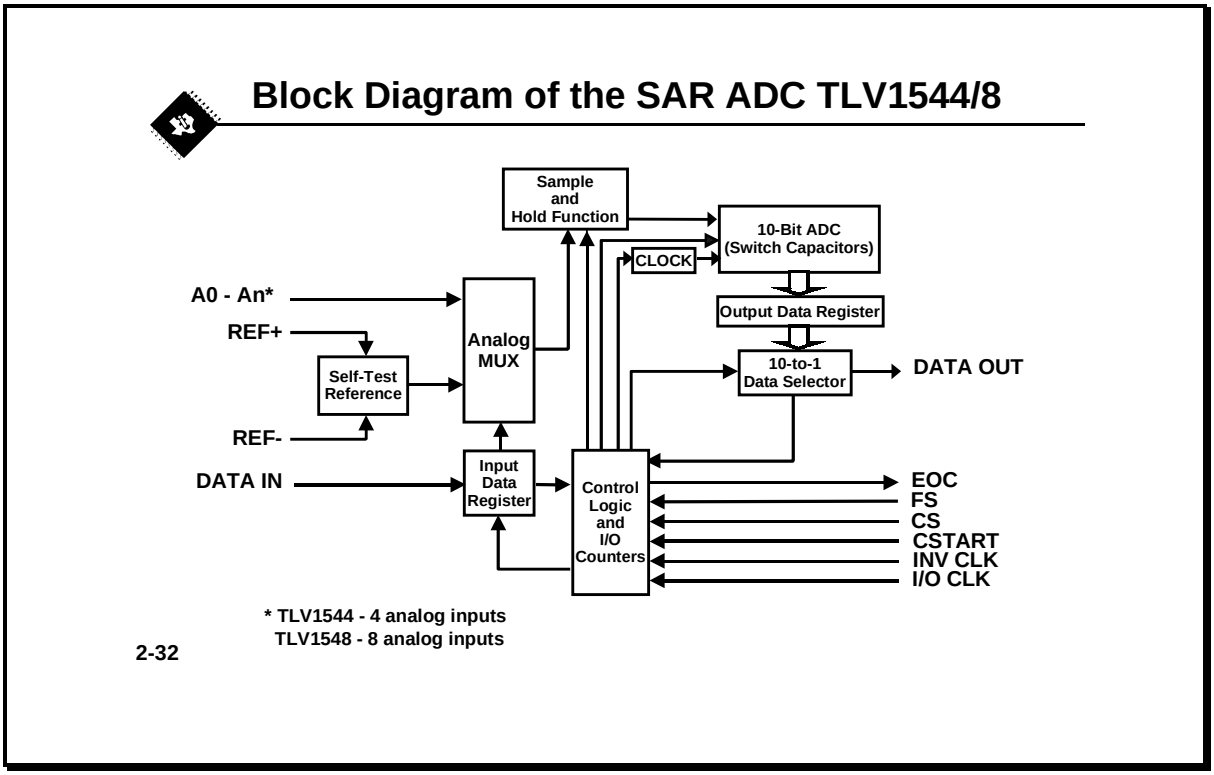
Successive approximation is a common technology for A/D converters. A conversion time from 100 μs to below 1 μs and a resolution up to around 16 bits is possible and make this type of ADC still the most popular type of converter.

Successive comparison of an unknown analog input voltage with binary weighted values of a reference give this method its name of “successive approximation”. A converter of N-bit resolution takes “N” steps to achieve a digital output. The conversion technique is the following. One input of the comparator, shown in the block diagram, is driven by an unknown input signal, V_{IN}, while the output of the DAC drives the other. The successive-approximation register (SAR) provides the input to the DAC When the DAC has its MSB set to logic level 1 (with all other bits zero) by the successive-approximation register (SAR), it will produce a voltage output of 1/2 the reference (analog input full-scale range). The comparator then determines if the DAC output is above or below the unknown input signal. If, as shown, the input signal V_{IN} is above the DAC output value, the MSB is retained in the successive-approximation register while the next weight of 1/4 the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register. While the successive-approximation converter process continues, the input signal must be held constant using a sample-and-hold circuit in front of the comparator. Alternatively, the signal should, as a rule of thumb, vary a maximum of 1/2 LSB during conversion. This puts a slew-rate or full-scale frequency limitation on the signals the converter can handle.



Circuit Diagram of a Switched Capacitor Network

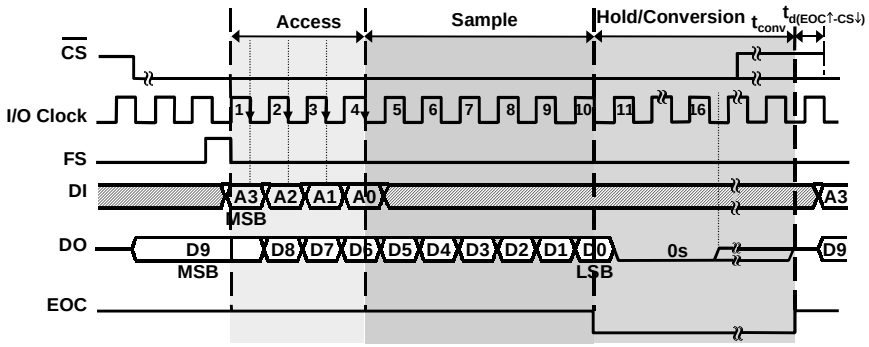
The CMOS threshold detector in the successive-approximation conversion system determines the value of each bit by examining the charge on a series of binary-weighted capacitors (see picture). In the first phase of the conversion process, the analog input is sampled by closing the S_C switch and all S_T switches simultaneously. This action charges all of the capacitors to the input voltage. In the next phase of the conversion process, all S_T and S_C switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half V_{CC}), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.



Block Diagram of the SAR ADC TLV1544/8

The picture shows the block diagram of the TLV1544/8 which is typical for a successive approximation ADC (SAR ADC). The ADC has an analog multiplexer on chip, where the analog input channel is selected. Further programmable features like self-test reference, programmable conversion rate, power-down state and the conversion speed can be chosen. These different choices have to be written into the Input Data Register. The analog input signal is sampled and held, and the converted signal is written into the Output Data Register where it can be read out via the 10-to-1 Data Selector and the Data Out pin of the device. The selection of the desired mode of the ADC needs specific timing, which is shown on the next page.

Maximum Sampling Rate of the TLV1544/8



t_{cycle} = 10 I/O Clk + t_{conv} + $t_{d(EOC↑ - CS↓)}$ = 11.35 µs

$f_{Smax} = \frac{1}{t_{cycle}} \approx$ 88 ksps

t_{conv} = 10 µs max

$t_{d(EOC↑ - CS↓)}$ = 100 ns min

f_{max} = 8 MHz

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Maximum Sampling Rate of the TLV1544/8

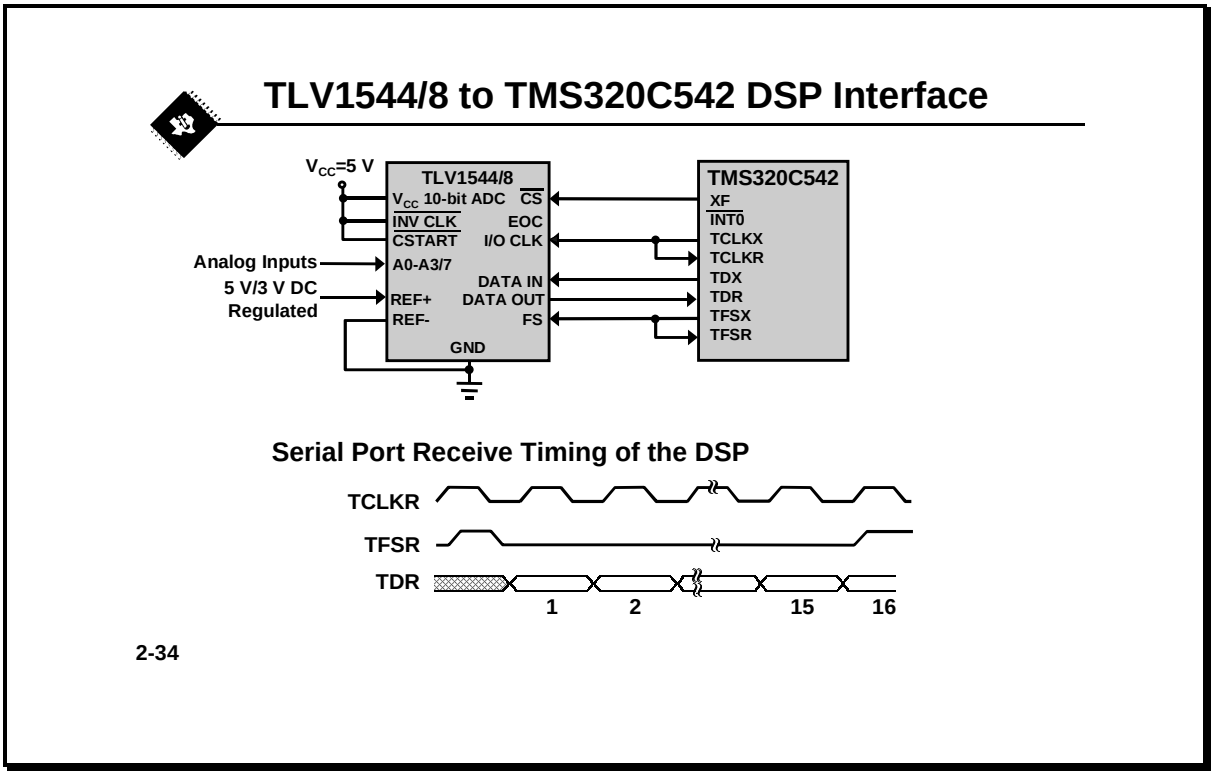
A frequently asked question is how to calculate the maximum sampling frequency of an A/D converter. The figure shows the timing diagram of the 10-bit serial A/D converter TLV1544/8. The first four I/O CLK cycles load the input data register with the 4-bit input data on DATA IN that selects the desired analog channel. The next six clock cycles provide the control timing for sampling the analog input. The sampled analog input is held after the first I/O CLK sequence of ten clocks. The tenth clock edge also takes EOC low and begins the conversion. The conversion time depends on the selected mode. If the fast conversion is selected, the maximum conversion time will be 10 µs (40 µs in the slow conversion mode). Therefore, the maximum sampling frequency can be calculated as follows:

$$f_s = \frac{1}{t_{cycle}}$$

The cycle time of a complete conversion is given by:

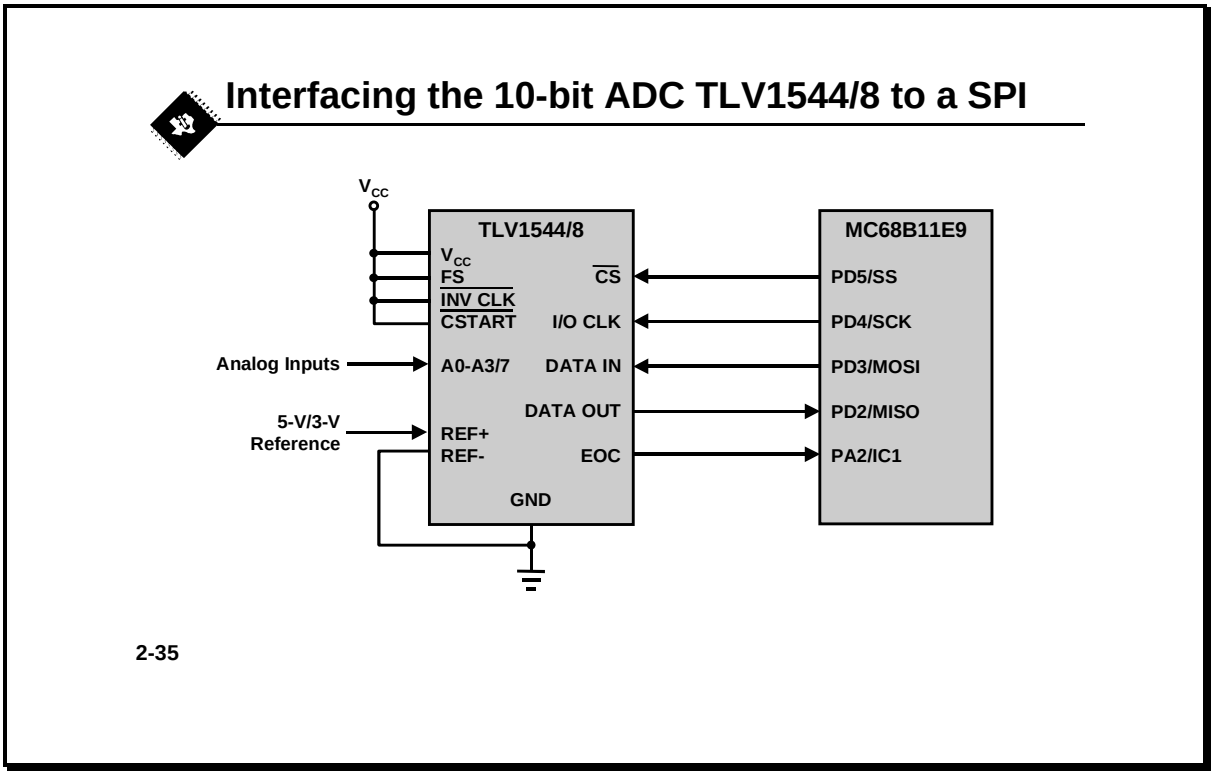
$$t_{cycle} = 10\, I/O\, Clk + t_{conv} + t_{d\,(EOC\uparrow - CS\downarrow)}$$

The minimum delay time, EOC ↑ to CS low is 100 ns. With a maximum I/O CLK frequency of 8 MHz, the maximum sampling frequency results in around 88 ksps. However, at this high sampling frequency the driving source resistance has to be taken into account.



Interfacing the TLV1544/8 to the TMS320C542 DSP

The circuit diagram shows the configuration that can be used to interface the A/D converter TLV1544/8 to the fixed point DSP TMS320C542.
The timing diagram of the TLV1544/8 was already shown before in combination with the maximum sampling rate of this converter. The I/O Clock signal is in this interface generated by the DSP and oscillates continuously. When CS is brought low by using the XF output of the DSP and a Frame Sync (FS) signal is received on the FS pin, the TLV1544/8 starts simultaneously to receive the next operation mode byte (DATA IN) and to send the last converted value (DATA OUT). Once the first four input bits have been received, any more data to the input is ignored.
Conversion complete is determined using a software routine and a DSP internal timer. This configuration is described in an application report. The EOC signal can be used with an inverter connected to an interrupt.



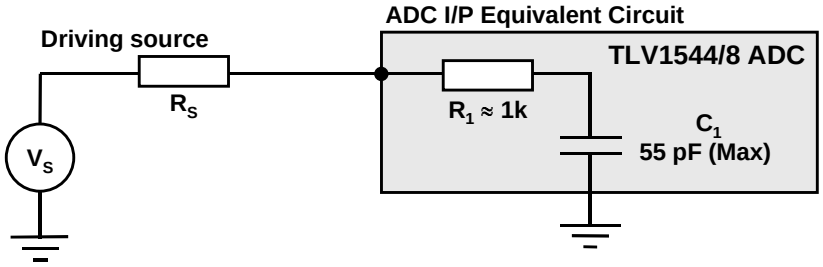
Interfacing the TLV1544/8 to a SPI

A very efficient way to interface an ADC to a Microcontroller is to use the SPI (Serial Peripheral Interface). Microcontrollers which include the SPI interface are for instance the TMS370C10 and the MC68HC11.

A SPI consists of an 8-bit serial shift register, which is initially loaded by software with the mode-control data to be sent to the ADC input. The SPI transfer is then initiated by software. This automatically starts the output of serial data from the MOSI (Master Out Slave In) pin of the microcontroller. At the same time data from the previous conversion result is received at the MISO (Master In Slave Out) pin of the microcontroller. This data is shifted into the other end of the serial shift register. On completion of an 8-bit SPI transfer the new content of the shift register is automatically loaded into a serial input buffer ready to be read by the next software instruction in the routine.

Driving the Input of a Switched Capacitor ADC

- Driving source needs to charge C1 to within 1/2 LSB during sampling time
- Time to charge to 1/2 LSB = TC × ln(2 × resolution)
- ≈ 7.6 × TC for a 10-bit converter, or 9 × TC for a 12-bit converter



Time constant (TC) = $(R_S + R_1) \times C_1$

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Driving the Input of a Switched Capacitor ADC

Switched capacitor ADCs offer an inherent sample-hold function at their input. This avoids the need to provide an external sample-hold but care should be taken to ensure that sufficient time is allowed during the sampling phase of the conversion process. For correct operation of the ADC, the capacitor must be charged to the required accuracy of ½ LSB or more during the sampling phase of the ADC. The voltage V_C on capacitor C_1 is given by:

$$V_C = V_S(1 - e^{-t/TC})$$

where TC is the time constant $C_1(R_S + R_1)$. Therefore, we get:

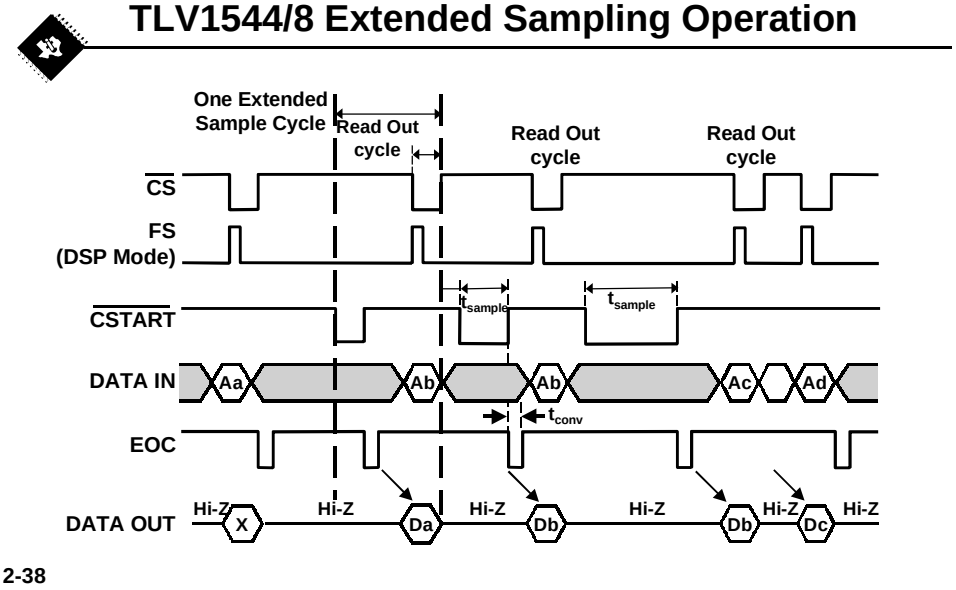
$$e^{-t/TC} = (1 - \frac{V_C}{V_S}), \text{ and } -t/TC = \ln(1 - \frac{V_C}{V_S})$$

Hence for a full-scale change in input voltage, the time to settle to ½ LSB for a converter with resolution N ($N=2^n$) is:

$$t = -TC \times \ln(1 - \frac{V_S - 1/2\,LSB}{V_S}) = -TC \times \ln(\frac{LSB}{2V_S}) = TC \times \ln(\frac{2V_S}{LSB}) = TC \times \ln(\frac{2 \times N \times LSB}{LSB})$$

$$\boxed{t = TC \times \ln(2 \times N)}$$

This therefore sets a maximum limit on the source impedance when driving into a capacitive ladder ADC. The maximum I/O CLK frequency for the TLV1544/8 is 8 MHz (this results with 6 I/O CLK cycles into 0.75 μs sampling time). To achieve this high sampling frequency, the source resistance has to be smaller than 800 Ω.

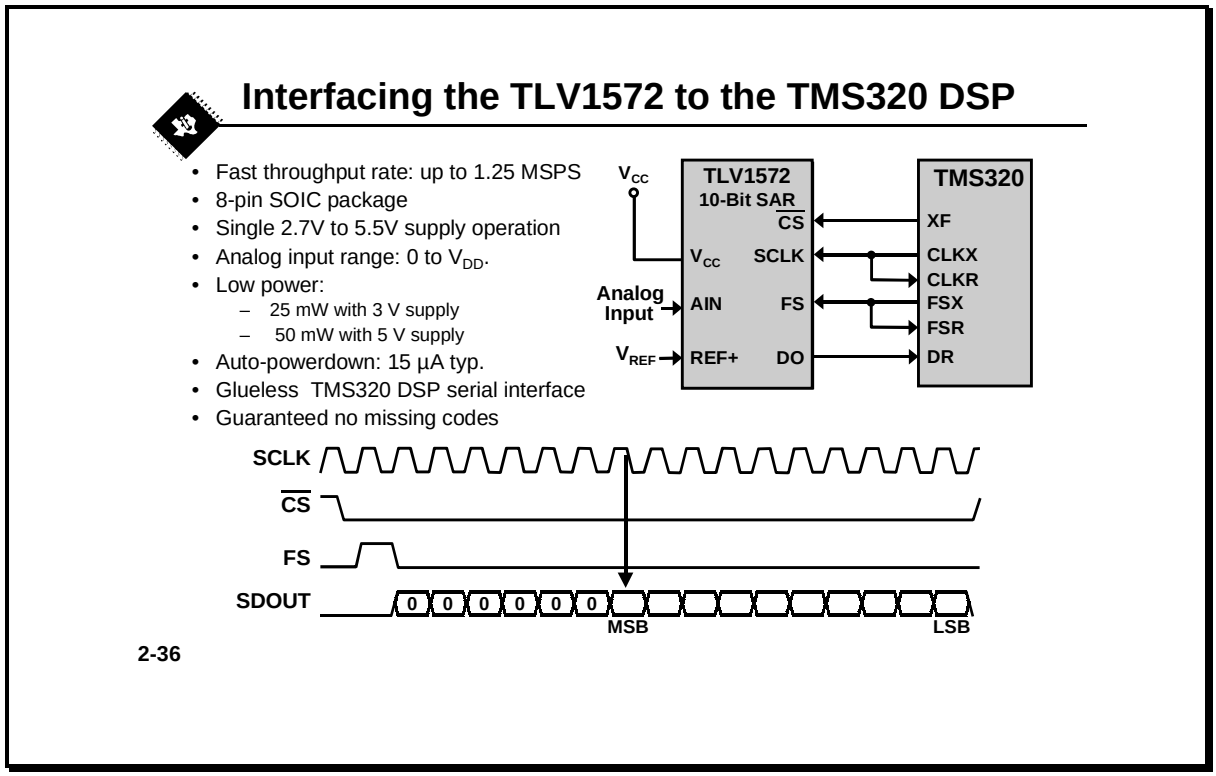


Extended Sampling Operation of the TLV1544/8

The extended sampling mode of operation programs the acquisition time (t_{ACQ}) of the sample-and-hold circuit. This allows the analog inputs of the device to be directly interfaced to a wide range of input source impedances. Power consumption for the extended sampling mode depends on the duration of the sampling period chosen.

The CSTART signal controls the sampling period and starts the conversion. The falling edge of CSTART initiates the sampling period of a preset channel. The low time of CSTART controls the acquisition time of the input sample-and- hold circuit. The sample is held on the rising edge of CSTART. Asserting CSTART causes the converter to perform a new sample of the signal on the selected valid MUX channel (one of eight) and discard the current conversion result ready for output. Sampling continues as long as CSTART is active (negative). The rising edge of CSTART ends the sampling cycle. The conversion cycle starts two internal system clocks after the rising edge of CSTART. Immunity to digital noise is improved since the extended sampling mode acquires the input signal when the digital circuitry is shut down.

Once the conversion is complete, the processor can initiate a normal I/O cycle to read the conversion result and select the input channel for the next conversion.



Interfacing the TLV1572 to the TMS320 DSP

The TLV1572 is a 10-bit, 1.25 Msps successive approximation analog-to-digital converter, which has one analog input channel (AIN), a chip-select (CS), serial clock (SCLK) and a serial data output. An additional input called frame sync (FS) initiates the data transfer when using a DSP and connects to the DSP serial port FSX pin. A high level on the CS pin disables the device, puts it in a power down mode and switches DATA OUT to high impedance. When taken low, CS enables the device inputs, but no data is transferred until the falling edge of FSX is received from the DSP to FS. After the falling edge of DSP FSX, the TLV1572 starts shifting the data out on the DO line. After six null bits, the 10 bit A/D conversion data becomes available.

Selection Guide: Successive Approximation ADCs

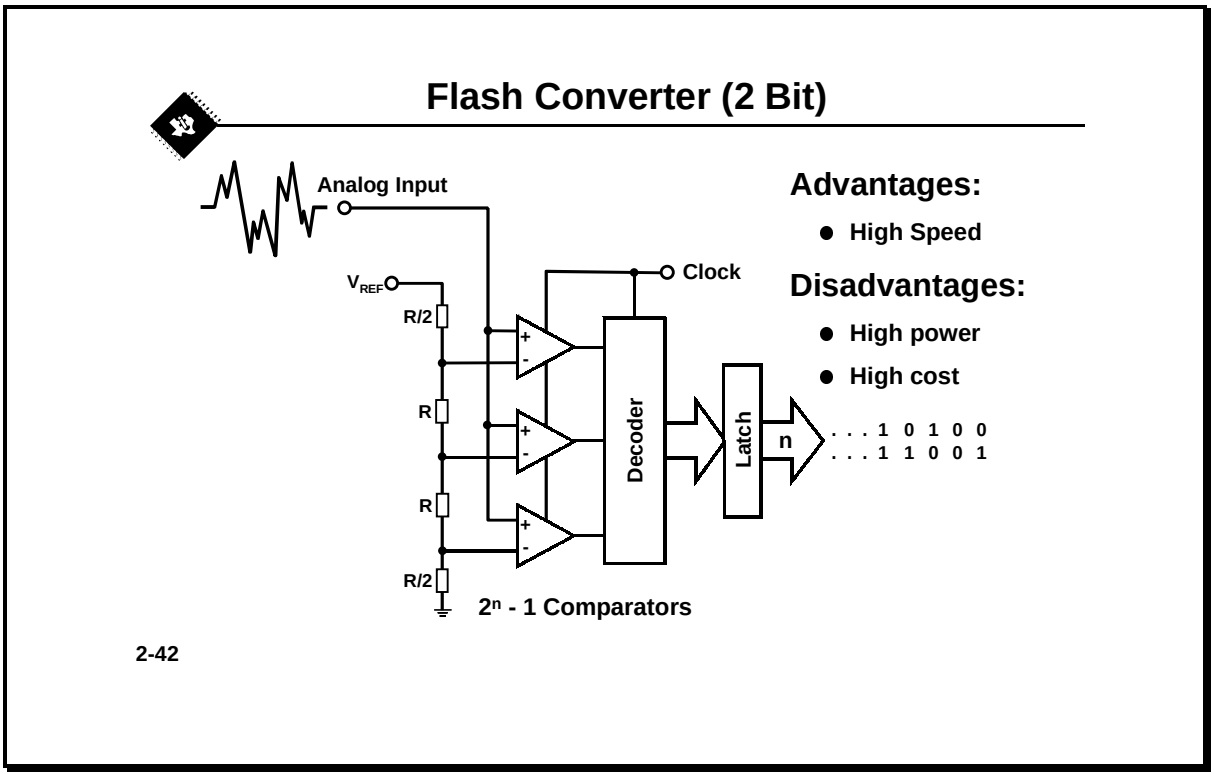
Successive Approximation ADC's

Part Number	Linearity [LSB]	Conversion Time [us]	Sampling Rate [kSPS]	Number of Inputs	Power Supply [V]	Parallel or Serial Output	Internal Clock	Powerdown	Power Consumption [mW]
10-bit Analog-to-Digital Converters									
TLC1540	±0.5	21	32	11	5	S			12
TLC1541	±1.0	21	32	11	5	S			12
TLC1542	±1.0	21	38	11	5	S	Y		12
TLC1543	±1.0	21	38	11	5	S	Y		12
TLC1549	±1.0	21	38	1	5	S	Y		12
TLV1543	±1.0	21	38	11	3.3	S	Y		12
TLV1544	±1.0	10	66	4	3 -5	S	Y	Y	3
TLV1548	±1.0	10	66	8	3 - 5	S	Y	Y	3
TLV1549	±1.0	21	38	1	3.3	S	Y		8
TLC1550	±0.5	6	164	1	5	P	Y		40
TLC1551	±1.0	6	164	1	5	P	Y		40
TLV1570	±0.5	0.8	1250	8	2.7-3.6	S		Y	21
TLV1572	±0.5	0.8	1250	1	3 - 5	S		Y	20
12-bit Analog-to-Digital Converters									
TLC2543	±1.0	10	66	11	5	S	Y	Y	12.5
TLV2543	±1.0	10	66	11	3.3	S	Y	Y	12.5

Successive Approximation ADC's

Part Number	Linearity [LSB]	Conversion Time [us]	Sampling Rate [kSPS]	Number of Inputs	Power Supply [V]	Parallel or Serial Output	Internal Clock	Powerdown	Power Consumption [mW]
Serial Output ADCs									
8-bit Analog-to-Digital Converters									
TLC0831	±1.0	13.3	28	1	5	S			12.5
TLC0832	±1.0	13.3	28	2	5	S			26
TLC0834	±1.0	13.3	28	4	5	S			12.5
TLC0838	±1.0	13.3	22	8	5	S			12.5
TLC540	±0.5	9	75	11	5	S			12
TLC541	±0.5	17	40	11	5	S			12
TLC542	±0.5	20	25	11	5	S	Y		10
TLC545	±0.5	9	76	19	5	S			12
TLC546	±0.5	17	40	19	5	S			12
TLC548	±0.5	17	45.5	1	5	S	Y		12
TLC549	±0.5	17	40	1	5	S	Y		12
TLV0831	±1.0	13.3	28	1	5	S			2.5
TLV0832	±1.0	13.3	28	2	5	S			8.25
TLV0834	±1.0	13.3	28	4	5	S			2.5
TLV0838	±1.0	13.3	22	8	5	S			2.5

Flash/Pipeline Converters



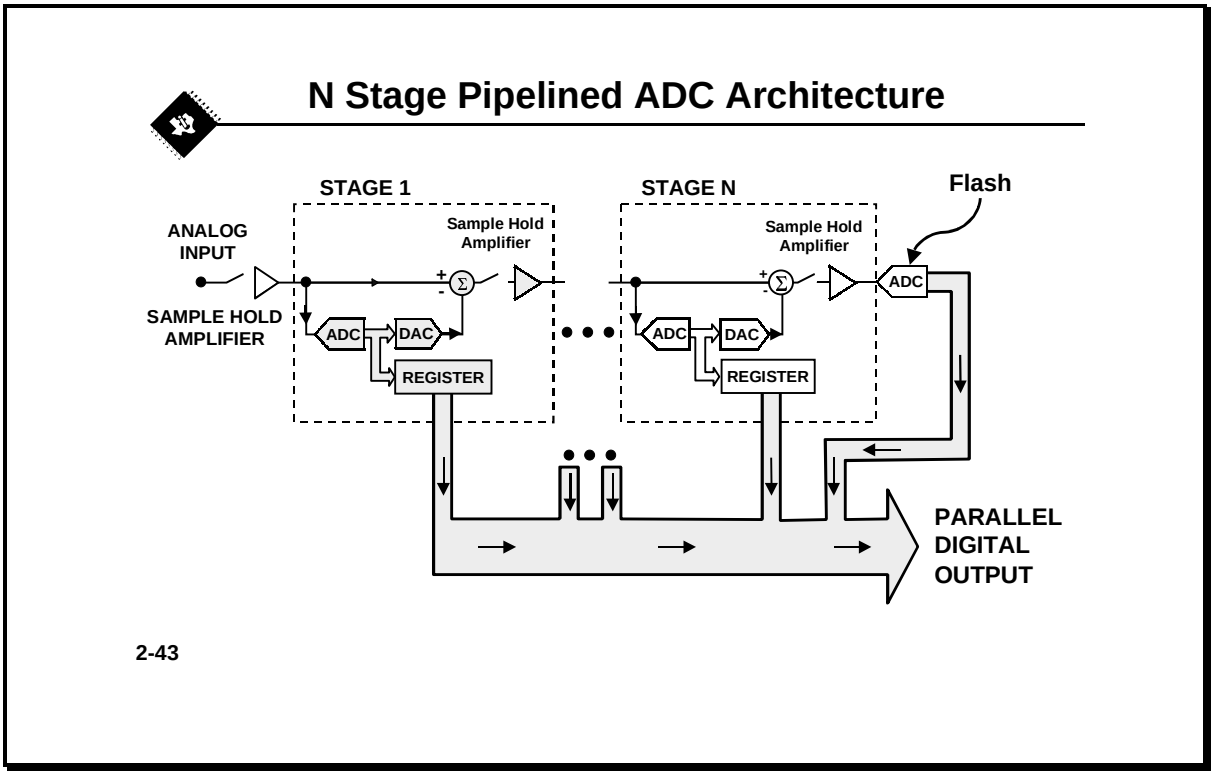
Flash Converter (2 Bit)

The flash analog to digital converter provides the fastest conversion method today. This is achieved by a simultaneous comparison of the analog input signal with 2^n–1 reference voltages. These reference voltages are generated with a voltage divider, which is built by a resistor chain. Each reference voltage is connected to the inverting input of a comparator. Again, for an n-bit resolution, 2^n–1 comparators are required with threshold voltages varying by 1 LSB. The analog input signal is connected to the noninverting input of every comparator. The output is low for every comparator where the analog input signal is smaller than the reference voltage. The output is high for every comparator where the analog input signal is higher than the reference voltage. The decoded digital output data, which is n bits wide, is written into a latch.

As previously mentioned, flash converters have been favored for achieving high sample rates. However, the flash method requires 2^n-1 comparators to implement an n-bit converter. This means that 255 comparators are needed for an 8-bit ADC and 4095 comparators for a 12 bit flash converter. Flash converters therefore occupy a relatively large area of silicon, require a lot of power, have a high input capacitance and are expensive.

A technology, which reduces the number of comparators, is the semi-flash converter. The semi-flash concept is first to digitize the upper 4 bits, which are fairly insensitive to noise. The converted 4 bits are then input to a 4 bit DAC, and subtracted from the original analog input, to create a residue voltage. This residue is then digitized to provide the lower 4 bits of information. For an 8-bit

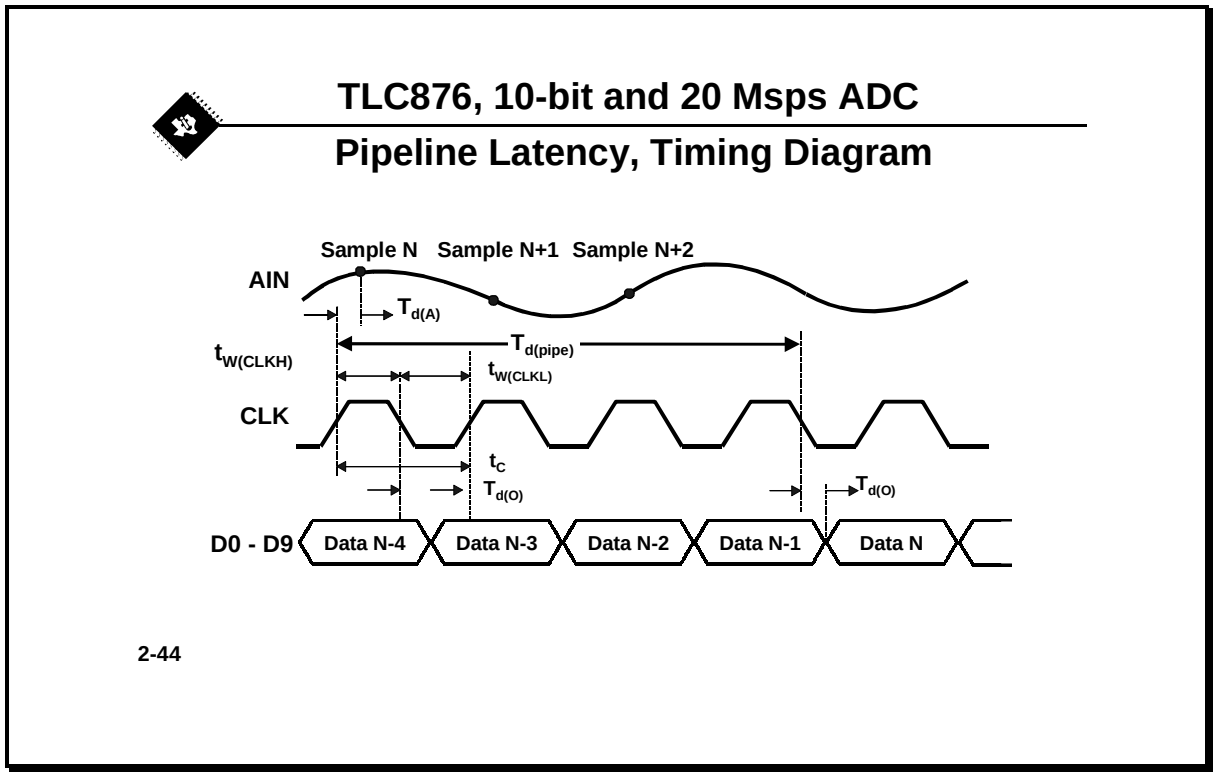
converter, this architecture can be implemented with 31 comparators, (an 8x reduction from the flash ADC). This yields improvements in cost, power and input capacitance. The semi-flash architecture is a popular choice for 8 bit, 20 MSPS ADCs. The TLC0820, TLC5510, TLC5733 and TLC5540 from Texas Instruments are all good examples.



N Stage Pipelined ADC Architecture

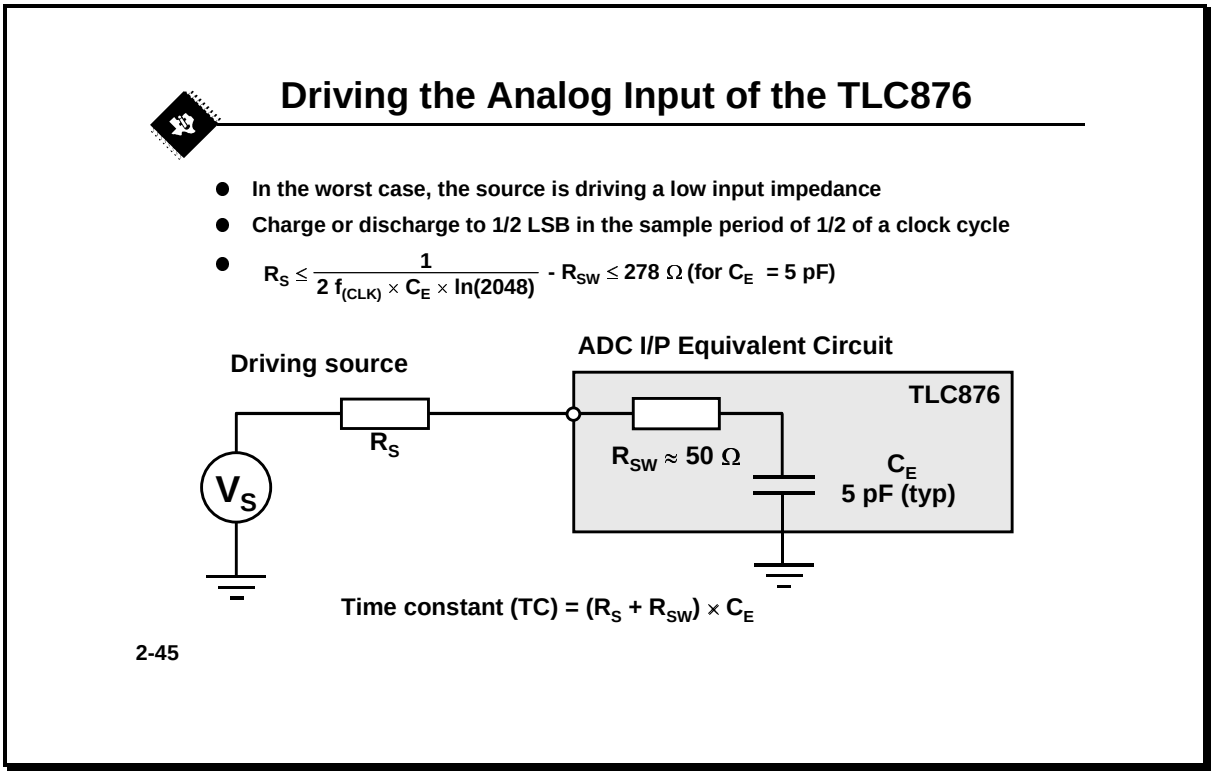
Higher sample rates than successive approximation techniques can be achieved cost effectively by using the pipelined architecture. The functional block diagram of this conversion method is shown in the picture. It consists of a number of individual n-bit resolution (typically n = 2 or 4) converter stages which are cascaded to form the complete converter. Each stage comprises of an n-bit ADC, an n-bit DAC, a sample/hold amplifier and a data register. The sample/hold should be N bits accurate where N is the resolution of the overall ADC. For a semi-flash (or 2 step) architecture, this is usually done in 2 stages. For an 8 bit ADC, the upper 4 bits are converted then the lower 4 bits.

The ADC operates as follows. The analog input signal is sampled and held. The first stage produces the first n MSBs of the overall ADC conversion result. This n-bit result is then reconverted back into analog form via the n-bit DAC and is subtracted from the held input signal level. The result of this subtraction is then sampled and held. The next stage then repeats the process performed by the previous stage and this in turn is repeated for subsequent stages. The instant that the result of the subtraction of stage 1 is successfully held, the preceding sample/hold amplifier acquires the next sample of the input signal. This allows the individual n-bit conversions to occur serially in time. Thus the throughput rate of the overall ADC is increased significantly. In addition, the chip area is significantly reduced from that which would be needed with a full Flash architecture. The pipeline or semi-flash will produce an output for each clock once the pipeline is filled. The number of clocks to fill the pipeline is referred to as latency. For the TI 8 bit semi-flash ADCs, the latency is 2.5 clock periods.



TLC876 Pipeline Latency – Timing Diagram

The principle of a pipeline ADC has been explained. The TLC876 uses a multistage pipelined architecture. This pipelined multistage architecture achieves a high sample rate with low power consumption. However, such architecture causes a pipeline latency, which is the number of clock cycles between the conversion initiation on an input sample and the corresponding output data. Once the data pipeline is full, new valid output data are provided every clock cycle. The picture shows a pipeline latency of 3.5 clock cycles for the TLC876.



Driving the Analog Input of the TLC876

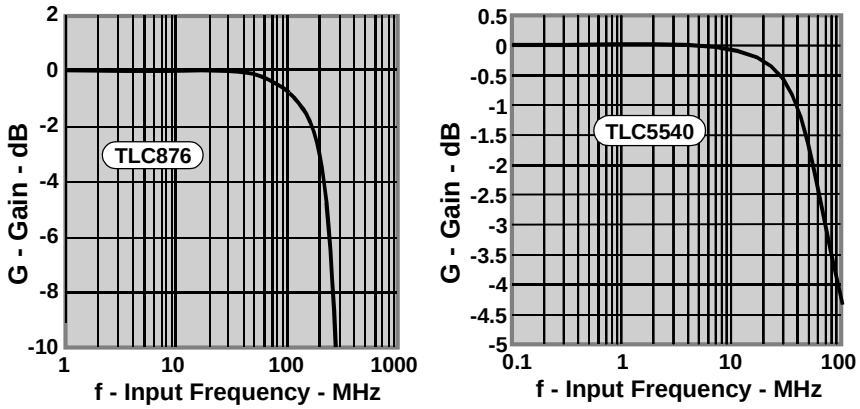
The picture shows an equivalent input circuit of the TLC876 sample-and-hold amplifier. The total equivalent capacitance, C_E, is typically less than 5 pF and the input source must be able to charge or discharge this capacitance to 10-bit accuracy in the sample period of one half of a clock cycle. When the switch S1 closes, the input source must charge or discharge the capacitor C_E from the voltage already stored on C_E (the previously captured sample) to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the switch resistance R_{SW} (50 Ω) of S1 and quickly settle (within 1/2 CLK period), and, therefore, the source is driving a low input impedance. However, when the source voltage equals the value previously stored on C_E, the hold capacitor requires no input current to maintain the charge and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN terminal reduces the drive requirements placed on the source. To maintain the frequency performance outlined in the specifications, the resistor should be limited to 200 Ω minus the source resistance or less. The maximum source resistance, R_S, for 10-bit, 1/2 LSB accuracy can be calculated by using the equation, already derived: $t = TC \times \ln(2 \times n) = TC \times \ln(2 \times Resolution)$

Therefore, R_S is given by:

$$R_S \le \frac{1}{2 f_{(CLK)} \times C_E \times \ln(2048)} - R_{SW}$$

Analog Input Bandwidth of the TLC876 (10-bit, 20 Msps), TLC5540 (8-bit 40 Msps)



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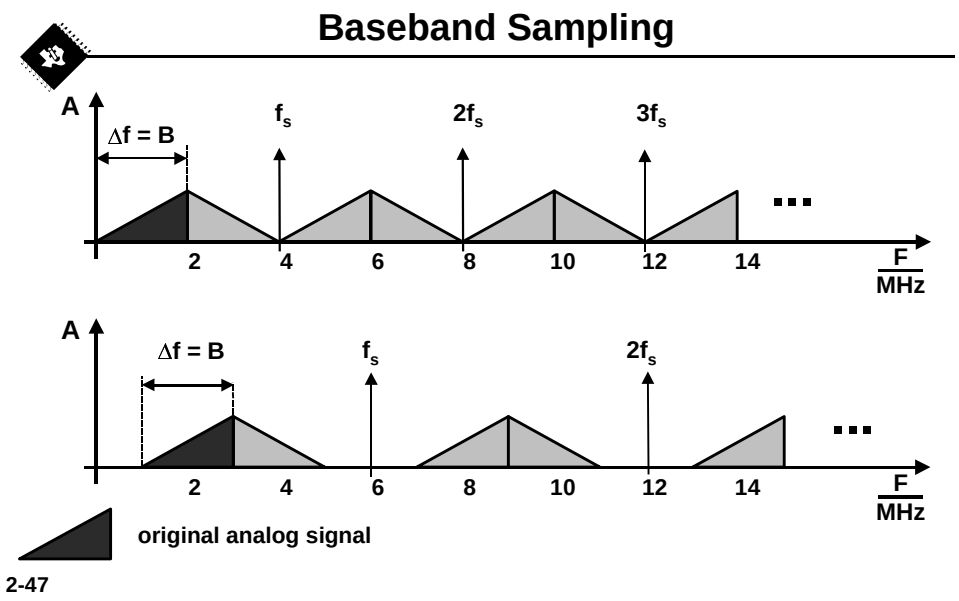
Analog Input Bandwidth of the TLC876, TLC5540

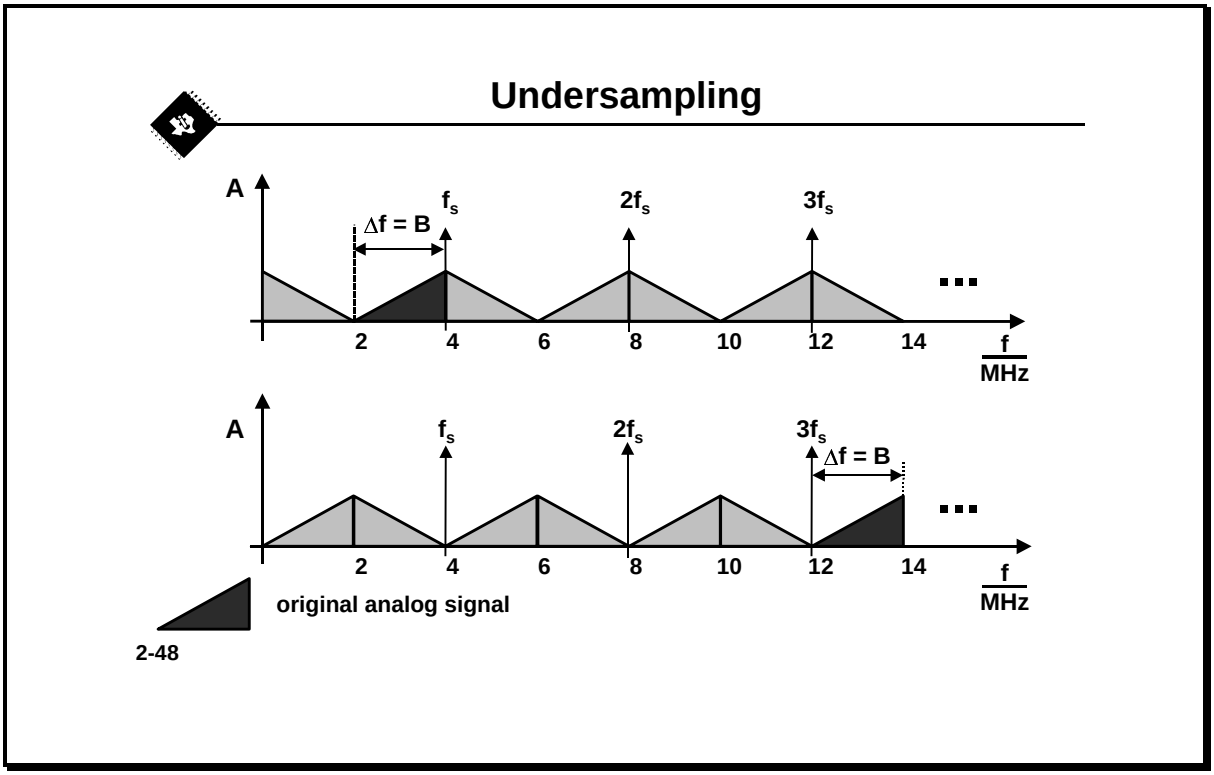
TLC876 (10-bit, 20 Msps), TLC5540 (8-bit 40 Msps)

As already discussed the analog input bandwidth of an A/D converter is very important for undersampling applications. An example is shown for the TLC876, a 10-bit, 20 Msps A/D converter. The typical analog input bandwidth of this device is 200 MHz, which makes the device well suited for undersampling applications. A further example is shown for the 40 Msps ADC TLC5540, which has a typical analog input bandwidth of 75 MHz.



Baseband Sampling

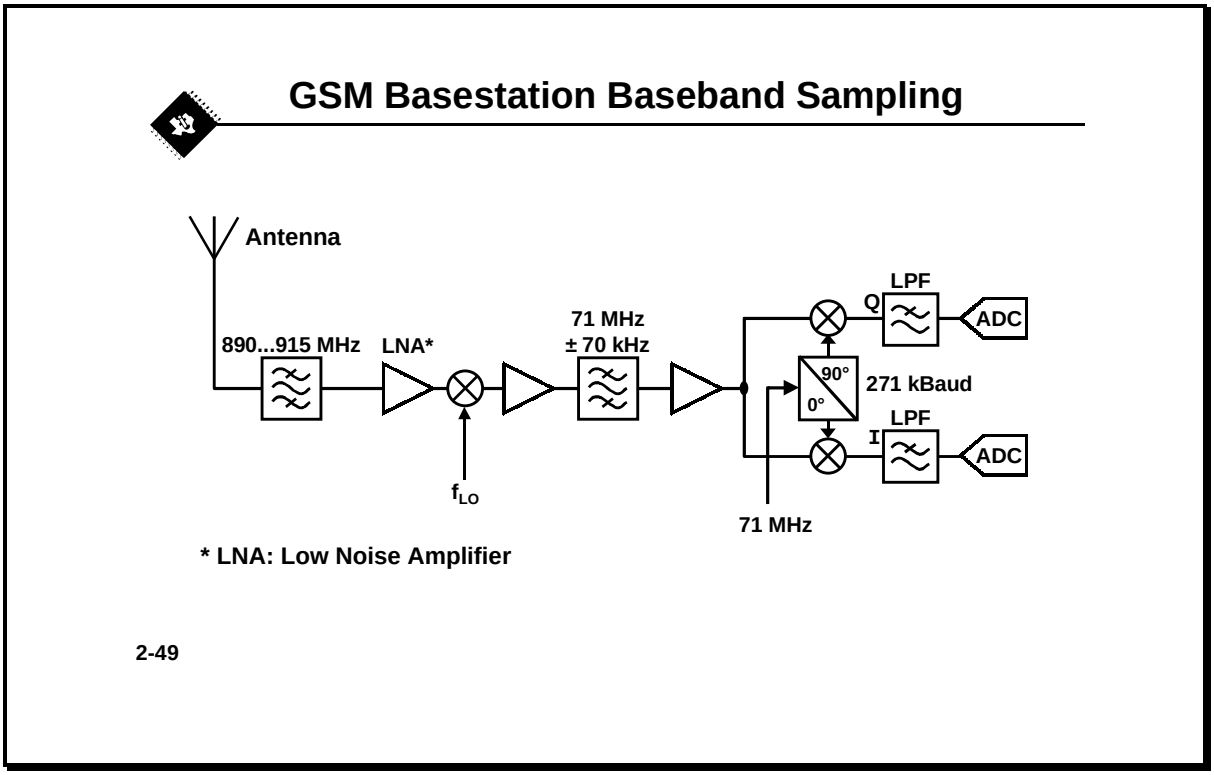
Baseband sampling is the type of conversion commonly used. In baseband sampling the actual frequency of the signal to convert does not exceed $f_s/2$. Nyquist's criteria states that the bandwidth (not the actual frequency) of the signal being converted should not exceed $f_s/2$ in order for the information to be preserved. When the actual frequency of the signal to be converted exceeds $f_s/2$ but the bandwidth does not exceed $f_s/2$ then this is called undersampling (or Super-Nyquist).



Undersampling

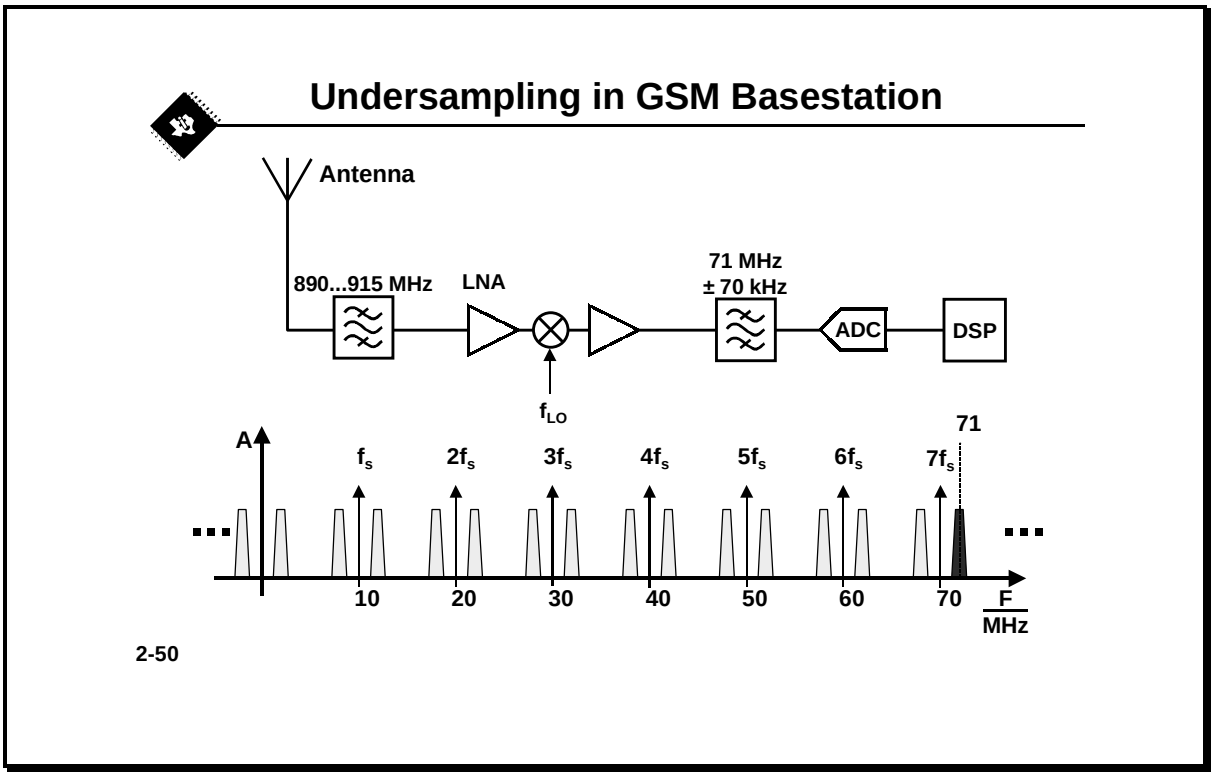
Undersampling is quite often not well understood. In most cases it is assumed that the analog input signal in front of an ADC has to be limited to less than one half of the sampling frequency of the converter. However, the ADC can convert the analog signal into the right digital signal, if only the bandwidth of the analog signal is limited. This means that a signal in the frequency area above the sampling frequency of the ADC can be converted, if the bandwidth is limited. An example of this is an analog signal with a bandwidth of 100 kHz, which is centered at 10 MHz. Without using undersampling the minimum sampling frequency is 20 MHz. If undersampling is used, the minimum sampling frequency in this example is only 20 kHz. Another advantage especially in high frequency systems is that the number of analog components, like downmixers, can be reduced.

A further big advantage is that the applied speed to the ADC and system can be reduced.



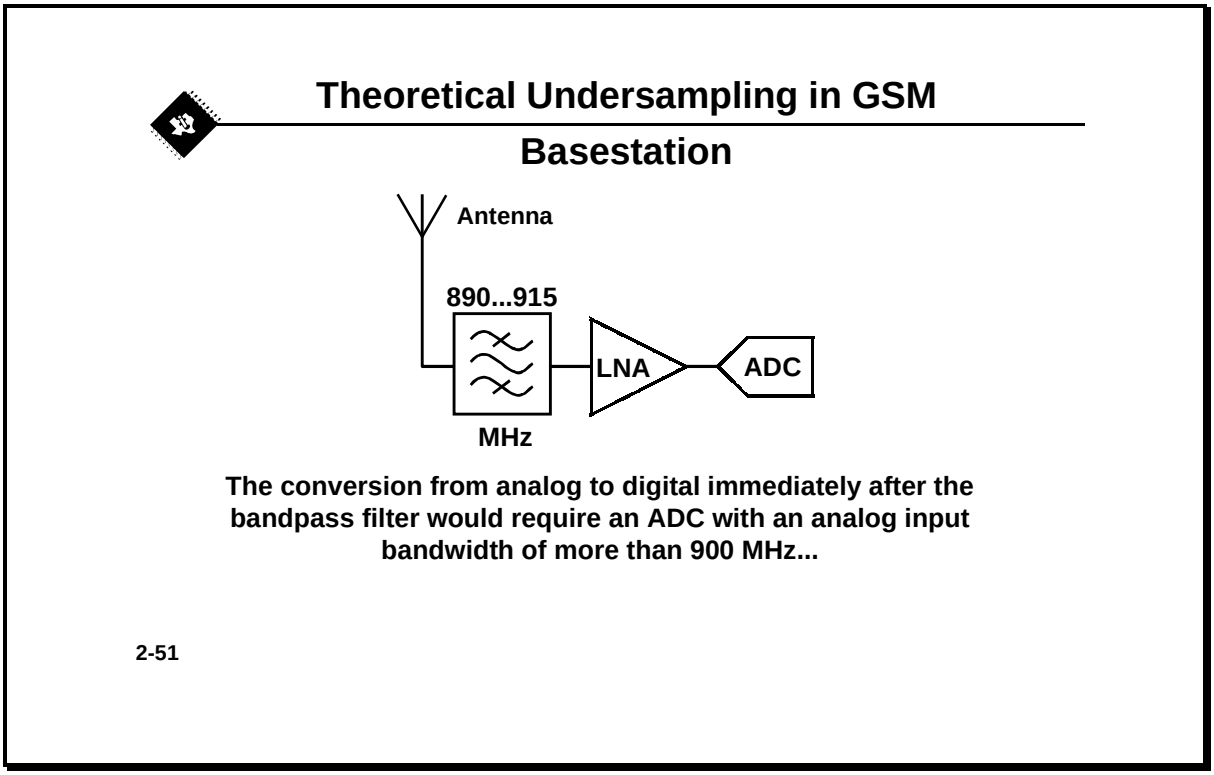
GSM Basestation Baseband Sampling

The picture shows a conventional GSM basestation baseband sampling system. The frequency of interest is in the range of 890 to 915 MHz. This range is filtered with a bandpass filter and amplified by a LNA (Low Noise Amplifier). The amplified frequency is mixed down to the IF frequency of 71 MHz ± 70 kHz. The IF signal is then applied to a quadrature demodulator where the I and Q components are separated. The baseband I(t) and Q(t) signals are then applied to the inputs of A/D converters. The digitized data is further handled by a DSP.



Undersampling in GSM Basestation

Today, the intention is to do more and more of the signal processing in the digital domain by using a DSP. Therefore, the ADC moves more and more in the direction of the antenna. The advantage in this example is that the analog I/Q demodulation can be performed digitally. Instead of converting the IF signal using a conventional I and Q demodulator, the IF 71 MHz IF signal is digitized. The band of interest is in this case around 140 kHz. By using undersampling technology, it is not necessary to sample at 140 MHz. The ADC can be operated at a sampling frequency of 10 or 20 Msps. The ADC actually functions as a mixer and aliases the signal down.



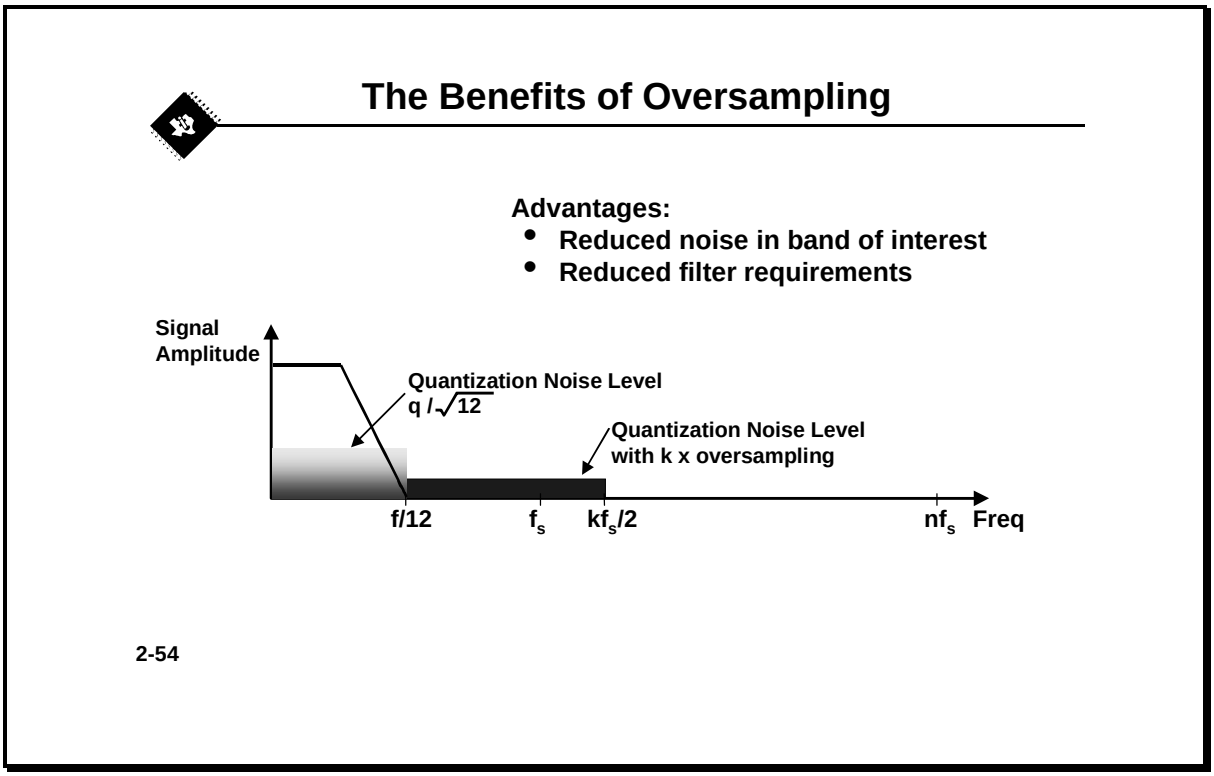
Theoretical Undersampling in GSM Basestation

The intention in undersampling applications is to bring the A/D converter as near as possible to the RF antenna of the system. However, this is actually still a problem because of the high analog input bandwidth in combination with the required resolution of the A/D converter. In GSM systems an analog input bandwidth of more than 900 MHz would be required. These bandwidth and resolution requirements are beyond the limits of current technology.

Selection Guide: Flash/Pipeline ADCs

Flash/Pipeline ADC's

Part Number	Linearity [LSB]	Conversion Time [µs]	Sampling Rate [Msps]	Number of Inputs	Power Supply [V]	Parallel or Serial Output	Internal Clock	Powerdown	Power Consumption [mW]
Video and High Speed ADCs									
6-bit Analog-to-Digital Converters									
TL5501	±0.5	0.050	20	1	5	P	N	N	300
8-bit Analog-to-Digital Converters									
TLC5510	±0.75	0.050	20	1	5	P	N	N	90
TLC5510A	±0.75	0.050	20	1	5	P	N	N	90
TLV5510	±1.0	0.100	10	1	3	P	N	N	60
TLC5540	±0.75	0.025	40	1	5	P	N	N	150
TLC5733A	±0.75	0.050	20	3	5	P	N	N	375
10-bit Analog-to-Digital Converters									
TLC876	±0.5	0.050	20	1	5	P	N	Y	110



The Benefits of Oversampling

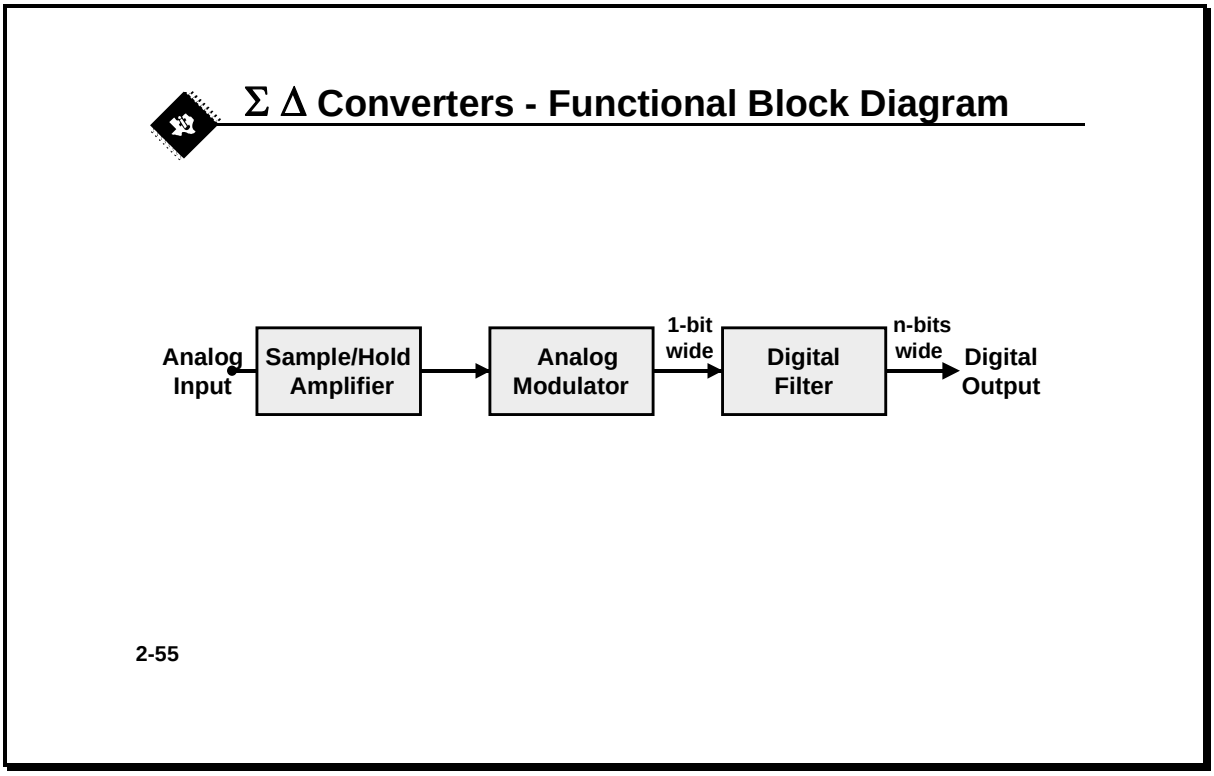
An ADC which is sampling an input signal at the Nyquist rate (twice the maximum input bandwidth) will produce a quantization noise, or error, of $\frac{q}{\sqrt{12}}$ (where q is the width of one step of the converter) within the signal band of $f_s/2$. This is illustrated in the figure. Comparing this quantization noise with the amplitude of a sinewave input we find that the theoretical signal to noise ratio (SNR) is given by the expression

$$\text{Theoretical SNR} = 6.02 \times n + 1.76 \text{ dB}$$

where n is the resolution of the ADC.

For example, the SNR of a 12 bit ADC has a theoretical upper limit of 74 dB. Using the same equation we find that the theoretical SNR of a 1-bit ADC, sampling at the Nyquist rate, fs (2 × maximum input frequency of interest) is as high as 7.78 dB!

If we now increase the sampling rate from f_s to some multiple, kf_s, we find that the same total amount of quantization noise is spread over a wider bandwidth, $kf_s/2$ as shown in the figure above. This has the effect of reducing the amount of noise in the signal band of interest. The quantization noise, which now appears outside of the signal band, can be filtered out. This has the overall effect of increasing the resultant SNR in the band of interest. The benefits of oversampling are used to produce excellent performance in sigma-delta converters.



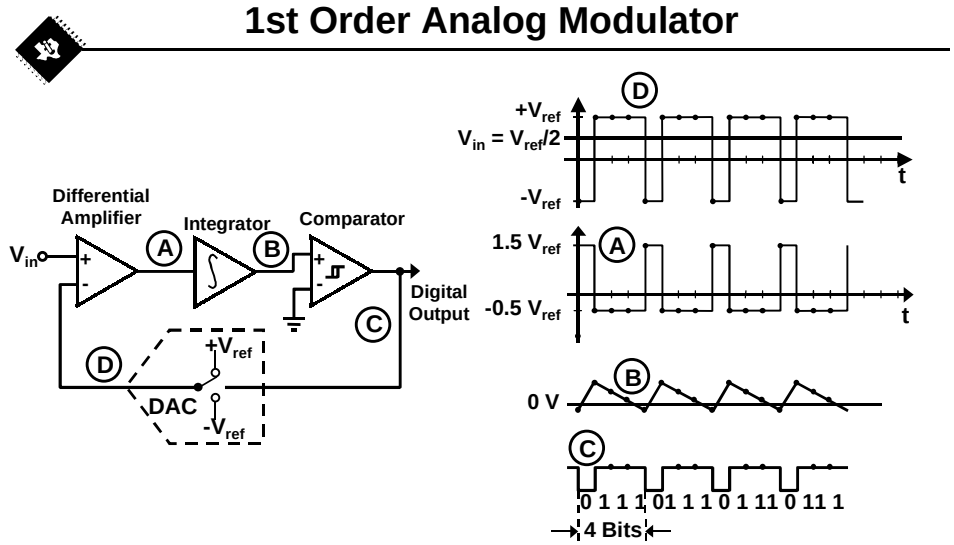
Sigma-Delta Converters – Functional Block Diagram

The simplified structure of a Sigma-Delta ADC is shown in the figure above and comprises an analog modulator and a digital filter. The analog modulator, running at a high sampling rate, converts the input signal at its output to a 1-bit pulse density modulated bit stream. The digital filter takes this bit stream and simultaneously removes out of band noise and reduces the bit rate while increasing the output word width.

To increase resolution the analog modulator not only oversamples the input signal but also shapes the quantization noise so it appears in the unwanted band to be removed by the digital filter.

The one bit quantization in the analog modulator provides low differential non-linearity and hence no missing codes in the output. The high input sampling rate means only a non-critical anti-aliasing filter is required and a sample and hold is not required.

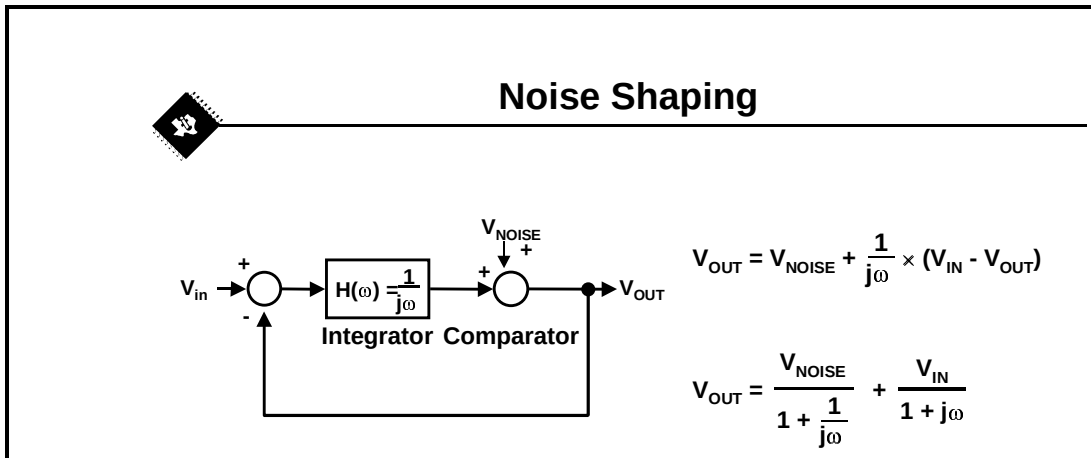
The resolution of a Sigma-Delta converter is determined from its output signal to noise ratio.



1st Order Modulator

The analog modulator performs the actual analog to digital conversion process. In its simplest form this consists of a differential amplifier, single integrator, comparator and 1-bit DAC connected in a closed loop configuration as shown in the figure above which illustrates a 1st Order modulator. The analog modulator converts the analog input signal into a 1-bit wide serial digital output.

The analog input voltage should not exceed the limits of $+V_{ref}$ and $-V_{ref}$. An example of the modulator operation is given for an analog input voltage of $V_{in} = +V_{ref}/2$ and where the starting conditions are: output voltage of the integrator $V_B < 0$ (therefore the output of the comparator is 0), DAC output $V_D = -V_{ref}$. Therefore, the voltage at the output of the differential amplifier is: $V_A = V_{in} - V_D = 1.5\ V_{ref}$. In this situation, the integrator integrates up and as soon as the output voltage of the integrator exceeds 0 V, the output of the comparator switches to 1. Therefore, the DAC output switches from $-V_{ref}$ to $+V_{ref}$ and the output of the differential amplifier becomes: $V_A = V_{in} - V_D = -0.5\ V_{ref}$. The integrator-input voltage is therefore negative and the integrator now integrates down.



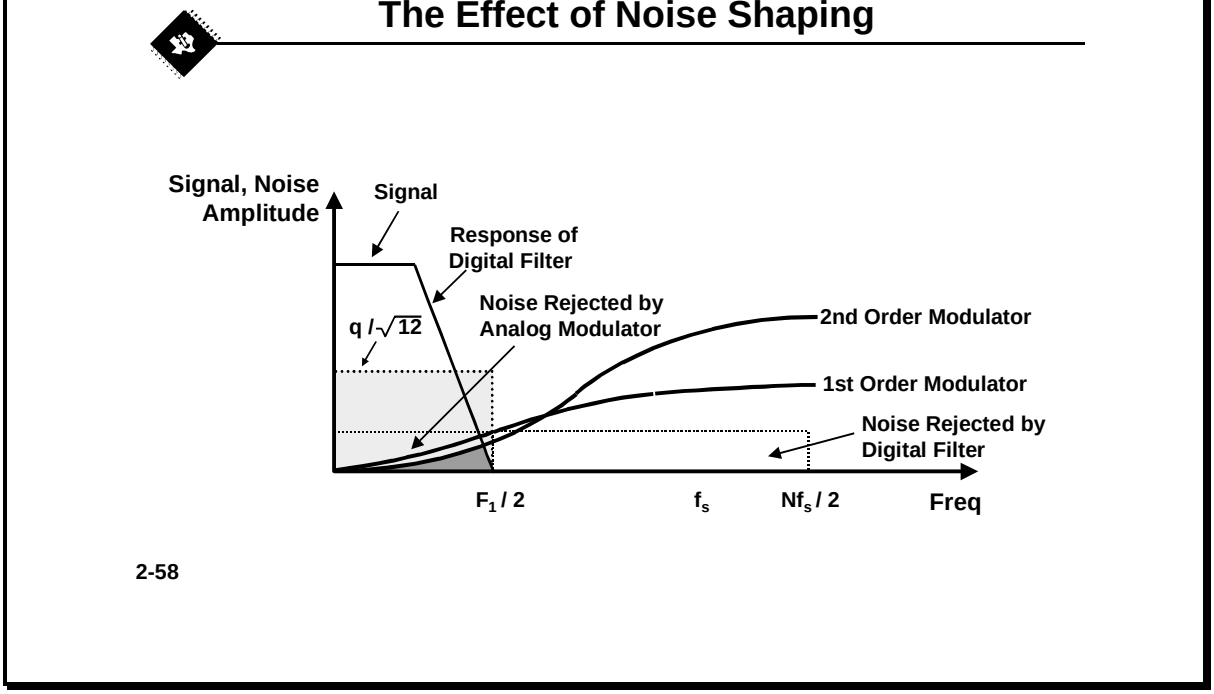
Noise Shaping

The modulator also shapes the quantization noise within the signal frequency band. This has the effect of pushing a significant percentage of the quantization noise out of the band of interest where it can be filtered by the digital filter. This effect can be derived mathematically. As visible in the picture of the analog modulator loop, the comparator is simplified to a quantization noise source. Therefore, the response of the analog modulator can be written as:

$$V_{OUT} = V_{NOISE} + \frac{1}{j\omega} \times (V_{IN} - V_{OUT}) \text{, or}$$

$$V_{OUT} = \frac{V_{NOISE}}{1 + \frac{1}{j\omega}} + \frac{V_{IN}}{1 + j\omega}$$

The analog modulator represents a low pass filter for the analog input signal and a high pass filter for the quantization noise.

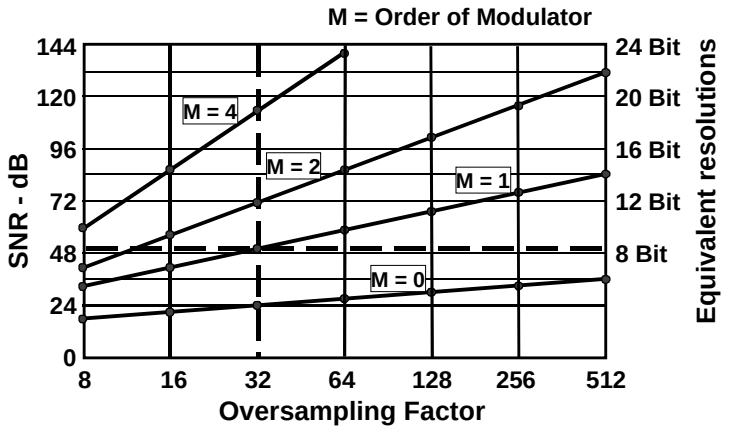


The Effect of Noise Shaping

The number of integrators, which are included, determines the order of the modulator. The higher the order of the modulator the greater the amount of quantization noise which is pushed out of band. Higher order analog modulators enable increased resolution converters offering enhanced signal to noise ratios to be produced, without the need to increase the oversampling rate. The effect of noise shaping produced by 1st and 2nd order modulators can be seen in the figure above.

The idea of increasing the order of the modulator to a high number sufficient to achieve any desired resolution and SNR is an attractive one. Unfortunately there is rarely gain without some pain. Higher order modulators tend to be more difficult to stabilize. Most sigma-delta converters tend to use modulators, which are 5th order or less.

Resolution of Sigma-Delta Converters



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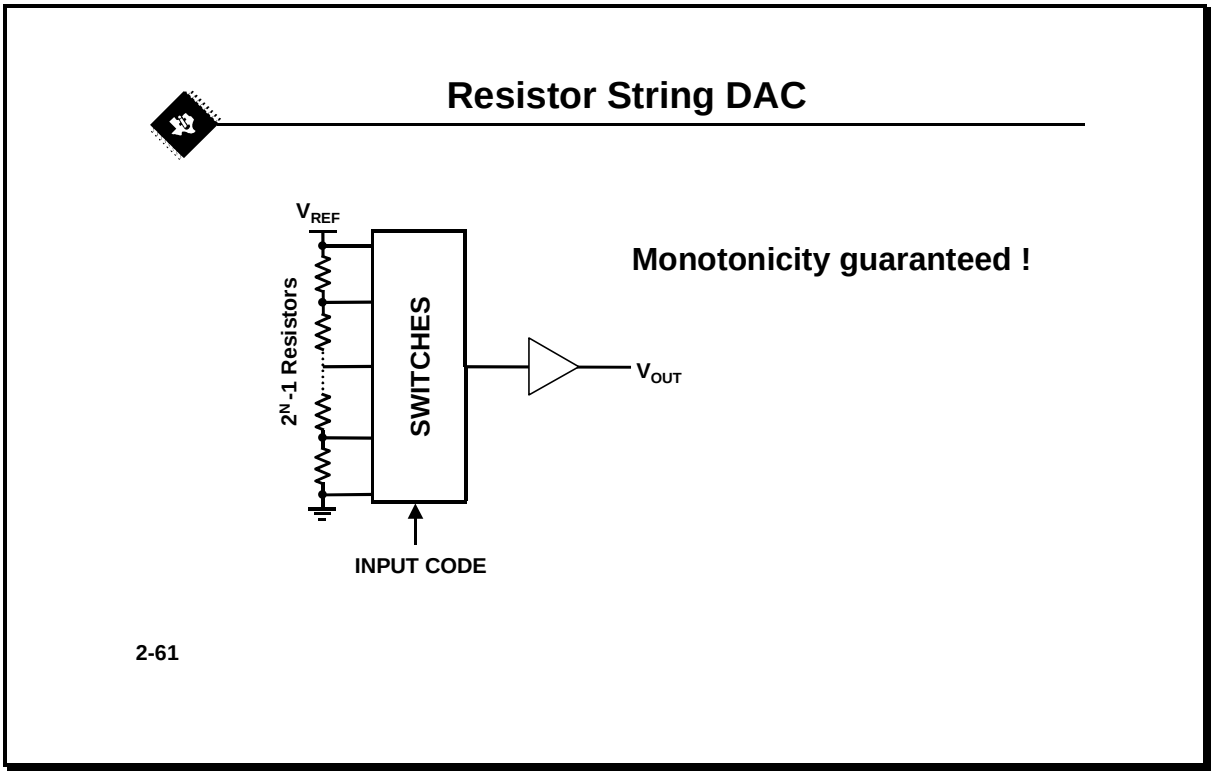
Resolution of Sigma-Delta Converters

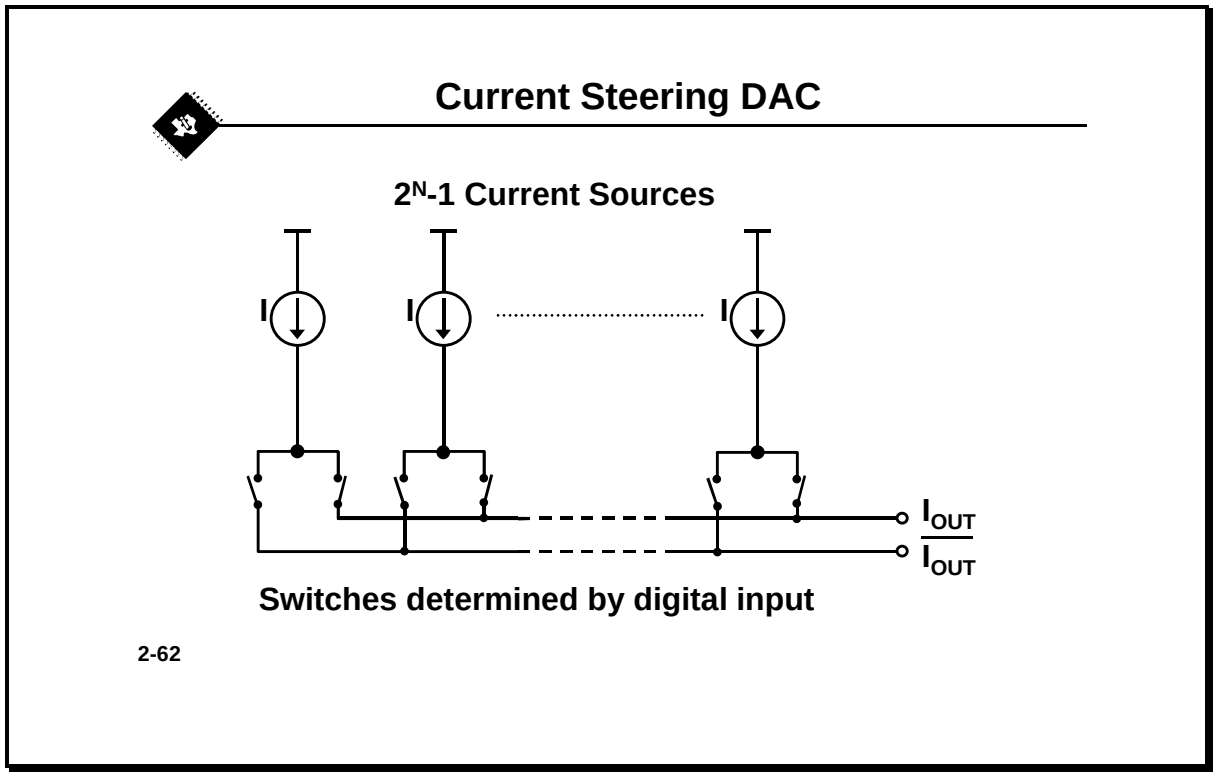
The graphic shows the performance of a Sigma-Delta converter in terms of resolution depending on the oversampling factor and the order of the modulator. As an example, a Sigma-Delta converter with a first order modulator is considered. The SNR is about 50 dB, which equivalent to an ADC with a resolution of 8 bit. A move from the first order modulator to a second order modulator increases the SNR to about 70 dB, which is then equivalent to approximately 11 to 12 bits of resolution. In addition, the higher the oversampling the higher the resolution.

D/A Converters



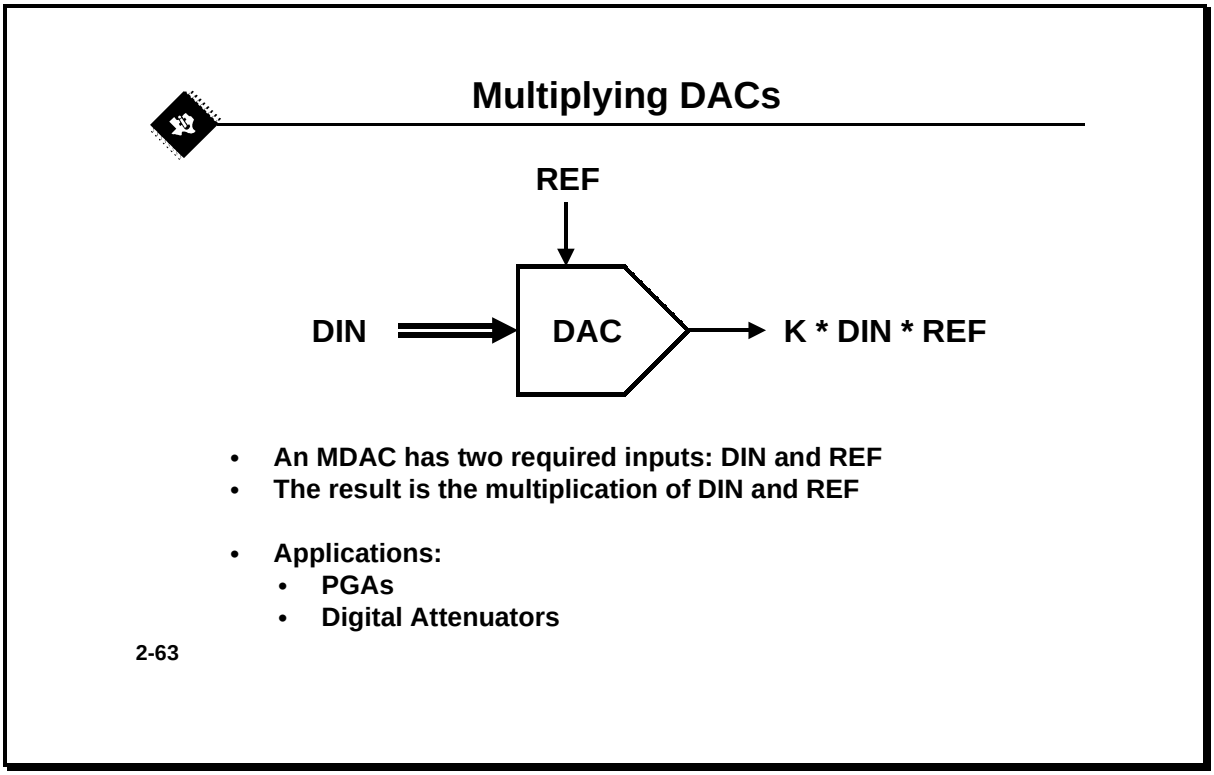
Resistor String DACs

In a Resistor String architecture, the reference voltage is divided into 2^N - 1 parts, each exactly one LSB high. A network of switches selects the output voltage from the resistor string, depending on the digital input code. To avoid errors due to a load current, a buffer is required on the DAC output. This buffer is usually part of the DAC. The big advantages of this architecture are, that the transfer function is always monotonic and that the design is relatively simple. The disadvantages are, that 2^N - 1 matching resistors are required, which limit the achievable resolution and that this architecture needs an amplifier (buffer), which limits the achievable speed.



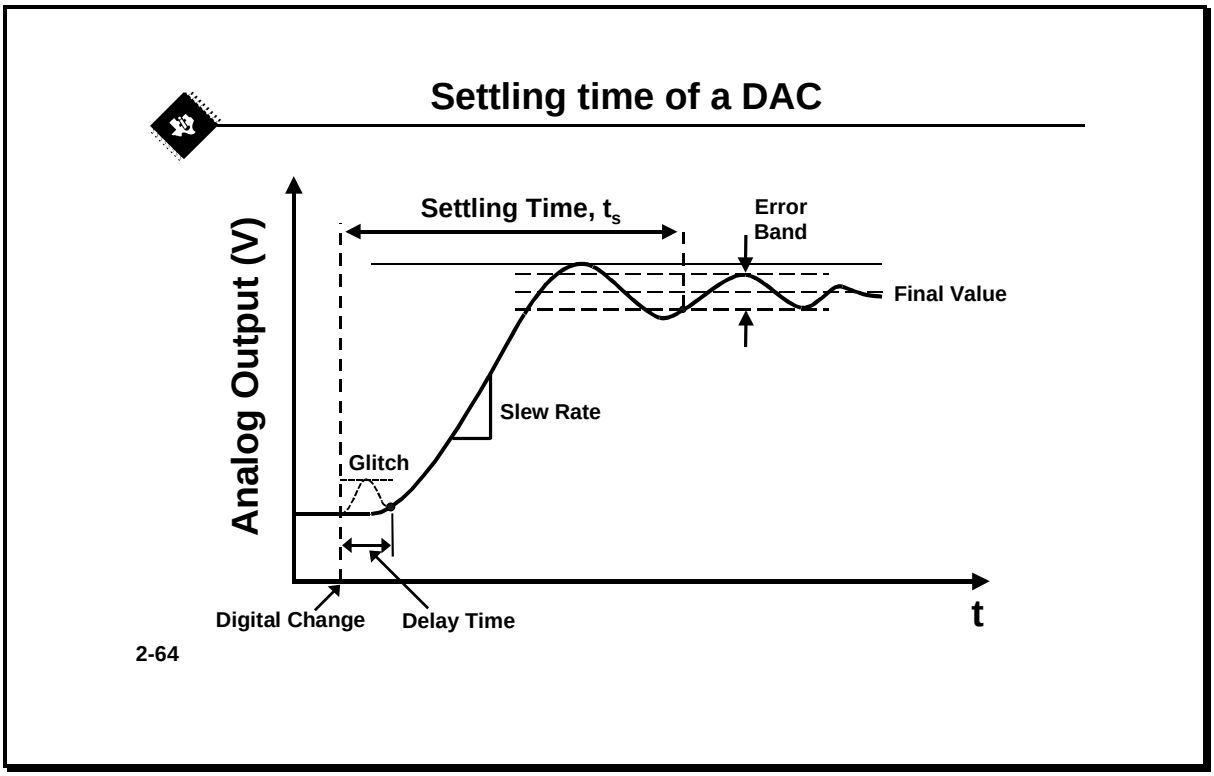
Current Steering DAC

A Current Steering DAC is based on switched current sources. It has two current outputs, with one providing the complementary current of the other. The sum of the output currents is always constant. An array of switches, which is controlled by the digital input, directs the current of the sources to one of the two output rails. Like the resistor string architecture, current steering also guarantees monotonicity. And it allows much higher speeds, than designs with voltage outputs.



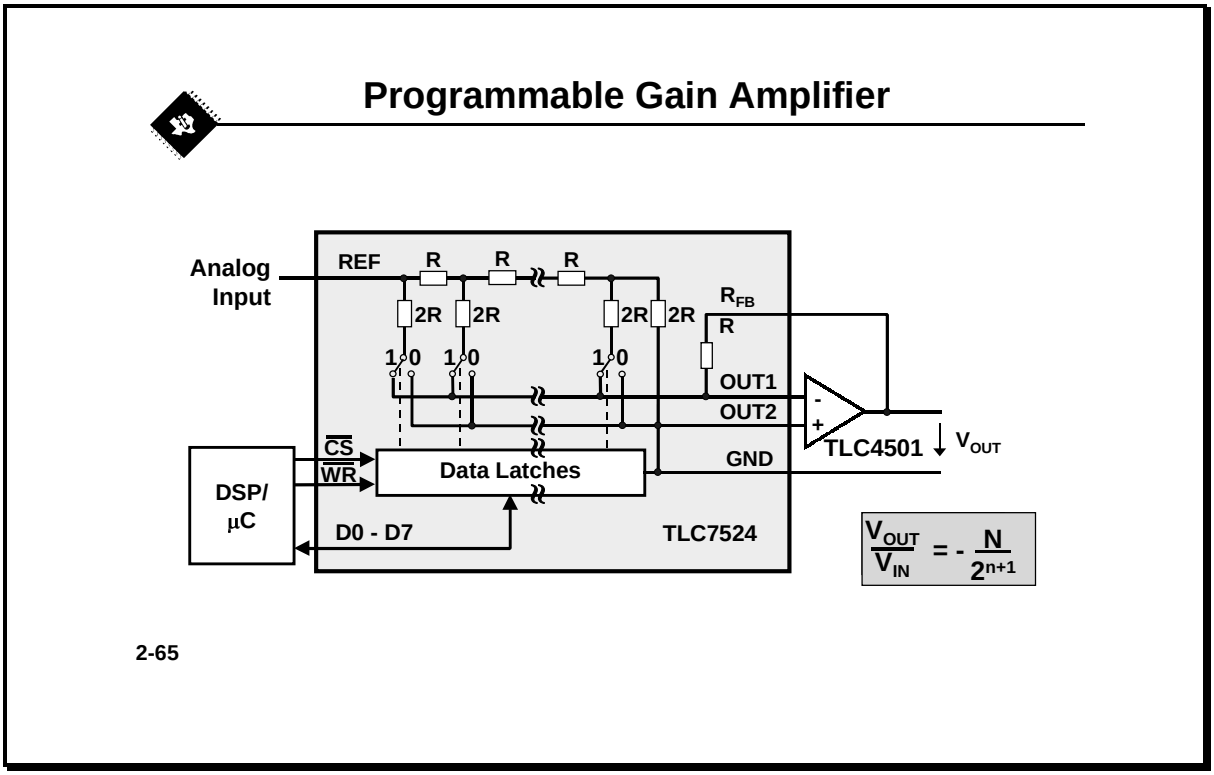
Multiplying DACs

Besides the input for the digital data, a multiplying DAC always has a dedicated input for the reference. Unlike non-multiplying DACs, which allow only a narrow band for the reference, MDACs are intended to handle signals over a specified voltage and frequency range on the reference input. The output of the MDAC is equal to the multiplication of the signal on the reference input and the input code. Depending on the reference voltage range and the input code range, the MDAC operates in specific quadrants. If both the reference and the digital input can have negative and positive values, then the MDAC operates in all four quadrants.



Settling Time of a D/A Converter

The settling time of a D/A-converter is the time between the switching of the digital inputs of the converter and the time when the output reaches its final value and remains within a specified error band. The settling time is a very important parameter, because this must be faster than the signal frequency in order to be able to reconstruct the waveform. The picture shows also a possible glitch in the waveform of a DAC. This glitch is an undesirable transient in the analog output occurring following a code change at the digital input. If a current output DAC is used with an external amplifier, then a ferrite bead can be used to minimize the glitch by minimizing the switching current.

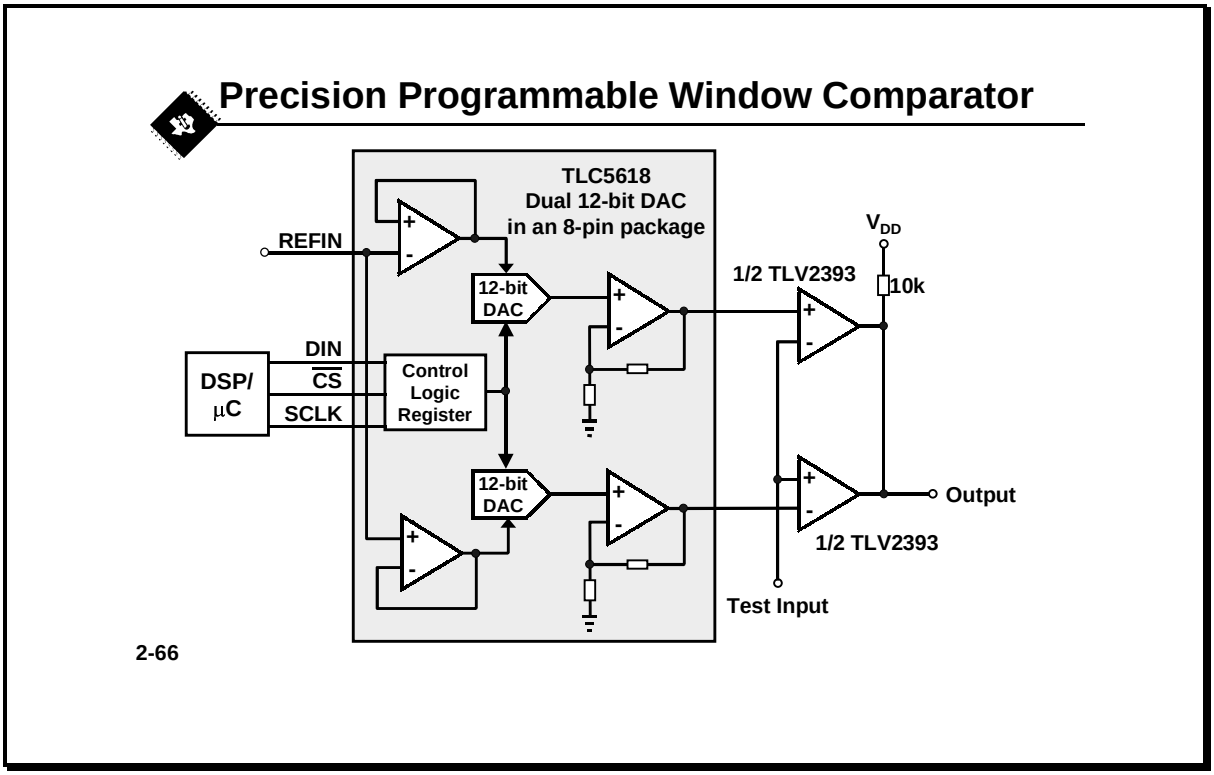


Programmable Gain Amplifier

A D/A-converter can be used to build up a Programmable Gain Amplifier (PGA). The advantages are that multiple gain levels with high accuracy can be selected via software. The DAC can be seen as a programmable resistance. The picture shows the configuration of a PGA by using the 8 bit DAC TLC7524. The internal resistor R_{FB} is used as a feedback resistor for the external op amp. The analog input voltage is applied to the REF input of the DAC. The input impedance R_I of a DAC in R-2R technology is always 2R. The feedback resistor R_{FB} of the TLC7524 is R ($R_I = 2R_{FB}$) and therefore the transfer function results into:

$$\frac{V_{out}}{V_{in}} = -\frac{N \times R_{FB}}{2^n \times R_I} = -\frac{N}{2^{n+1}}.$$

N in this equation is the decimal input code of the DAC and n is the resolution of the DAC.



Precision Programmable Window Comparator

The figure shows a precision programmable window comparator, which uses a 12-bit dual D/A-converter TLC5618, and a dual open collector comparator TLV2393. The threshold voltages of the comparators are programmed via the D/A-converter. 1 LSB of the TLC5618 corresponds to 1 mV with a reference voltage of 2.048 V and a gain of 2. The input offset voltage of the comparator in this case limits the accuracy of the system.

Low Power DAC Families

TI's New Low Power DAC Family

New TLC/TLV56xx 10-Bit Family

Device	No. of DACs	Settling Time	Clock Rate	Power Dissipation	Internal Voltage Ref.	Serial/Parallel Interface
TLC5615	1	12.5 µs	14 MHz	1.15 mW	No	serial
TLC5617A	2	12.5 / 2.5 µs	20 MHz	3 / 8 mW	No	serial
TLV5604	4	12/3 µs	20 MHz	3 / 8 mW	No	serial
TLV5637*	2	3 / 1 µs	20 MHz	TBD / TBD mW	Yes	serial

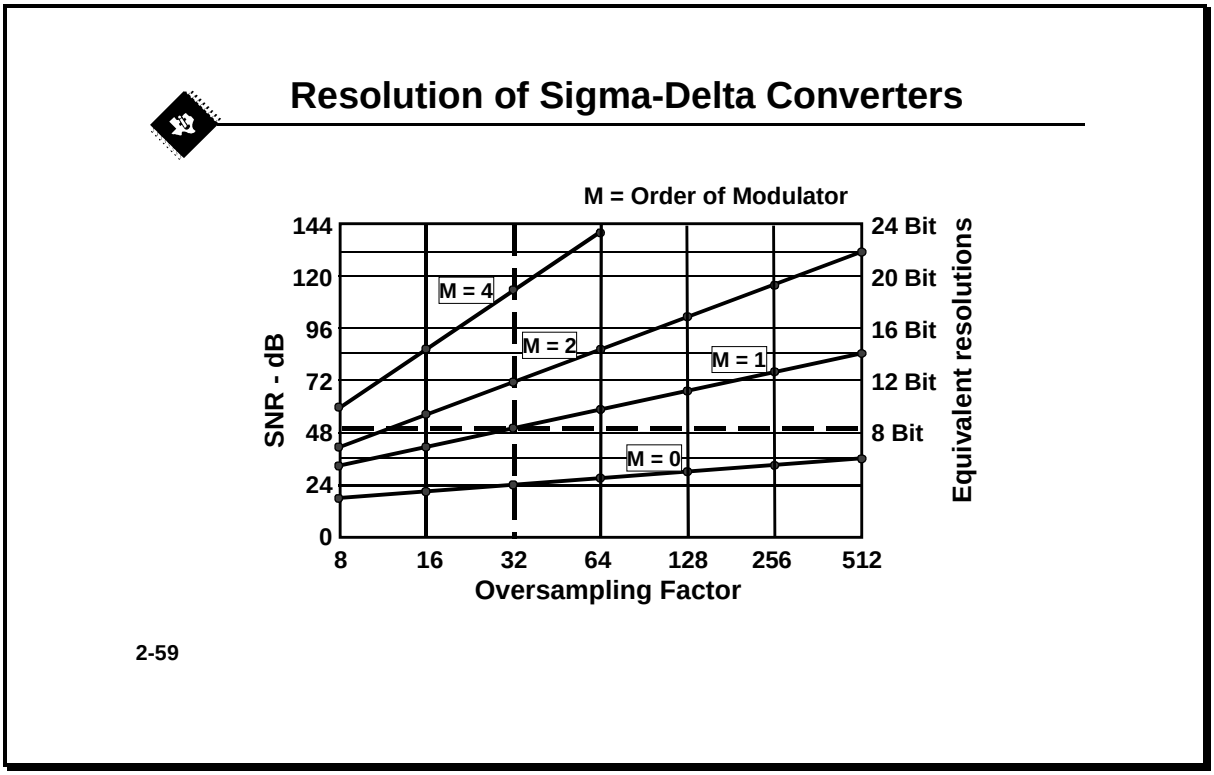
New TLC/TLV56xx 12-Bit Family

Device	No. of DACs	Settling Time	Clock Rate	Power Dissipation	Internal Voltage Ref.	Serial/Parallel Interface
TLV5616	1	8.2 / 2.5 µs	20 MHz	0.6 / 1.7 mW	No	serial
TLV5613	1	3 / 1 µs	---	1.2 / 4.2 mW	No	parallel
TLV5619	1	1 µs	---	4.2 mW	No	parallel
TLC5618A	2	12.5 / 2.5 µs	20 MHz	3 / 8 mW	No	serial
TLV5614	4	12/ 3 µs	20 MHz	3 / 8 mW	No	serial
TLV5636*	1	3 / 1 µs	20 MHz	TBD / TBD mW	Yes	serial
TLV5638*	2	3 / 1 µs	20 MHz	TBD / TBD mW	Yes	serial
TLV5633*	1	3 / 1 µs	---	10 / 20 mW	Yes	8+4 bit parallel
TLV5639*	1	3 / 1 µs	---	10 / 20 mW	Yes	12 bit parallel

2-67 *** Product Preview Only**

Selection Guide: D/A Converters

Part Number	Linearity [LSB]	Parallel or Serial Output	Output (V or I)	Number of DACs	Internal Reference	Settling Time	Power Supply [V]	Conversion Rate [Msps]	Power Consumption [mW]
Video and High Speed DACs									
8-bit Digital-to-Analog Converters									
TLC5602	±0.2	P	V	1	EXT	30ns	5	20	125
TL5632	±0.5	P	V	3	INT	15ns	5	60	450
Video and High Speed DACs									
8-bit Digital-to-Analog Converters									
TLC5620	±1.0	S	V	4	EXT	10µs	5	0.1	10
TLC5628	±1.0	S	V	8	EXT	10µs	5	0.1	20
TLC7225	±1.0	P	V	4	INT	5µs	5-15	0.05	60
TLC7226	±1.0	P	V	4	EXT	5µs	5-15	0.05	60
TLC7524	±0.5	P	I	1	EXT	0.1µs	5-15	10	5
TLC7528	±0.5	P	I	2	EXT	0.1µs	5-15	10	5
TLC7628	±0.5	P	I	2	EXT	0.1µs	10-15	10	20
TLV5620	±1.0	S	V	4	EXT	10µs	3	0.1	6.6
TLV5621	±1.0	S	V	4	EXT	10µs	3	0.1	4.5
TLV5628	±1.0	S	V	8	EXT	10µs	3	0.1	13.2



Analog Interface Circuits for DSP

Analog Interface for DSP

Digital signal processing (DSP) techniques are today being used in a whole range of industrial and consumer products. The advantages of accuracy and repeatability of digital approaches are being utilized in functions ranging from multi-tap filters in communications systems through to precision motor control.

A fundamental requirement which remains necessary, in order to exploit DSP methods, is the conversion of signals from analog into digital and digital into analog form, and the rapid transfer of these conversion results in and out of the DSP. It is important that bottlenecks are avoided in the flow of data between the real world and the computational heart of the DSP. The Analog Interface Circuit (AIC) is a class of mixed-signal products which includes the necessary analog circuit blocks and an optimized interconnection scheme to facilitate the rapid and efficient transfer of information between the analog and digital domains.

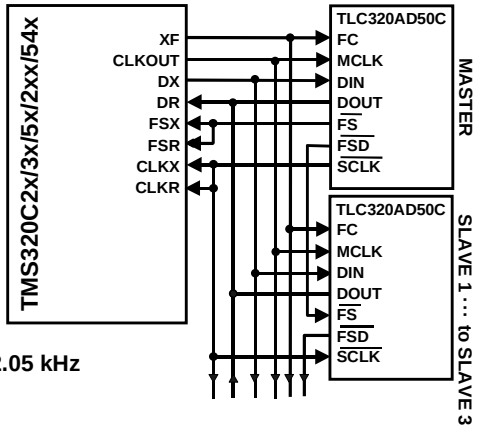
Texas Instruments offers today a growing family of analog interface circuit products. These consist always of A/D and D/A converters generally in sigma-delta technology. The sampling frequency of these circuits is in the range of in voice- and audio applications. The next page gives an overview of the today's available components.

DSP Interface with 16-Bit AIC TLC320AD50

ADC	MIN	TYP	UNIT
SNR (V_i= -1 dB)	85	89	dB
DNR (V_i = -1 dB)		88	dB
THD (V_i = -3 dB)	80	85	dB
THD + N (V_i = -3 dB)	78	82	dB

DAC	MIN	TYP	UNIT
SNR (V_O= 0 dB)	85	89	dB
DNR		88	dB
THD (V_O = -3 dB)	76	80	dB
THD + N (V_O = -3 dB)	75	79	dB

maximum sampling frequency = 22.05 kHz



Up to 4 TLC320AD50 can be connected to one serial port !

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TLC320AD50

The TLC320AD50 is the latest analog interface circuit. The chip consists of sigma-delta A/D and D/A converters with a maximum sampling frequency of 22.05 kHz. The typical performance of the TLC320AD50 is listed in the picture.

In many applications it is important to connect more than one component to a DSP. By using the TLC320AD50 it is possible to connect up to 4 devices on one serial port of a DSP. In this case, one TLC320AD50 operates as the Master which generates the synchronization signal for the digital signal processor (DSP) and the slaves. The slave receives the synchronization signal from the master device. This configuration is shown in the picture. This master-slave technique makes a stereo or multi-channel application easy.

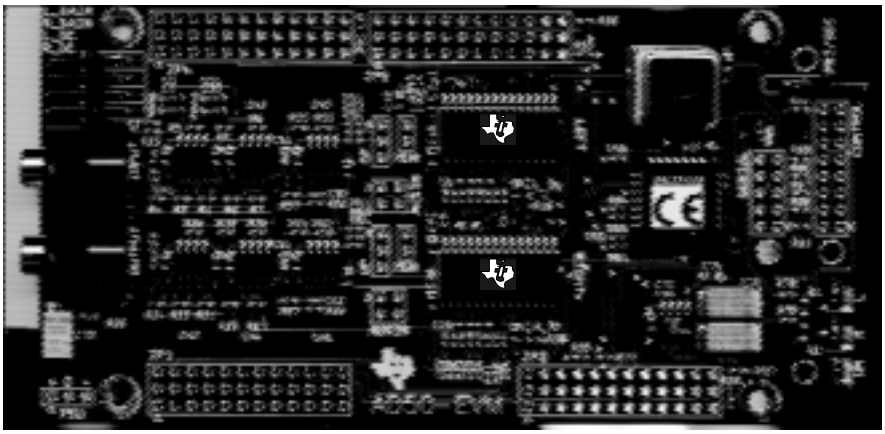
SNR = Signal to Noise Ratio

DNR = Dynamic Range

THD = Total Harmonic Distortion

THD+N = Total Harmonic Distortion plus Noise

TLC320AD50 Evaluation Board



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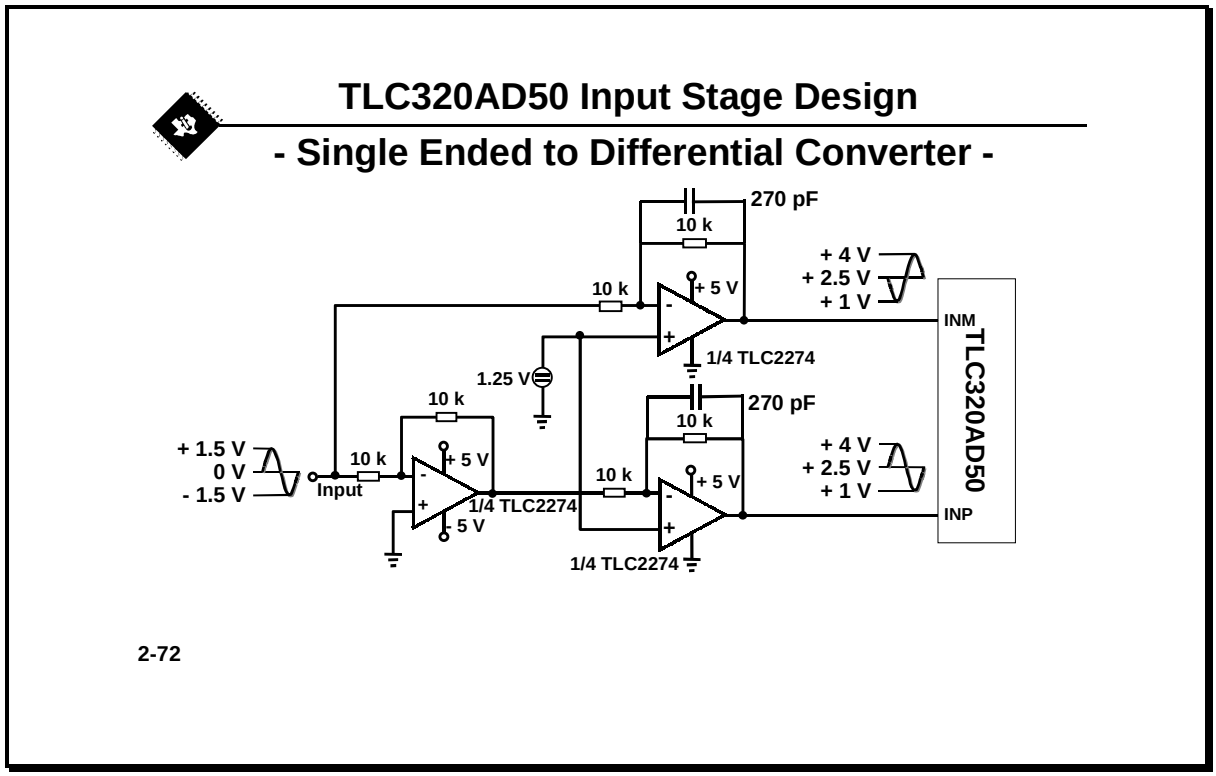
TLC320AD50 Evaluation Board (AD50-EVM)

The AD50-EVM has two AD50 devices for stereo operation. Two AD50-EVMs can be configured as a four-channel system using a single serial interface.

The objective was to design a development board (the AD50-EVM) which would allow prospective users of the AD50 to determine its capabilities with a minimum of effort. The AD50-EVM can be directly connected to the low cost TMS320C54x DSP Starter Kit (DSK+), or to any other system with a compatible synchronous serial interface. Directly compatible DSP devices include TMS320C2x, C2xx, C3x, C5x, C54x and C6xxx.

A demonstration program is provided for the DSK+ development system, which allows the board to be used as a sine-wave generator, or to output samples read in from the ADC onto the DAC. In this echo mode, signal-processing functions such as filtering can easily be included. The AD50-EVM board was also interfaced to a TMS320C25 development board, which was used to transfer analog data to a personal computer running real-time FFT spectrum analysis software. This system was used to prepare the ADC and DAC FFT spectrograms shown in this seminar.

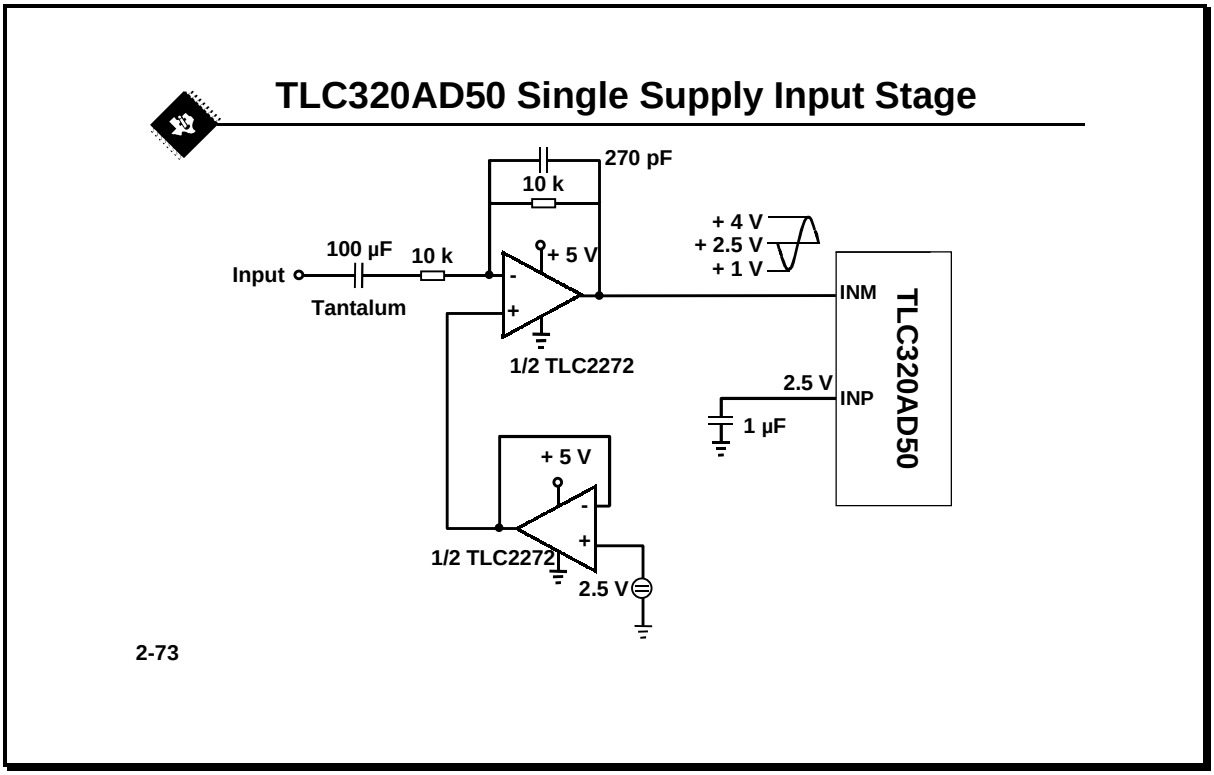


TLC320AD50 Input Stage Design, Single Ended to Differential Converter

The A/D converter of the TLC320AD50 features a differential input structure. Therefore, a single ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD50 to achieve the best possible performance. The differential inputs are biased at 2.5 V. A maximum code is generated with a 3 V_{PP} signal on both differential inputs. The circuit diagram shows such a single ended to differential converter, where the first op amp inverts the incoming signal to provide a differential signal. The second op amps perform the necessary level shifting. The noninverting inputs of these op amps are biased with 1.25 V, which results in an output voltage range from1 V up to 4 V with an input voltage range from –1.5 V to 1.5 V. The first op amp needs a bipolar voltage supply because of the bipolar input voltage range; the second need only a single supply.

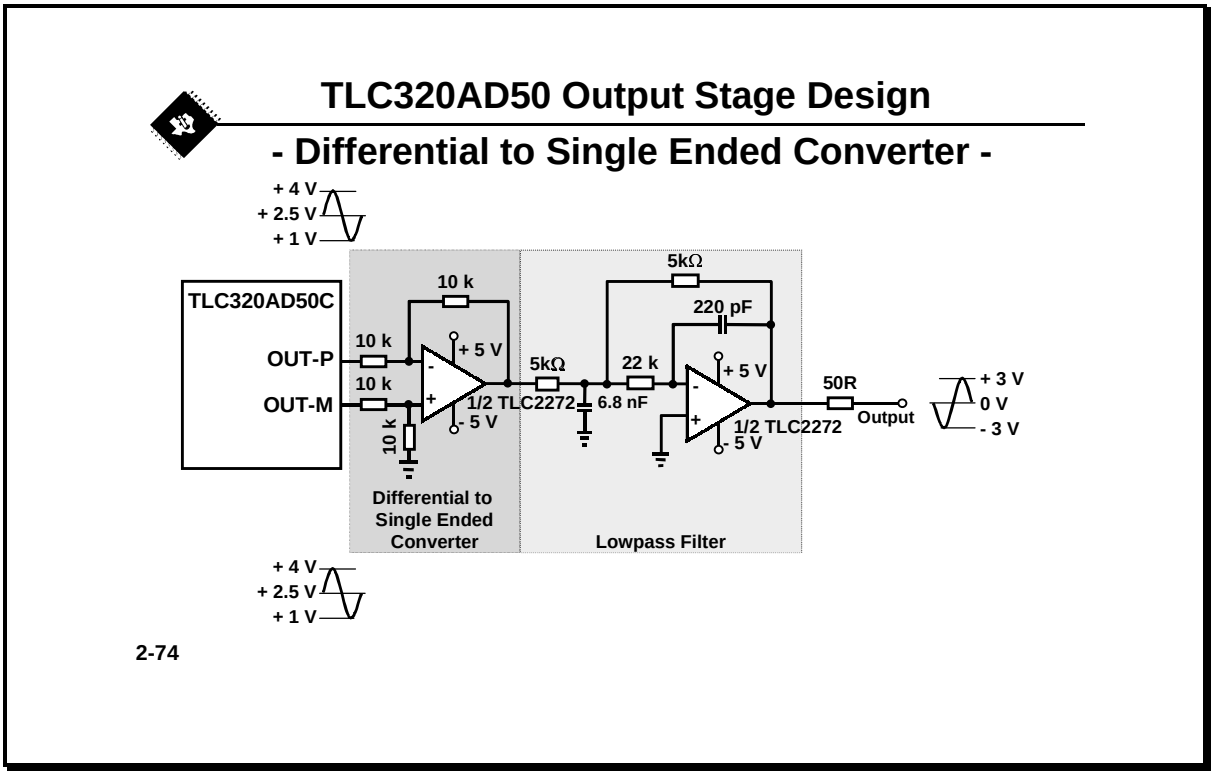
The bias voltage of 1.25 V is derived with a resistive divider on the AD50-EVM.

To obtain the same gain for both differential channels it is recommended a resistor network array be used to achieve a very high accuracy in each of the resistors.



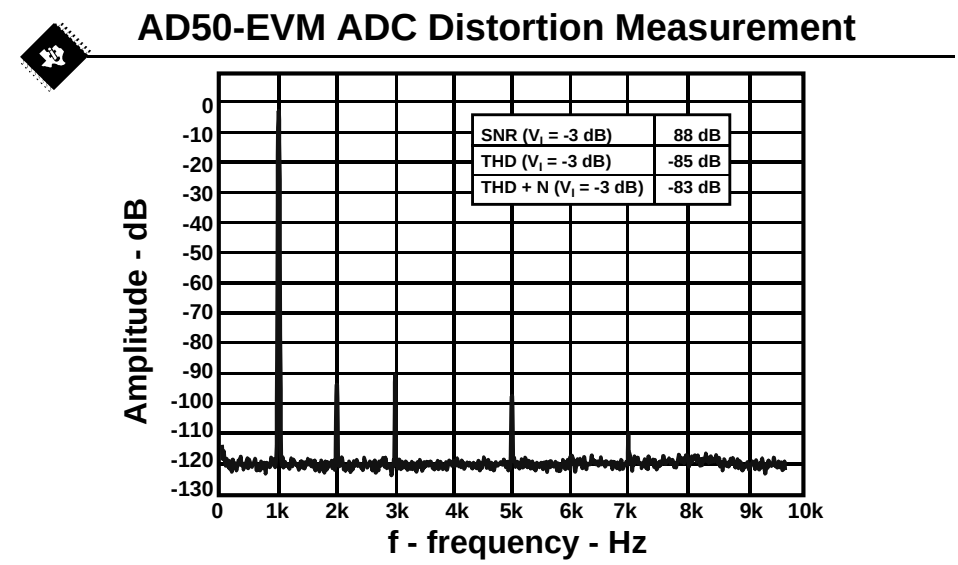
TLC320AD50 Single Supply Input Stage

In this example of an input stage design, only a single supply is required. The input signal is ac coupled by the 100 µF coupling capacitor and is level shifted to 2.5 V by half the op amp. The other half of the op amp provides a buffered 2.5 V supply. However, beside the advantages of a simple circuit and only a single supply, this proposal has also some disadvantages. The input must be ac coupled in order to allow the required level shifting. Furthermore, the TLC320AD50 has differential inputs, which are designed to provide immunity from noise and interference. To take advantage of this feature it is necessary to ensure that any noise at the reference point appears equally on both differential inputs. In this circuit, the INP input sees the noise directly whilst the INM input sees the noise amplified by 2. In addition to this, this input stage can only produce 50% of the differential voltage needed for maximum input. This effectively reduces the signal to noise ratio and dynamic range by 6 dB.



TLC320AD50 Output Stage Design, Differential to Single Ended Converter

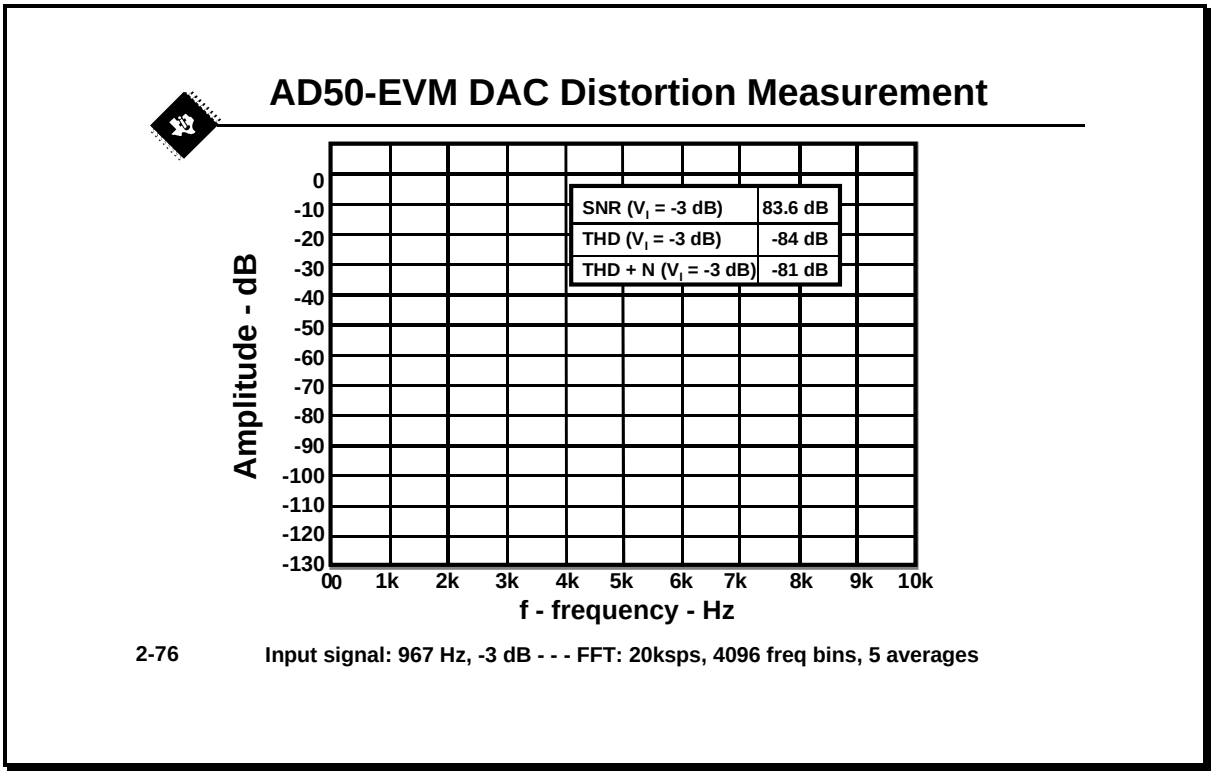
The D/A converter of the TLC320AD50 uses a pair of differential voltage outputs. The output needs to convert the differential signals to a single ended output, and to attenuate noise outside the pass-band. This filter is not a conventional reconstruction filter, since the AD50 has an integral low-pass reconstruction filter. This filter is a 12 kHz second order low-pass filter designed for use at 20 ksps and will be less effective at lower sampling rates. Since this filter only removes out of band noise it will be unnecessary in many applications.



2-75 Input signal: 1 kHz, -3 dB - - - FFT: 20ksps, 4096 freq bins, 5 averages

AD50-EVM ADC Distortion Measurement

To evaluate the performance of the ADC channel of the AD50-EVM, FFT measurements were performed. The input signal was a 1 kHz sinewave at –3 dB relative to maximum input. An audio analyzer (UPD, Rohde & Schwarz) was used to produce the test signal and to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 88 dB SNR, 85 dB THD and 83 dB THD+N.



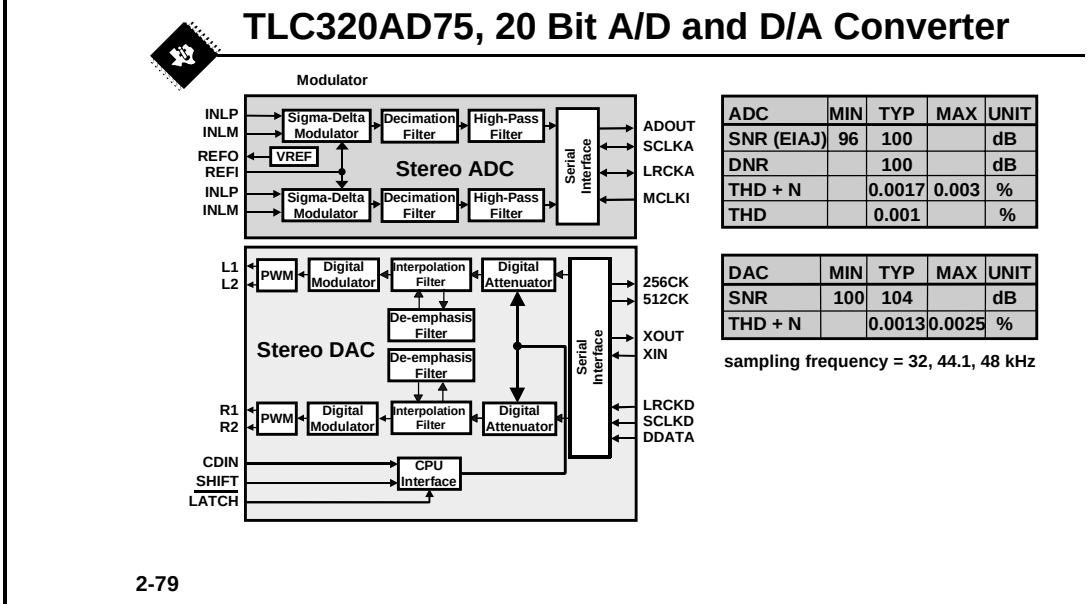
AD50-EVM DAC Distortion Measurement

The DAC was measured in 16 bit mode using a sine-wave table lookup program running on a TMS320C54x DSK+ coupled to an AD50-EVM. The picture shows an FFT plot of the output from the AD50-EVM. This was measured using a Rohde & Schwarz audio analyzer (UPD). The SNR was 83.6 dB, the THD was 84 dB and the THD+N was 81 dB.

Selection Guide: Analog Interface Circuits

Part Number	Band Pass Filter Hz	Low-Pass Filter Hz	Sampling Rate (max)	Sin x/x correction	Internal V Ref	Supply Voltage	PD (mW)	Ma / SL
TLC32040	300-3600	3400	19.2 kHz	No	Yes	+/- 5 V	430	M
TLC32041	300-3600	3400	19.2	No	No	+/- 5 V	430	M
TLC32042	200-3600	3400	19.2	No	Yes	+/- 5 V	430	M
TLC32044	100-3800	3800	19.2	Yes	Yes	+/- 5 V	430	M
TLC32045	100-3800	3800	19.2	Yes	No	+/- 5 V	430	M
TLC32046	300-7200	7200	25	Yes	Yes	+/- 5 V	430	M
TLC32047	300-11.4 k	11.4 k	25	Yes	Yes	+/- 5 V	430	M
TLC320AC01	up to 10.8 k	10.8 k	25	Yes	Yes	+ 5 V	110	M/S
TLC320AC02	up to 10.8 k	10.8 k	25	Yes	Yes	+ 5 V	110	M
TLC320AD50	up to 8.82 k	8.82 k	22.05	Yes	Yes	+ 5 V/+3V	100	M/S
TLC320AD55	up to 4.41 k	4.41k	11.025	Yes	Yes	+ 5 V	150	M
TLC320AD56	up to 8.82 k	8.82 k	22.05	Yes	Yes	+ 5 V/+3V	100	M

Audio Converters



ADC	MIN	TYP	MAX	UNIT
SNR (EIAJ)	96	100		dB
DNR		100		dB
THD + N		0.0017	0.003	%
THD		0.001		%

DAC	MIN	TYP	MAX	UNIT
SNR	100	104		dB
THD + N		0.0013	0.0025	%

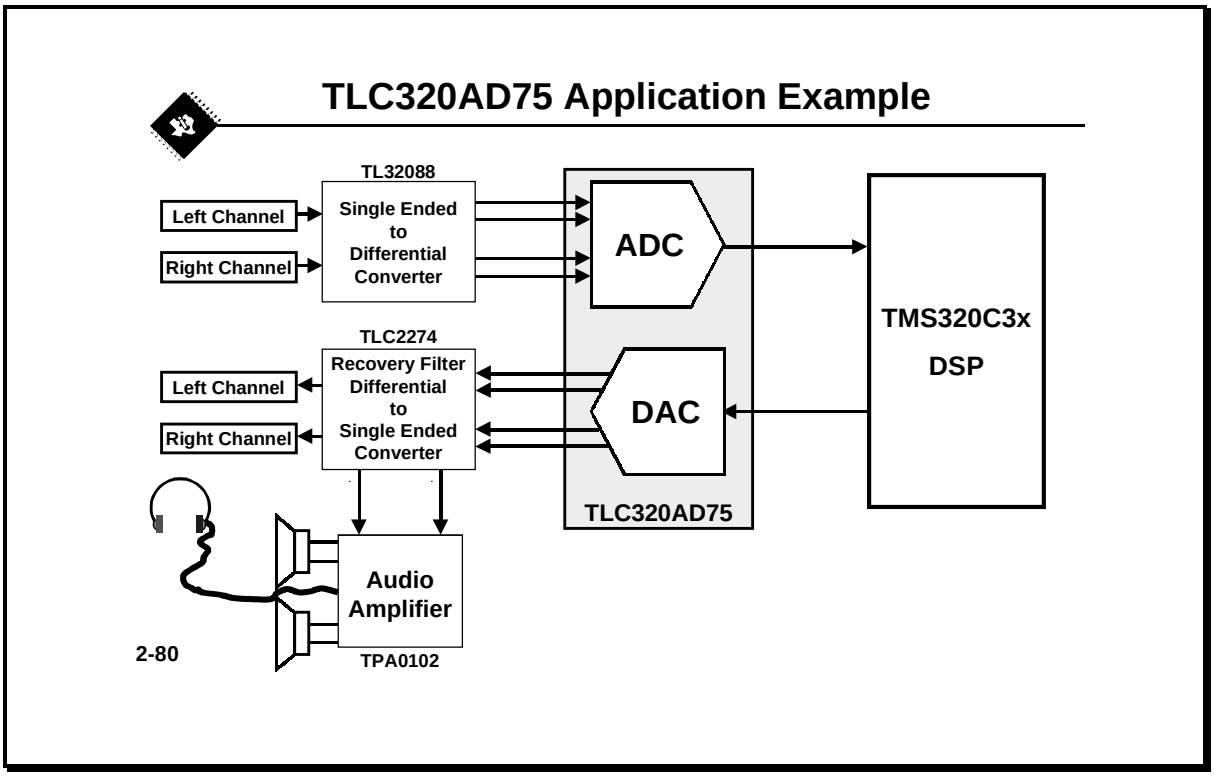
sampling frequency = 32, 44.1, 48 kHz

TLC320AD75, 20 Bit A/D and D/A Converter

The TLC320AD75C is a high-performance stereo 20-bit analog-to-digital and digital-to-analog converter (ADA) using sigma-delta technology to provide four concurrent 20-bit resolution conversions from both analog-to-digital (A/D) and digital-to-analog (D/A) signal paths. Additional functions provided are digital attenuation, digital de-emphasis filtering, soft mute, and on-chip timing and control. Control words from a host controller or processor are used to implement these functions.

The main features are:

- Single 5-V (Analog/Digital) Power Level and 3.3-V to 5-V Digital Interface Level
- Sample Rates up to 48 kHz
- 20-Bit Resolution Conversions
- Internal Voltage Reference (V ref)
- Serial Port Interface
- Differential Architecture
- DAC Provides PWM Output
- Digital De-emphasis Filtering for 32-, 44.1-, and 48-kHz Sample Rates for the DAC
- Digital Attenuation/Soft Mute Function for the DAC

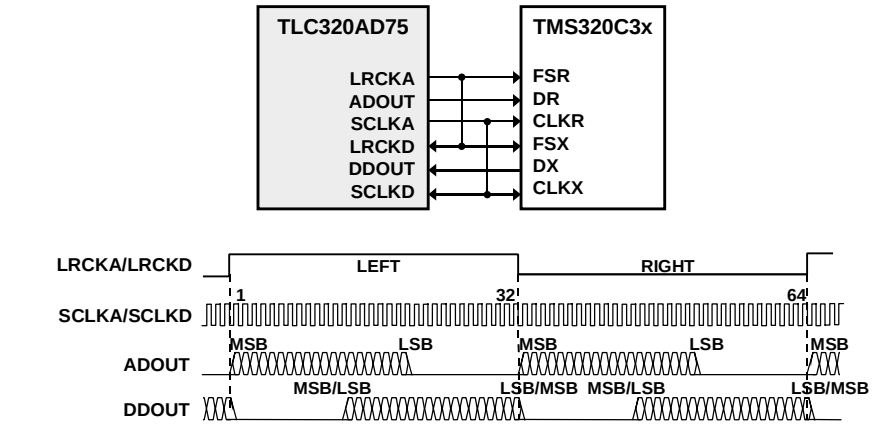


TLC320AD75 Application Example

The picture shows an application example with the TLC320AD75, which was used to convert analog audio data into digital format. The TMS320C3x is here used to read out the ADC digital data and to transmit digital data to the DAC which then can be converted into analog domain again. The DSP is here used to manipulate the digital data (echo cancellation, echo generation, filtering, equalizer function, etc.). On the analog output, an audio amplifier can be used to connect passive speakers or a headphone.

DSP I/F with 20-Bit Stereo Audio Codec

TLC320AD75



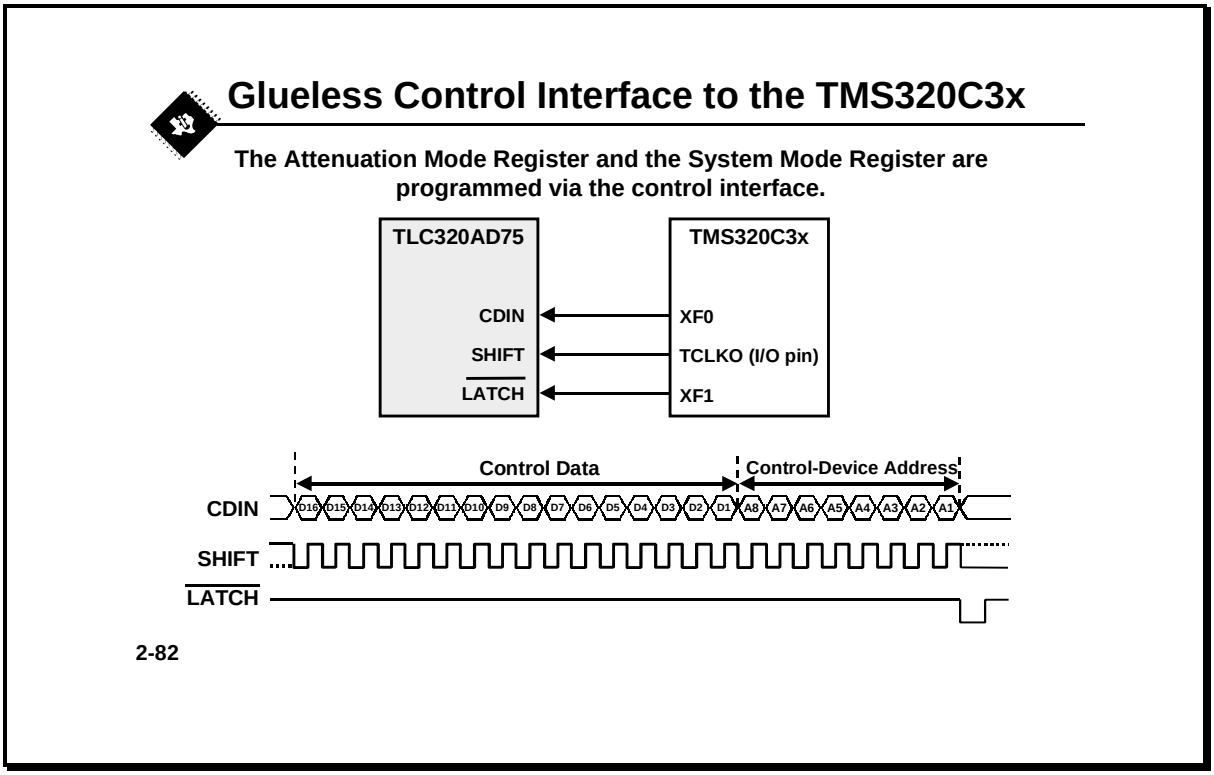
2-81

Interface of the TLC320AD75 to the TMS320C3x

The picture shows the glueless interface of the TLC320AD75 to the Texas Instruments digital signal processor TMS320C3x. To achieve this, the serial port of the DSP is configured in the variable mode. When the TLC320AD75 is configured as the master device (M_S is connected to V_{DD1}), the TLC320AD75C generates LRCKA and SCLKA from MCLKI. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

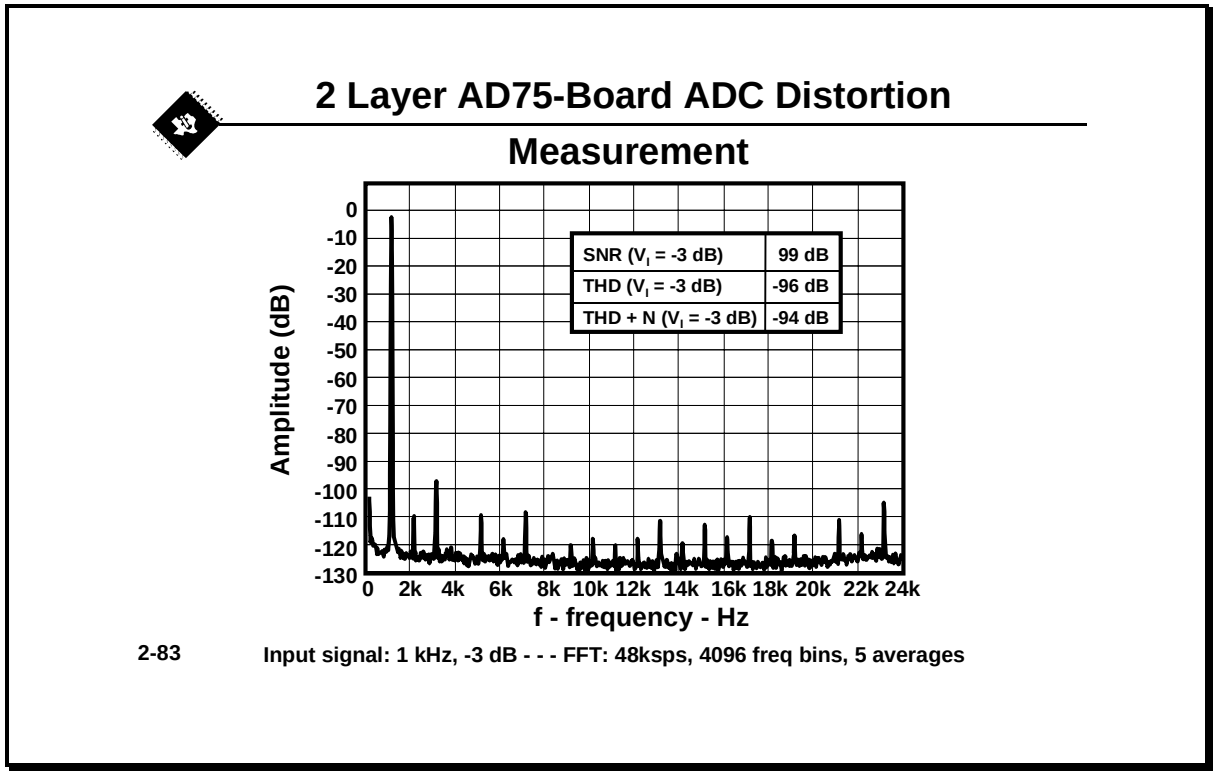
LRCKA is generated internally from MCLKI. The frequency of LRCKA is fixed at the sampling frequency, f_S (MCLKI/256). During the high period of LRCKA, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output (ADOUT). The conversion cycle is synchronized with the rising edge of LRCKA.

For the DAC, the conversion cycle is synchronized to the rising edge of LRCKD, and the data must meet the setup requirements specified in the timing requirements. The input data is 16 or 20 bits with the MSB or LSB first as selected in the system register. The recommended SCLKD frequency is 64 × f_S. The picture illustrates the input and output timing for ADC and DAC.



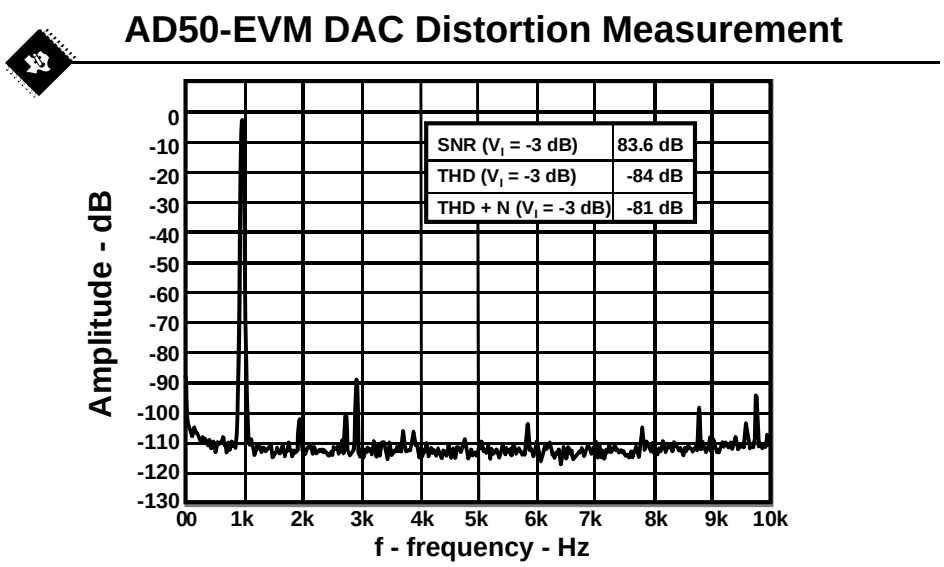
Glueless Control Interface to the DSP TMS320C3x

The TLC320AD75 has two internal registers, which are used to program the mode of the converter chip. These registers are accessible via a further interface. Also this interface can be built up glueless. It consists of three signals, SHIFT, CDIN and Latch. SHIFT is the clock signal of the interface. CDIN is the data information which has to be sent to the AD75. The LATCH input is used for latching the data information into the selected register of the device. The SHIFT signal is here generated with the timer pin TCLK0. The data bits are generated with the XF0 pin and the data is latched with the XF1 pin of the DSP.



2 Layer AD75-Board ADC Distortion Measurement

To evaluate the performance of the ADC channel of the 2-layer board of the TLC320AD75, FFT measurements were performed. The input signal was a 1 kHz sine wave at –3 dB relative to maximum input. An audio analyzer (UPD, Rohde & Schwarz) was used to produce the test signal and to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 99 dB SNR, 96 dB THD and 94 dB THD+N.



2-76 Input signal: 967 Hz, -3 dB - - - FFT: 20ksps, 4096 freq bins, 5 averages

2 Layer AD75-Board DAC Distortion Measurement

To evaluate the performance of the DAC channel of the 2-layer board of the TLC320AD75, FFT measurements were performed. The input signal was a 1 kHz sine wave at -3 dB relative to maximum input, which was generated by an audio analyzer (UPD, Rohde & Schwarz). This analyzer was also used to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 106 dB SNR, 95 dB THD and 94 dB THD+N.

Selection Guide: Audio Converters

Stereo Audio ADCs

	Resolution	Signal-to-noise	Dyn. Range	Signal-to-noise + distortion / Total harmonic distortion	Convers. time	max samp rate	inputs	internal ref	Suppl.Voltage	Interface
Stereo Audio ADCs										
TLC320AD57C	**2 x 18-bit**	97dB	95dB	91dB	20.8uS	48kHz	2	Y	5V	serial
TLC320AD58C	**2 x 18-bit**	100dB	95dB	93dB	20.8uS	48kHz	2	Y	5V	serial
Stereo Audio ADC/DAC										
TLC320AD75C	**2 x 20-bit**	100dB(ADC)	100dB(ADC)	0.003%	20.8uS	48kHz	2 + 2	Y	5 / 3.3-5V	serial
		104dB(DAC)								
AC '97 Multimedia Audio Codec with Volume control, Mixer, Mux, Plug & Play										
TLC320AD91	**2 x 18-bit**	80dB(ADC)			20.8uS	48 kHz	4 +	Y	3.3 - 5V	serial
		90dB(DAC)					(4 x 2)			
Set Top Box Stereo DAC with digital & analog input mux, Volume/Balance control, wideband analog Mux										
TLC320AD80	**2 x 16-bit**	85dB		0.02%		48kHz	9	Y	5V	serial

Data Converter Application Reports

Interfacing the TLV1544/TLV1548 ADC to Digital Processors	SLAA022
Interfacing the TLC5540 ADC to the TMS320C203-80 DSP	SLAA032
Interfacing the TLC5510 ADC to the TMS320C203 DSP	SLAA029
Interfacing ADCs TLC5540/10 to the DSKPLUS DSP Starter Kit TMS320C54X	SLAAE14
Interfacing the TLV1572 ADC to the TMS320C203 DSP	SLAA026A
Interfacing the TLV1544 ADC to the TMS320C50 DSP	SLAA025
Interfacing the TLV1544 ADC to the TMS320C203 DSP	SLAA028
Minimizing Input Design Problems with the TLV5590	SWCA001
Interfacing the TLV1549 10-Bit Serial-Out ADC to Popular 3.3-V Microcontrollers	SLAA005
Microcontroller Based Data Acquisition Using the TLC2543 12-Bit Serial Out ADC	SLAA012
Interfacing the TLC2543 ADC to the TMS320C25 DSP	SLAA017
Signal Acquisition and Conditioning with Low Supply Voltages	SLAA018
Understanding Data Converters	SLAA013
TLC320AD57C Sigma-Delta Stereo Analog-to-Digital Converters	SLAA010
TLC320AD58C Sigma-Delta Stereo Analog-to-Digital Converter	SLAA015
TLC2932: PLL Building Block with Analog VCO & Phase Frequency Detector	SLAA011B

This is a representative sample and was accurate when this workbook was printed. For a complete up to date listing of application reports, designer note pages and EVMs please check the TI web site.