FPGA XILINX-BASED NEURAL NETWORK FRAGMENT HARDWARE IMPLEMENTATION WITH ADJUSTABLE WEIGHTS AND ACTIVATION FUNCTION IN REAL-TIME APPLICATIONS

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Abstract. The prototype of feedforward neural network scalable fragment has been developed. We have implemented the ability to choose the fast-changing data - weights or input patterns. This option is embedded for the sake of partial independence of our fragment with respect to the task which is desired to be solved. The fragment is based upon VIRTEX-E FPGA (XCV400E-pq240) which consists of 570 thousand system gates. Neurochip design methology has been worked through with respect to given technology using Xilinx ISE 5.2 CAD.

Introduction

While designing a neural network algorithm, or any other computational algorithm, one should take care of two major criteria of its effectiveness – accuracy and task time. Using general purpose computers for neural algorithm computation is not effective in respect to perfomance to cost ratio, because complicated problems are bound to be solved with large neural networks. In accordance with a huge amount of literature dedicated to this issue we may conclude that the most effective NN-algorithm hardware implementation would be a neuroships based upon FPGA's (leader manufacturers – Xilinx, Altera) [1, 2].

To design the neural network fragment at this stage of our researches we use XCV400E-pq240 Xilinx chip which integration is 570 thousand system gates.

Neural network fragment structure

To fight the problem of the impossibility to place all network on one chip one should divide it into several scalable fragments. In our research we deal with a feedforward NN-fragment since this topology is a most common in real tasks. The fragment consists of 8 neurons. Weights and input patterns digit capacity equals 8. Each neuron has 8 inputs. We've chosen vertical cascading type which increases the number of neurons in one layer [3].

Fragment on-chip implementation

The fragment occupies 86% of XCV400E chip resources. Fragment consists of 64 constatnt coefficient multipliers (all work in parallel), 56 two-port adders, block single-port RAM which volume is 256x16 bit for each neuron (8 blocks altogether), mode control block[4]. Circuit clock speed: **90 MHz**. Computational time of one output vector: **70 ns**.

Operation and modes

The fragment is designed to acquire 8 components of input vector in parallel, parallel multiplication of these by the contents of multipliers' internal RAMs, parallel addition of the 8 products and parallel activation in each neuron. There are two modes of operation at this point: direct computation, weights and activation function renewal (can be chosen). In this design we have eliminated (on purpose) the difference in logical meaning of weights and input patterns. Now they differ only in a rate of change. Thus we've provided a partialy invariance in respect to the task. Think of the slow changing weights and fast patterns when doing your recognition or classification project. Then think of the slow patterns and fast weights when deal with system of algebraic equations.

Conclusions

The fragment developed is being used in practical applications. Moreover, it'll be a basis of future neural systems. Worked throught design methology in Xilinx ISE 5.2. CAD will make a great contribution in a development of neural network algorithms being developed in our center.

References

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