UNITRODE
Design Note

A High Performance Linear Regulator for Low Dropout Applications

by: Dave Zendzian

Introduction

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down and regulating the existing 5V system supply. To complicate matters further, the performance of these devices is directly related to supply voltage. This results in a need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. As of late, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design offers several desirable features including low output noise and wide bandwidth resulting in excellent transient load response.

This design note presents a linear regulator capable of maximizing the performance of these digital systems. The regulator is designed to meet the following system requirements:

V_{IN} = 5V, ±10%
V_{OUT} = 3.3V, ±5%
I_{OUT} = 3.5A typical, 4A maximum

Transient Response:
5% to 75% I_{OUTmax} in 100nsec, V_{REG} = ±5%

Topology Review

The regulator is implemented using a UC3833, precision linear controller. This IC includes all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier and an uncommitted output stage. Providing a driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. An innovative, switchmode current limiting technique is also implemented by the UC3833, significantly reducing power dissipation during fault conditions.

The crux of the design lies in the selection of a pass device. Requirements for the selected power device include operation under very low input/output differential voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage compared to a Darlington and simpler base drive than an NPN configuration. However, the gain of these devices is typically quite low, resulting in the need for significant base drive current. As the output requirements of the regulator increase the base current losses quickly become excessive, thereby decreasing the efficiency, along with the advantages of the linear regulator.

This leaves the P-channel MOSFET as the most likely candidate. While older generation P-channel devices are plagued with high on-resistance, recent advancements in high cell density technology have led to substantial reductions in R_{DSon}. Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL is a 50A, 30V, logic level P-channel device with a maximum on-resistance of only 30mΩ. The maximum gate threshold voltage of 2.0V is necessary due to the 5V input requirement of this application. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in transconductance mode it can be biased with minimal drive current, further improving the efficiency of the regulator.

Bulk output capacitance is added to the design in order to help meet the 100nsec load transient requirement. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time charge is removed from the capacitor and its volt-

age correspondingly decreases until the control loop can catch the error and correct for the increased load. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship I = CdV/dt. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected.

Design Details

Figure 1 illustrates the final design. Resistors R4 and R5 provide the bias for the pass transistor, Q1. By including emitter resistor R5, the UC3833 drive transistor's β is eliminated from the loop gain expression, thereby simplifying the compensation. Resistors R6 and R7 provide voltage feedback to the UC3833 while components R3, C2 and C3 compensate the voltage and current loops. Further compensation of the current loop is provided by the pole-zero pair introduced by R8, C7 and C8.

Current control is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the 100mV comparator threshold, the UC3833 begins to modulate the output driver. The duty cycle is approximately 5% with on and off-times set by timing components C1 and R2. During the on-time, the current sense amplifier provides constant output current by maintaining 135mV across R1. Duty cycle protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation, and not the full short circuit power.

Output capacitors were chosen based upon their ESR/ESL specifications and package style. The output capacitance is implemented using three surface mount, solid tantalum capacitors in parallel. This acts to reduce the equivalent ESR and ESL by 1/3, keeping the associated voltage transients within specification. Sprague 595D capacitors were used, providing an equivalent impedance of approximately 13mΩ typical and 60mΩ max at 100kHz. The surface mount package helps to further reduce the parasitic effects induced by component leads.

In order to achieve the expected performance, careful attention must be paid to circuit layout. The circuit should be laid out using a single point ground referenced to the return of the output capacitor. In addition, all high current carrying traces should be made as short and wide as possible in order to

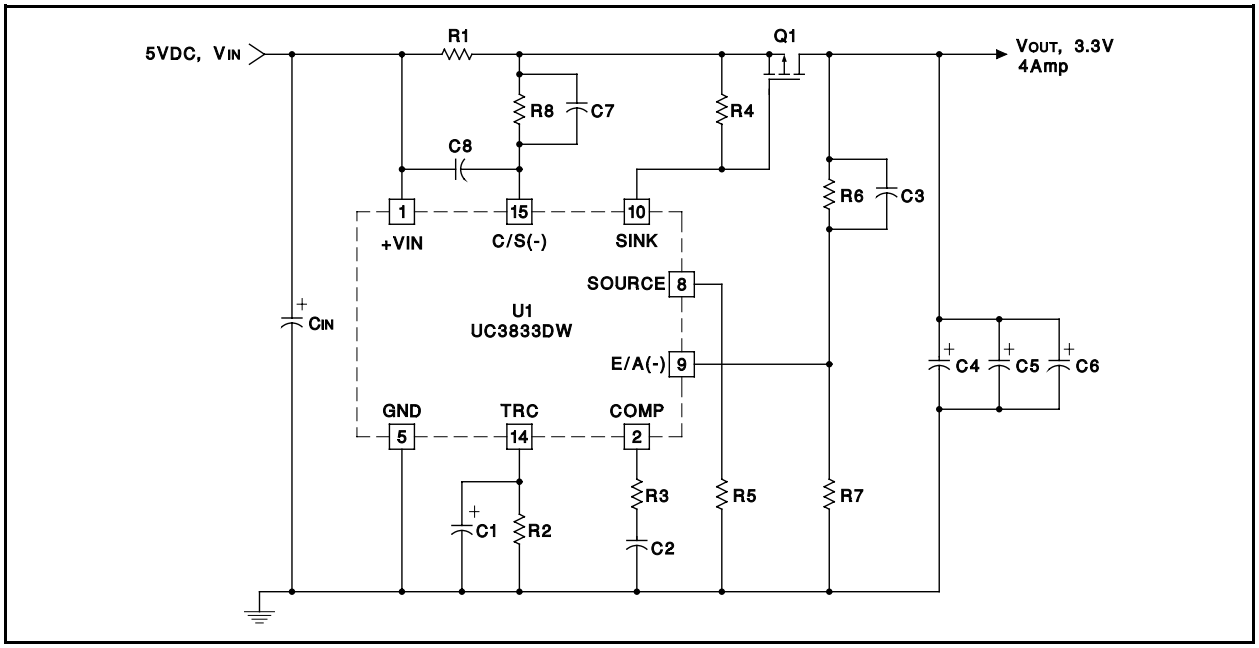

Figure 1. A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

minimize the effects of parasitic resistance and inductance. To illustrate the importance of these concepts, lets examine the effect of a 1.5" PCB trace located between the output capacitor and the UC3833 ground reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A. Each of these effects can be minimized by optimizing the layout and using generous amounts of copper on all high current runs.

Thermal control is provided by heatsinking the power MOSFET pass device. Any heatsink of 7.5°C/W or lower will keep the junction temperature of the MOSFET below 125°C at ambient temperatures up to 50°C and worst case operating conditions.

Performance

In a typical application of 3A out with 5.0V in, the efficiency of the regulator is 65.5%. Under maximum load and worst case conditions the efficiency drops to 60%. During a short circuit, the regulator limits the peak output current to approximately 6A by design. At the 5% duty cycle set by C1 and R2, the average current is limited to 300mA, resulting in only 2W of power dissipated in the MOSFET as opposed to the potential dissipation of 32W in a constant current application!

Worst case DC regulation of ±3% is accomplished using the UC3833 in conjunction with 1% feedback resistors. If a tighter tolerance is required the UC3832 can be substituted for the UC3833 along with 0.1% resistors. The UC3832 includes provisions for an external voltage reference, allowing increased performance over the UC3833's 1% internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 2 illustrates how the design behaves during the specified 100nsec load transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 2. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable state within 40µsec. Figure 3 shows the same response with a

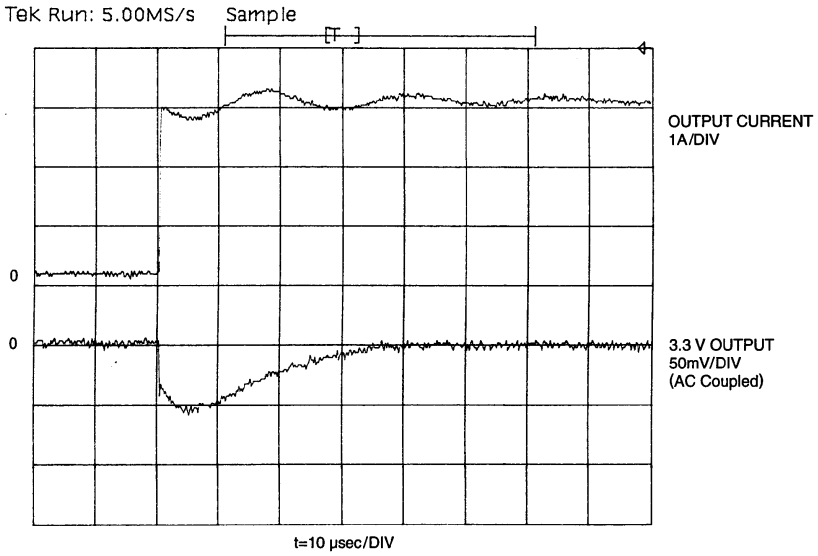

Figure 2. Transient response of the regulator illustrated in Figure 1 with a time base of 10µsec. The top trace is the load current on the output of the regulator. The bottom trace shows the transient recovery of the regulator's output when the load is stepped from 200mA to 3A.

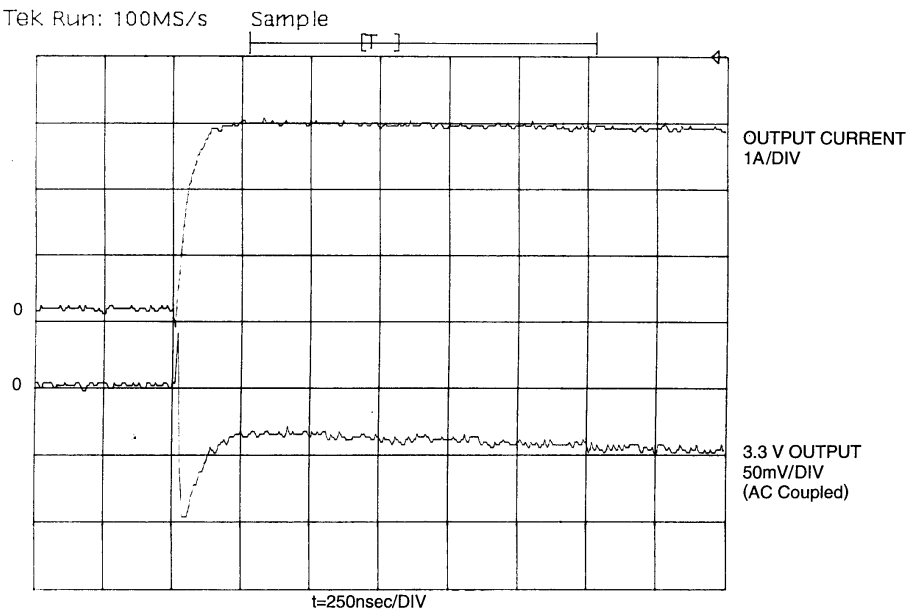

Figure 3. Transient response of the regulator illustrated in Figure 1 with a timebase of 250nsec. The top trace is the load current on the output of the regulator. The bottom trace shows the initial output transient resulting from the equivalent impedance of the output capacitor during a load step from 200mA to 3A.

timebase expanded to 250nsec. In this plot the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

The circuit described in this design note can be easily modified to accommodate a variety of output voltage and current requirements. For additional information regarding the UC3832/3 linear controllers consult Unitrode application note U-116. Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectively.

Parts List:

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1,C8 = 1µF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2,C3 = 0.1µF		
R3,R8 = 100Ω	C4,C5,C6 = 270µF		
R4 = 300Ω	C7 = 3300pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460