UNITRODE

Low Power Pulse Width Modulator

UCC1570
UCC2570
UCC3570

FEATURES

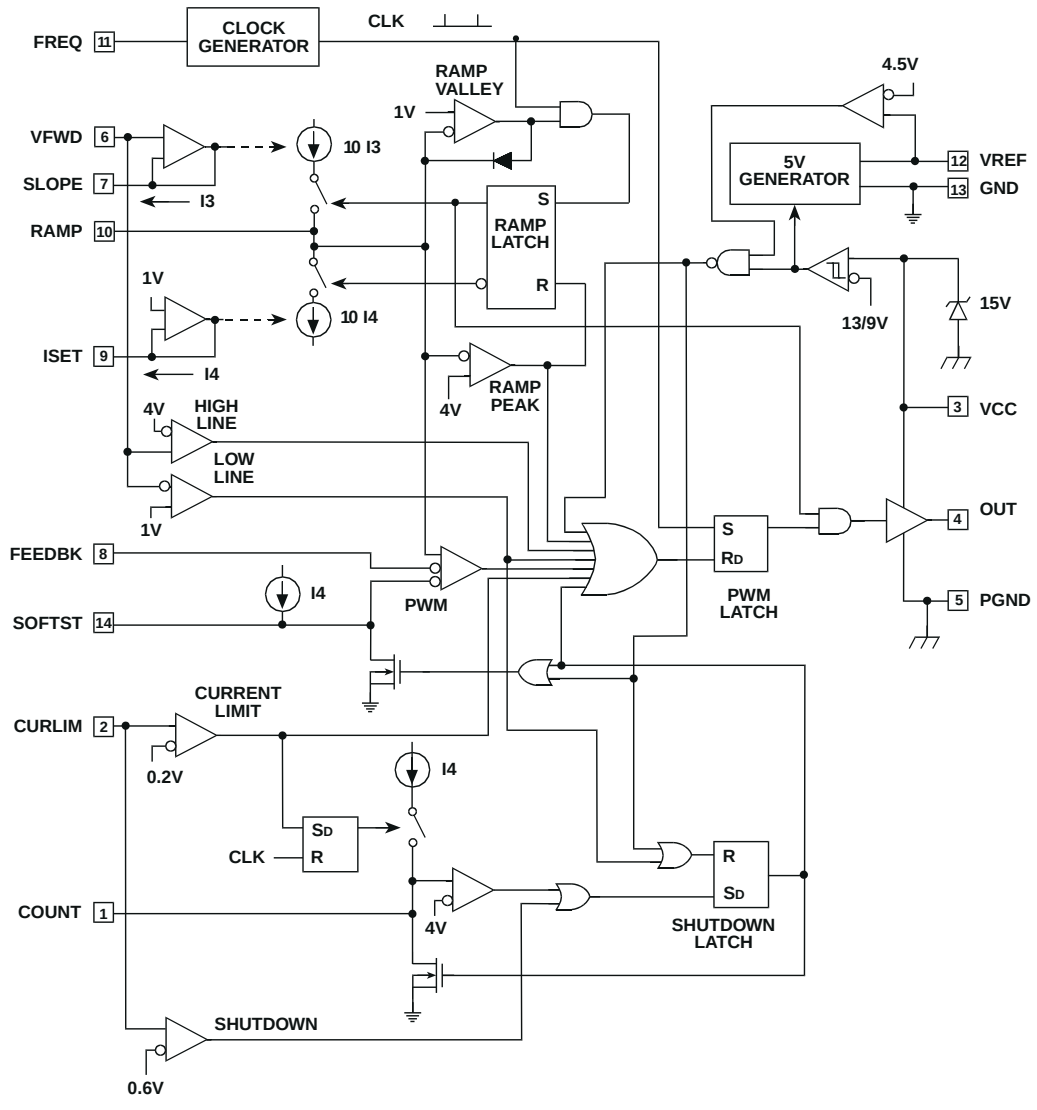
- Low Power BiCMOS Process
- 85µA Start-up Current
- 1mA Run Current
- 1A Peak Gate Drive Output
- Voltage Feed Forward
- Programmable Duty Cycle Clamp
- Optocoupler Interface
- 500kHz Operation Soft Start
- Fault Counting Shutdown
- Fault Latch Off or Automatic Restart

DESCRIPTION

The UCC1570 family of pulse width modulators is intended for application in isolated switching supplies using primary side control and a voltage mode feedback loop. Made with a BiCMOS process, these devices feature low startup current for efficient off-line starting with a bootstrapped low voltage supply. Operating current is also very low; yet these devices maintain the ability to drive a power MOSFET gate at frequencies above 500kHz.

Voltage feedforward provides fast and accurate response to wide line voltage variation without the noise sensitivity of current mode control. Fast current limiting is included with the ability to latch off after a programmable number of repetitive faults has occurred. This allows the power supply to ride through a temporary overload, while still shutting down in the event of a permanent fault. Additional versatility is provided with a maximum duty cycle clamp programmable within a 20% to 80% range and line voltage sensing with a programmable window of allowable operation.

BLOCK DIAGRAM



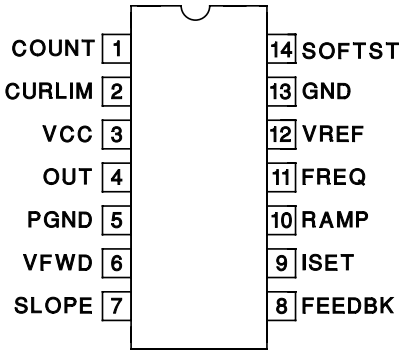
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Limit Supply Current to 20mA) . . . . . Self Limiting at 15 V
Supply Current . . . . . +20mA
Analog Inputs (CURLIM, VFWD, FEEBK) 6V
Programming Current (I (SLOPE), I (ISET)) . . . . . -1mA
Output Current (I (OUT)) . . . . . DC . . . . . ±180mA
. . . . . Pulse (0.5ms) . . . . . ±1.2A

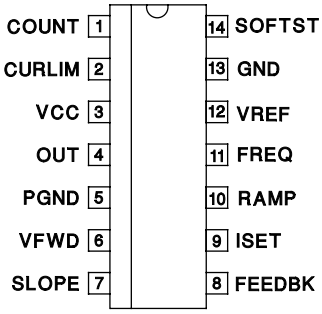
Note: *All voltages are with respect to GND. Currents are positive into the specified terminal.*

CONNECTION DIAGRAMS

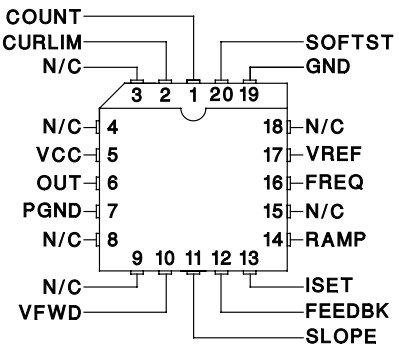
DIL-14 (TOP VIEW)
N or J PACKAGE



SOIC-14 (TOP VIEW)
D PACKAGE



PLCC-20 (TOP VIEW)
L Or Q PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Reference					
VREF	VCC=10 to 13V, I(VREF) = 0 to 2mA	4.9	5	5.1	V
Line Regulation	VCC = 10 to 13V		2	10	mV
Load Regulation	I(VREF) = 0 to 2mA		2	10	mV
Short Circuit Current	VREF = 0		10	50	mA
VCC					
Vth (On)		12	13		V
Vth (Off)		8	9	10	V
Hysteresis		3	4	5	V
VCC	I(VCC) = 10mA	13.5	15	16	V
I(VCC) Start	VCC = 11V, VCC Comparator Off		85	150	µA
I(VCC) Run	VCC Comparator On		1	1.5	mA
Line Sense					
Vth High Line Comparator		3.9	4	4.1	V
Vth Low Line Comparator		0.96	1	1.04	V
lib (VFWD)			0	±100	nA
Oscillator					
Frequency		90	100	110	kHz
Ramp Generator					
I(RAMP)/I(SLOPE)		9	10	11	A/A
-I(RAMP)/I(ISET)		9	10	11	A/A
Peak Ramp Voltage		3.8	4	4.2	V
Valley Ramp Voltage		0.95	1	1.05	V
ISET Voltage Level		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Soft Start					
Saturation	VCC = 11V, VCC Comparator Off		25	100	mV
I(SOFTST)/I(ISET)		0.8	1	1.2	A/A
Pulse Width Modulator					
lib(FEEDBK)			0	±100	n A
FEEDBK	Zero Duty Cycle	0.9	1	1.1	V
	Maximum Duty Cycle, Note 1	3.8	4	4.2	V
Current Limit					
lib(CURLIM)			0	±100	nA
Vth Current Limit		180	200	220	mV
Vth Shutdown		500	600	700	mV
Fault Counter					
Vth		3.8	4	4.2	V
Vsat			0	100	mV
I(COUNT)/I(ISET)		0.8	1	1.2	A/A
Output Driver					
Vsat High	I(OUT) = -100mA		0.4	1	V
Vsat Low	I(OUT) = 100mA		0.4	1	V
Rise/Fall Time	C(OUT) = 1nF, Note 1		20	100	ns

Note 1: *This parameter guaranteed by design but not 100% tested in production.*

PIN DESCRIPTION

VCC: Chip supply voltage pin. Bypass to PGND with a low ESL/ESR 0.1µF capacitor plus a capacitor for gate charge storage. Lead lengths must be minimum.

PGND: Ground pin for the output driver. Keep connections less than 2cm. Carefully maintain low impedance path for high current return.

OUT: Gate drive output pin. Connect to the gate of a power MOSFET with a resistor greater than 2 ohms. Keep connection lengths under 2cm.

VFWD: Voltage Feed Forward and Line Sense pin. Connect to input DC line using a resistive divider.

SLOPE: Program the charging current for RAMP with a resistor from this pin to GND. This pin will follow VFWD.

FEEDBK: Input to the pulse width modulator comparator. Drive this pin with an optocoupler to GND and a resistor to VREF. Modulation input range is from 1V to 4V.

ISET: A resistor from this pin to GND programs RAMP discharge current, FREQ current, SOFTST current, and COUNT current.

RAMP: Ramp Pin. Connect a capacitor to GND. Rising slope is programmed by current in SLOPE. This slope is compared to FEEDBK for pulse width modulation. The falling slope is programmed by the current in ISET and used to limit maximum duty cycle.

FREQ: Oscillator pin. Program the frequency with a capacitor to GND.

VREF: Precision 5V reference, and bypass point for internal circuitry. Bypass this pin with a 1µF minimum capacitor to GND.

GND: Analog ground. Connect to a low impedance ground plane containing all analog low current returns.

SOFTST: Soft start pin. Program with a capacitor to GND.

COUNT: Program the time that fault events will be tolerated before shutdown occurs with a capacitor and resistor to GND.

CURLIM: Current Limit Sense pin. Terminates OUT gate drive pulse for inputs over 0.2V. Enables fault counting function (COUNT). For inputs over 0.6V, the shutdown latch is activated.

FUNCTIONAL DESCRIPTION

(Note: Refer to Typical Application for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.

Power Sequencing

VCC normally connects through a high impedance (R5) to the rectified line, with an additional path (R6) to a low voltage, bootstrap winding on the power transformer. VFWD normally connects to a divider (R1 and R2) from the rectified line. For circuit activation, all of the following conditions are required:

1. VFWD between 1V and 4V
2. VCC has been under 9V (to reset the shutdown latch)
3. VCC over 13V

FUNCTIONAL DESCRIPTION (cont.)

At this time, the circuit will activate. I(VCC) will increase from its start up value of 85μA to its run value of 1mA. The capacitor on SOFTST is charged with a current determined by

$$-I(SOFTST) = 1V/R4.$$

When SOFTST rises above 1V, output pulses will begin and I(VCC) will further rise to a level dictated by gate charge requirements as I(VCC) ≈ 1mA + $Q_T f_S$. With output pulses, the low voltage bootstrap winding should now power the controller. If VCC falls below 9V, the controller will turn off and the start sequence will reset and retry.

Vcc Clamp

An internal shunt regulator clamps V_{CC} so that it will not exceed 15V.

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and back low when RAMP either crosses FEEDBK or equals 4V. If, however, any of the following occur, OUT is immediately driven low for the remainder of the clock period:

1. VFWD is outside the range of 1V to 4V
2. CURLIM is greater than 0.2V
3. FEEDBK or SOFTST is less than 1V

Normal output pulses will not resume until the beginning of the next clock period in which none of the above conditions exist.

Current Limiting

CURLIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse overcurrent control for excessive loads. This comparator also causes C_F to be charged for the remainder of the clock cycle. The charging current is

$$-I(COUNT) = 1V/R4$$

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than (4 * R4.)/(1-D_{MAX})

Latched Shutdown

If CURLIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SOFTST and COUNT, and reduce I(VCC) to approximately 1 mA. When, and if, VCC falls below 9V, the shutdown latch will reset and I(VCC) will fall to 85μA, allowing the circuit to restart. If VCC remains above 9V, an alternate restart will occur if VFWD is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or CURLIM pins.

Deadtime Control

The voltage waveform on RAMP has independently controlled rising and falling edges. At the start of the clock period, RAMP is at 1V and rises to 4V. It then discharges back to 1V and awaits the next clock period. OUT can only be high during the rising part of the waveform, while it is positively blanked off during the falling portion. Setting the -dV/dt slope by R4 from ISET to GND establishes a minimum deadtime as:

$$td = 0.3 * R4 * C_R.$$

Choose R4 between 20k and 200k and C_R greater than 50pF. In order to have a pulse at OUT in the next clock period, RAMP must fall to 1V prior to the end of the current period. If it does not, OUT will remain low for the entire next clock period.

Voltage Feedforward

The +dV/dt on RAMP is made proportional to line voltage. The slope is:

$$dV/dt = 10 * VFWD / (R3 * C_R),$$

where VFWD is line voltage scaled by R1 and R2. Therefore, a changing line voltage will accomplish an immediate proportionate pulse width change without any action from the feedback amplifier. This will result in constant volt-second drive to the power transformer providing both international voltage operation, and excellent dynamic line regulation. VFWD is intended to operate over a 4:1 range (1V to 4V) with undervoltage and overvoltage sensors designed to drive OUT low if this range is exceeded. Choose R3 between 20k and 200k.

Frequency Set

A capacitor from FREQ to GND will determine a constant clock frequency. Frequency is:

$$F = 1.8/(R4 * C_T).$$

If required, frequency can be trimmed down from the above equation by the addition of R_T from FREQ to GND. The reduction in frequency is a function of the ratio of R_T/R4. R_T should be greater than 2.4 * R4 for reliable operation.

External synchronization can be accomplished by coupling a narrow pulse to a resistor inserted in series with the ground side of C_T. The value should be less than R4/200 and the synchronizing pulse width should be less than 5% of the oscillator period.

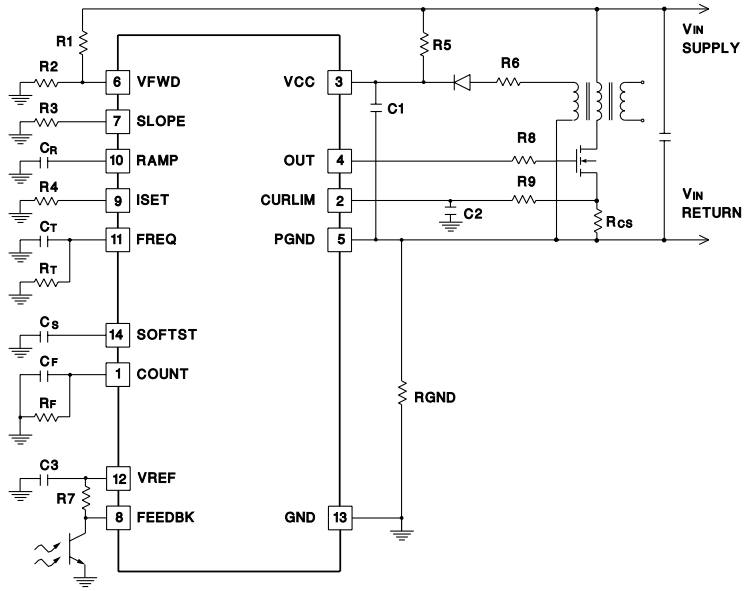
FUNCTIONAL DESCRIPTION (cont.)

External synchronization can also be accomplished by driving FREQ with an CMOS inverter. The inverter must be able to sink 4 * I4 with at a voltage less than the 3.5V upper threshold of the oscillator. It must also be able to source 36 * I4 at a voltage greater than the 1.5V lower threshold of the oscillator. As long as FREQ is held high, the output is guaranteed to be low.

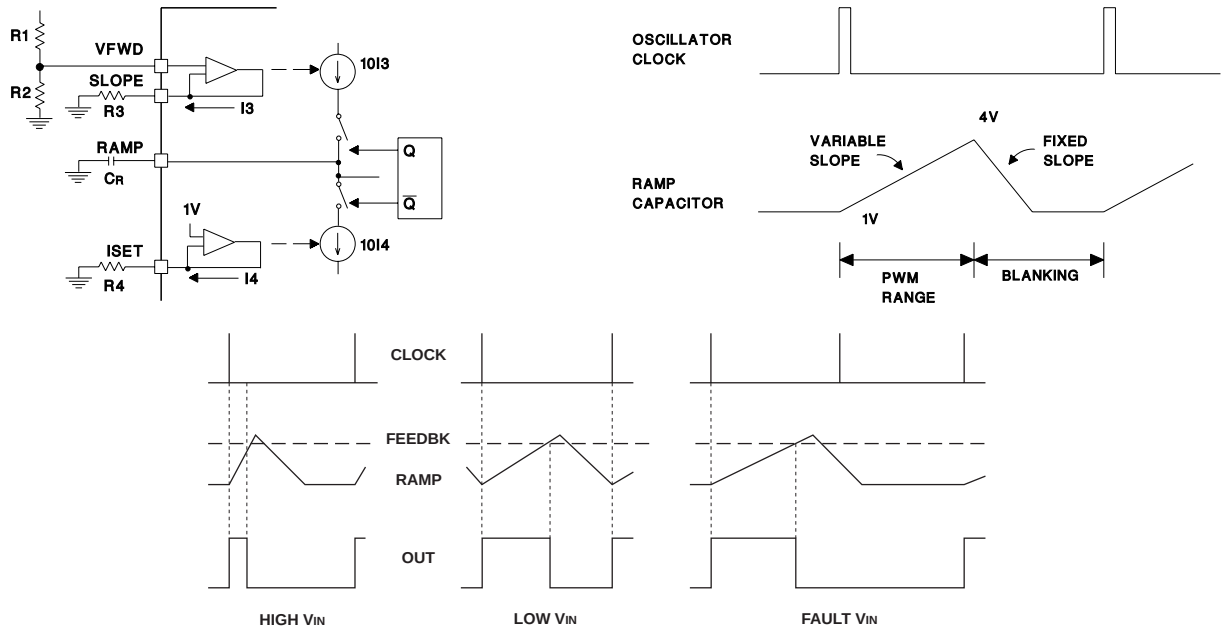
Gate Drive Output

The UCC1570 is capable of 1A peak output current. Bypass VCC with at least 0.1µF directly to PGND. Use a capacitor with low equivalent series resistance and inductance. The connection from OUT to the MOSFET gate should have a 2 ohm or greater damping resistor and the length should be minimized. A low impedance connection must be established between the MOSFET source (or the ground side of the current sense resistor), the VCC bypass capacitor and PGND. PGND should then be connected by a single path (shown as RGND in the application) to GND.

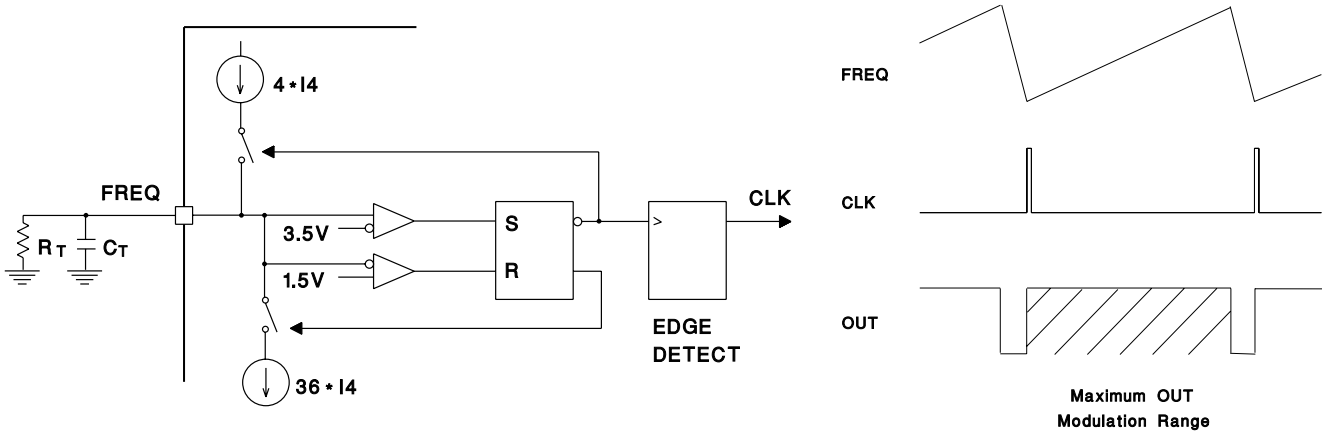
UCC1570 TYPICAL APPLICATION



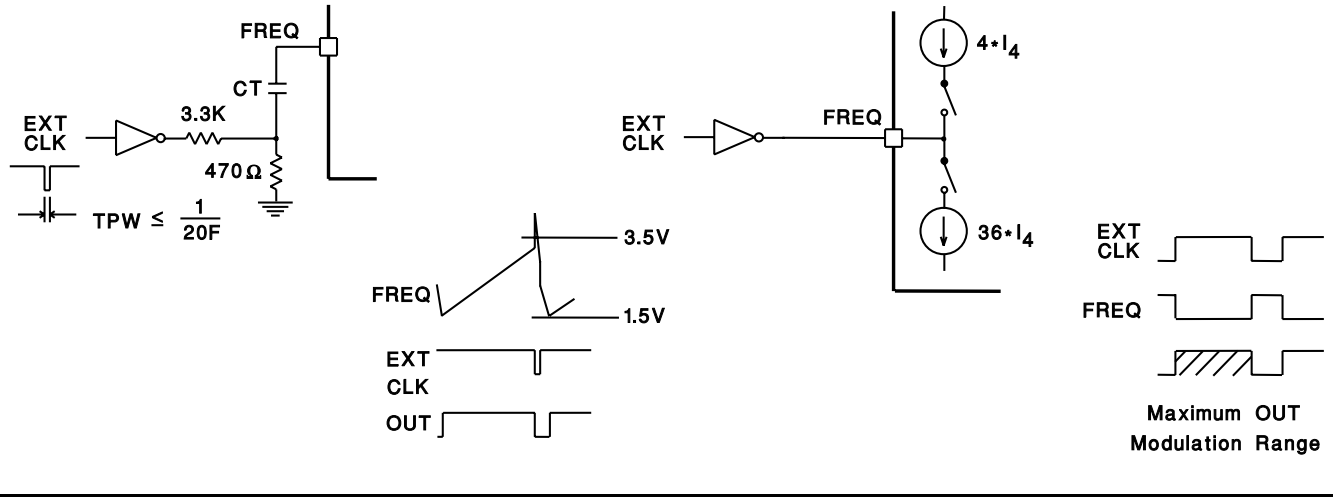
RAMP AND PWM WAVEFORMS



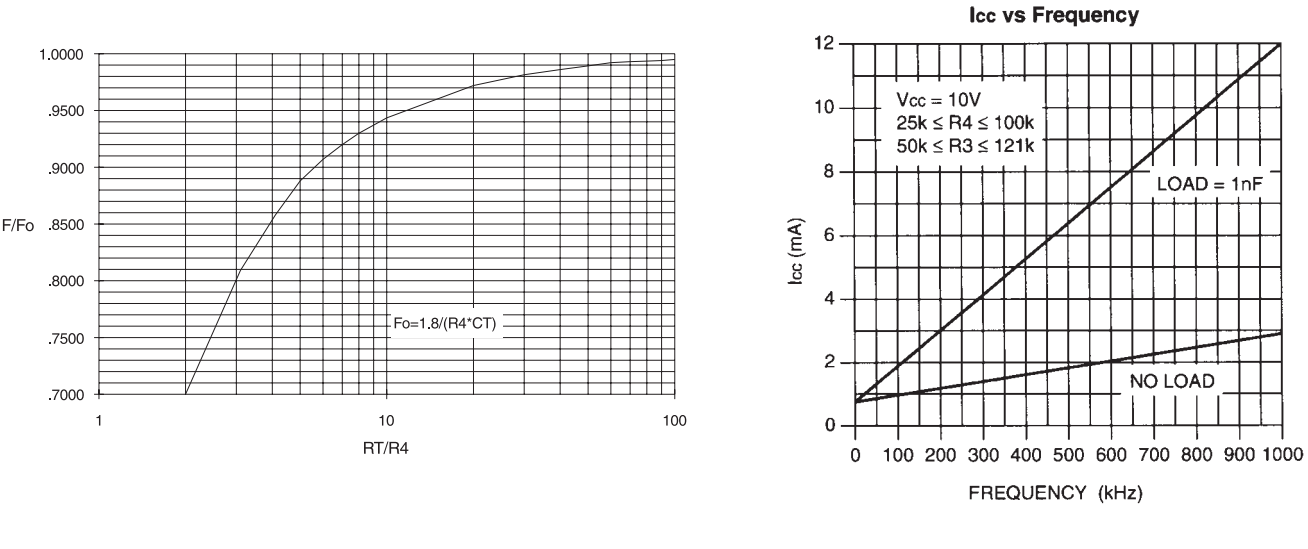
CLOCK GENERATOR



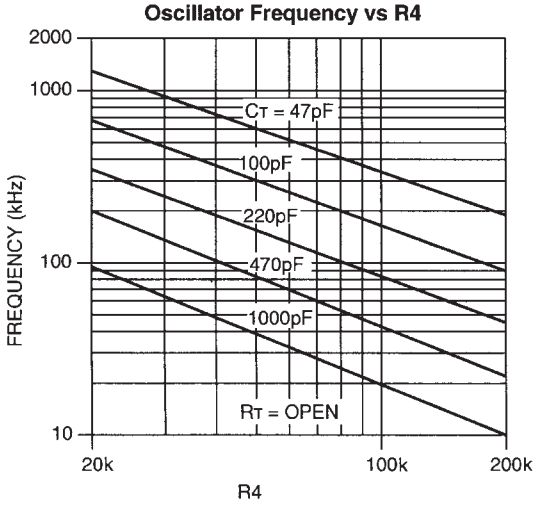
EXTERNAL CLOCK SYNCHRONIZATION



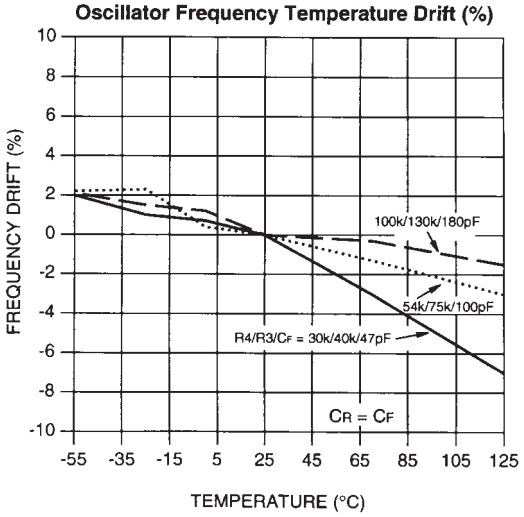
FREQUENCY DEPENDENCE ON RT/ R4 RATIO



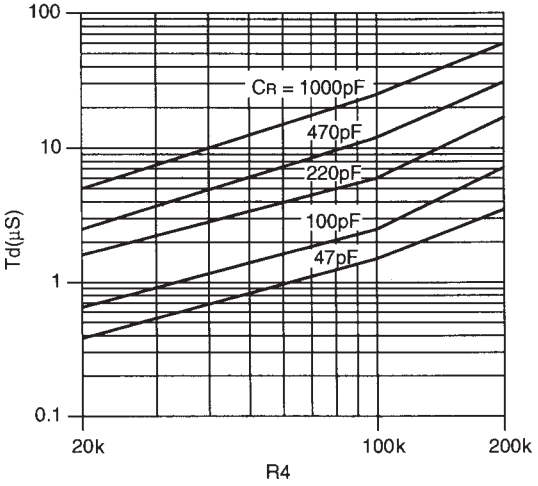
Oscillator Frequency vs R4



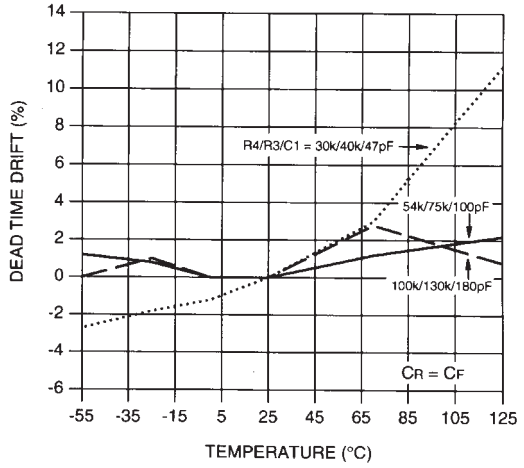
Oscillator Frequency Temperature Drift (%)



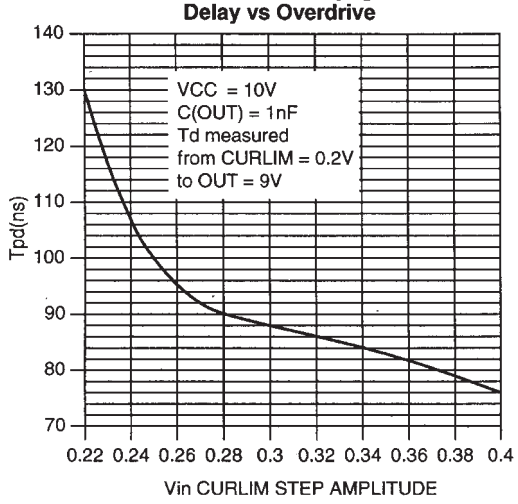
Minimum Dead Time vs R4



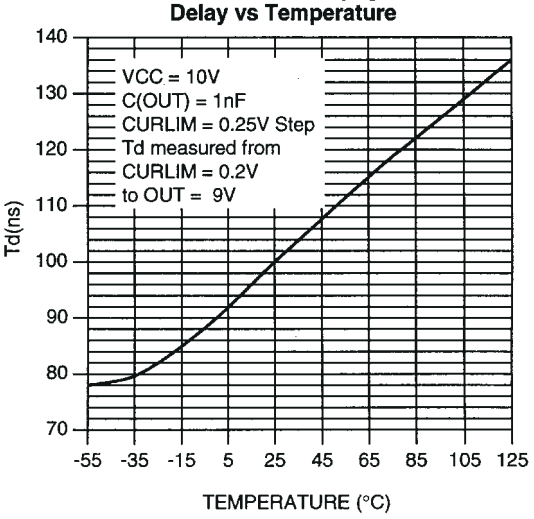
Minimum Dead Time Temperature Drift (%)



CURLIM to OUT Propagation Delay vs Overdrive



CURLIM to OUT Propagation Delay vs Temperature



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